Coding for Unreliable Flash Memory Cells

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Mapping Information to Voltage Levels in TLC

- Most Significant Bit MSB
- Center Significant Bit CSB
- Least Significant Bit LSB

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  1. Erase the block. (block= 2^{20} cells)
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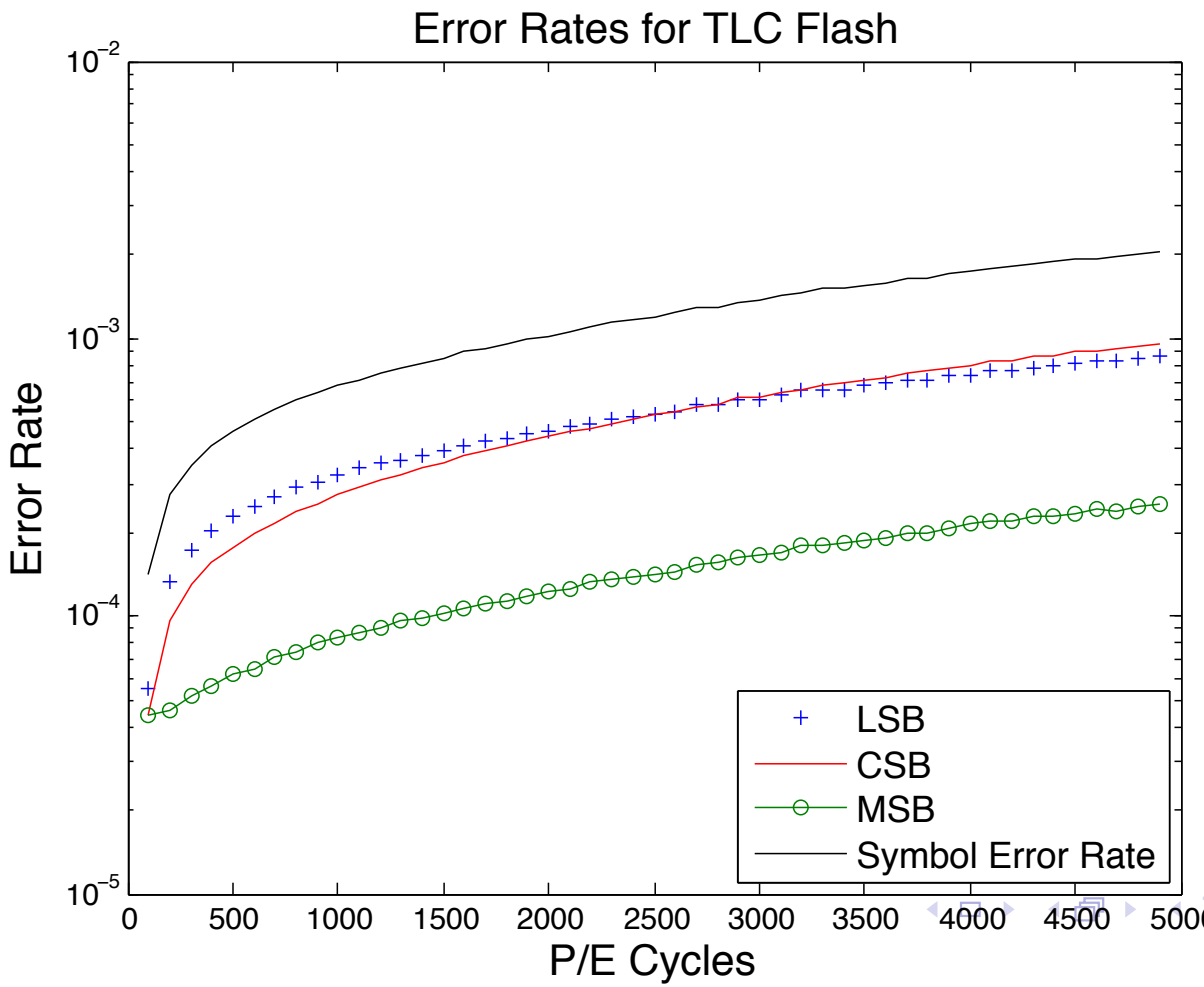
- On the other 99 cycles, the block was erased and all-zeros were written.

Raw Error Rate



Observation 1: Error Patterns Within a Symbol

Number of bits in symbol that err	Percentage of errors
1	0.9617
2	0.0314
3	0.0069

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- An unreliable Flash cell is a cell that experienced ≥ 50 errors across the lifetime of the device.
- We identified 62659 (of the 134217728 total cells tested) unreliable Flash cells.
- These cells accounted for over 10% of the total errors measured.

Observation 3: Unreliable Flash Cells Have Prominent Error Patterns

Programmed state	Percentage of Errors
000	0.4745
000	0.1630
010	0.0711
000	0.0676
001	0.0558
001	0.0525
011	0.0186

High Voltage

011
010
000
001
101
100
110
111

Low Voltage

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  1. Code corrects errors where most of the errors affect only a single bit within each Flash cell (Observation 1).
  2. Code allows unreliable Flash cells to be programmed at low voltage levels (Observations 2,3).

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- Example over alphabet of size 8:
  $(45702) -> (100\ 101\ 111\ 000\ 010)$

Error Vectors

Definition (Graded Bit-Error Vector)

The length-nm vector $\boldsymbol{e} = (\boldsymbol{e}_0, \boldsymbol{e}_1, \ldots, \boldsymbol{e}_{n-1})$, where each m-bit vector $\boldsymbol{e}_i$ represents a symbol of size 2^m, is a $[t_1, t_2; \ell_1, \ell_2]$-bit-error-vector if

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3. $|\{i : wt(\boldsymbol{e}_i) > \ell_1\}| \leq t_2$.

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  - There is 1 **symbol that has more than** 1 **bit** in error.

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- The code $\mathcal{C}$ is referred to as an $[t_1, t_2; \ell_1, \ell_2; s_1, s_2]_{2^m}$ **dynamic-bit-error-correcting code**.

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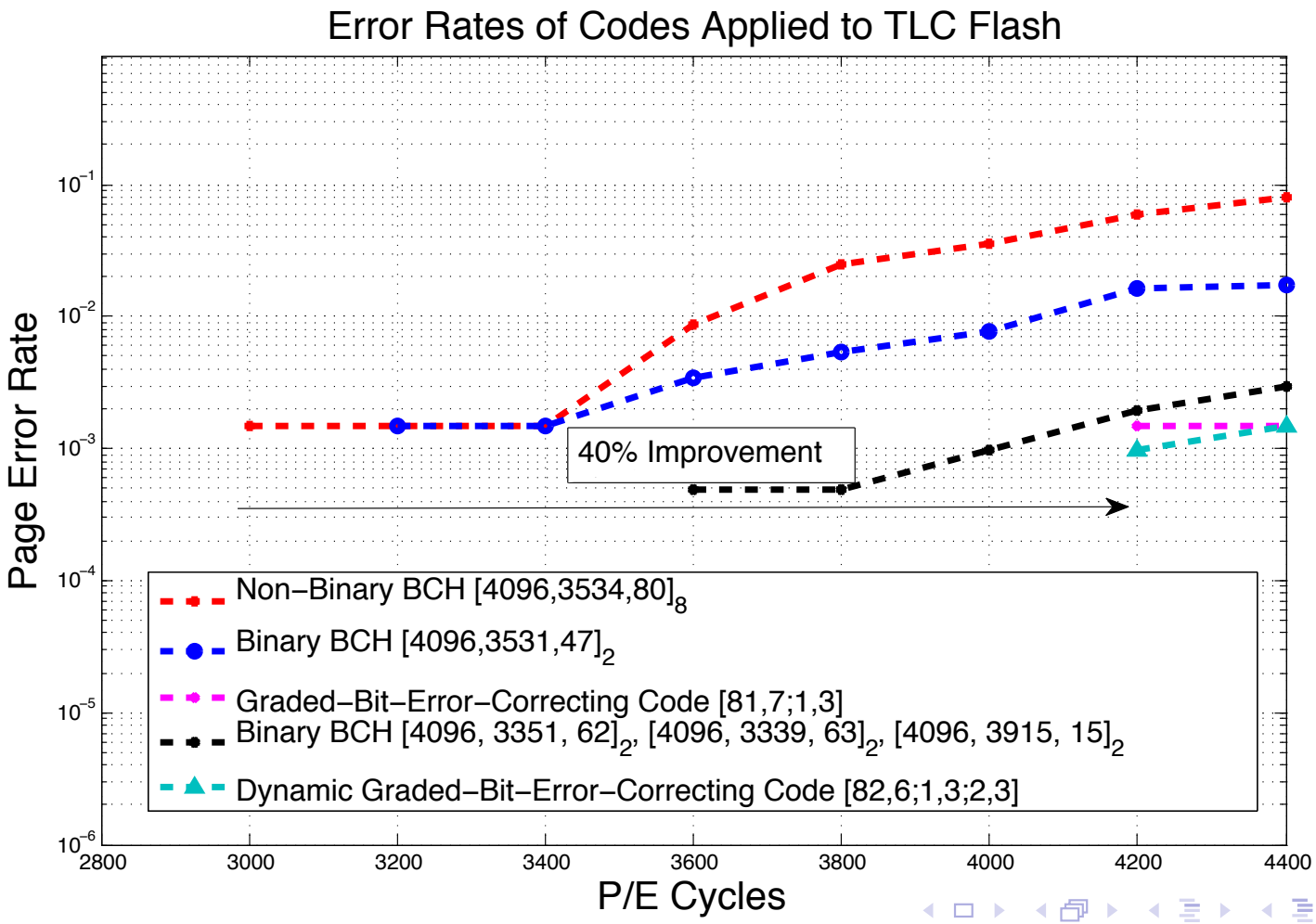
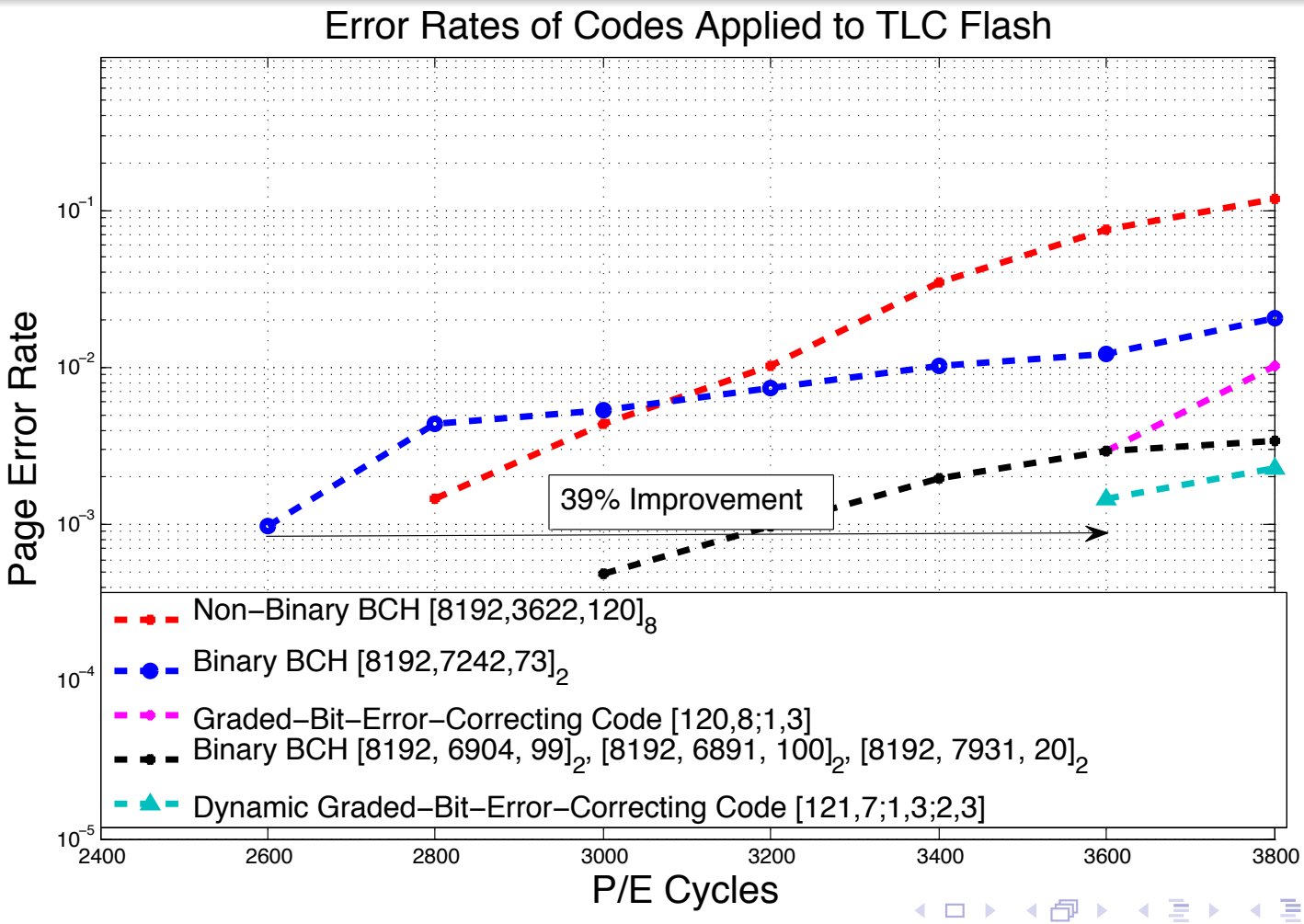
- For each graph, the codes compared have the same length and the same rate.

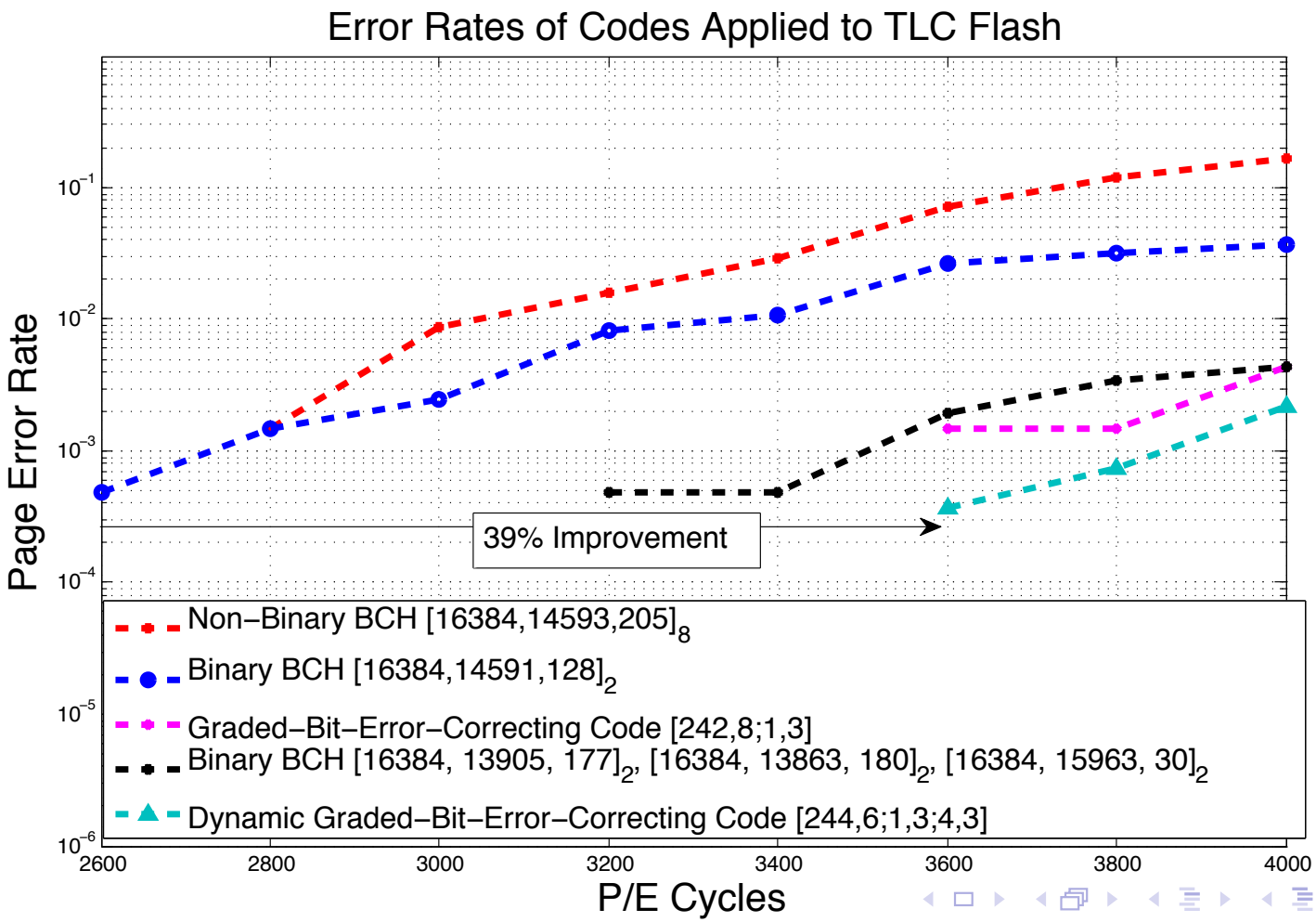
Results for block length 4096



Results for block length 8192



Results for block length 16384



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- Errors that occur within these newer Flash devices tend to follow certain patterns.
- By taking into account the dominant error patterns observed on a TLC Flash cell, we designed more efficient error correction codes.

Thank You

New center on Coding for Storage at UCLA:
http://www.loris.ee.ucla.edu/codess

Kick-off day on 9/19/2013!

Registration is free.
Register early, space is limited.