FLASH RELIABILITY, BEYOND DATA MANAGEMENT AND ECC

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AGENDA

Section 1: Flash Reliability

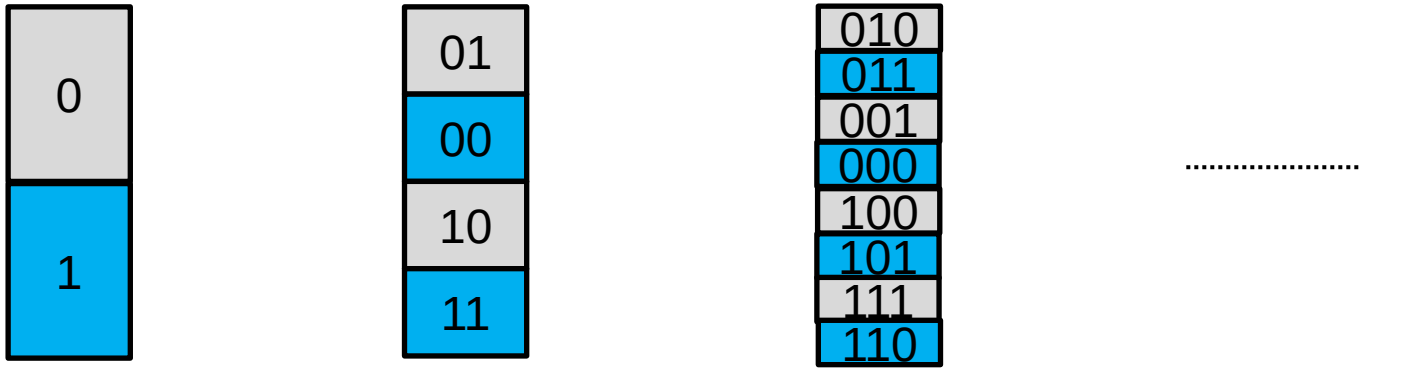
Section 2: Components to Improve Flash Reliability

Section 3: FLASHPRO Media Manager

Section 4: Conclusion

FLASH RELIABILITY

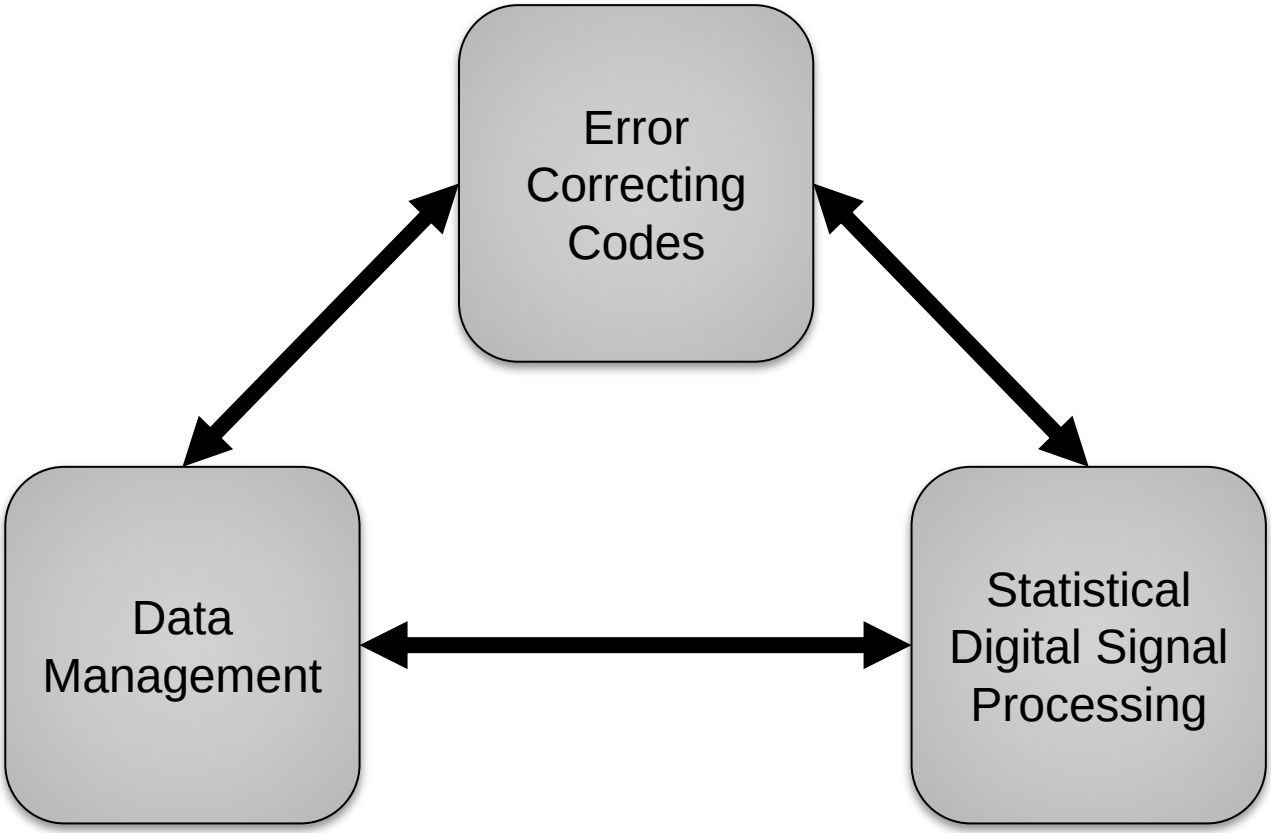
- Two major trends are driving NAND Flash Capacity and Cost:
  - Flash geometry
  - Number of bits stored in a cell



SLC (1-bit per cell) | MLC (2-bit per cell) | TLC (3-bit per cell) | QLC (4-bit per cell)

Both trends significantly degrade Flash endurance and reliability

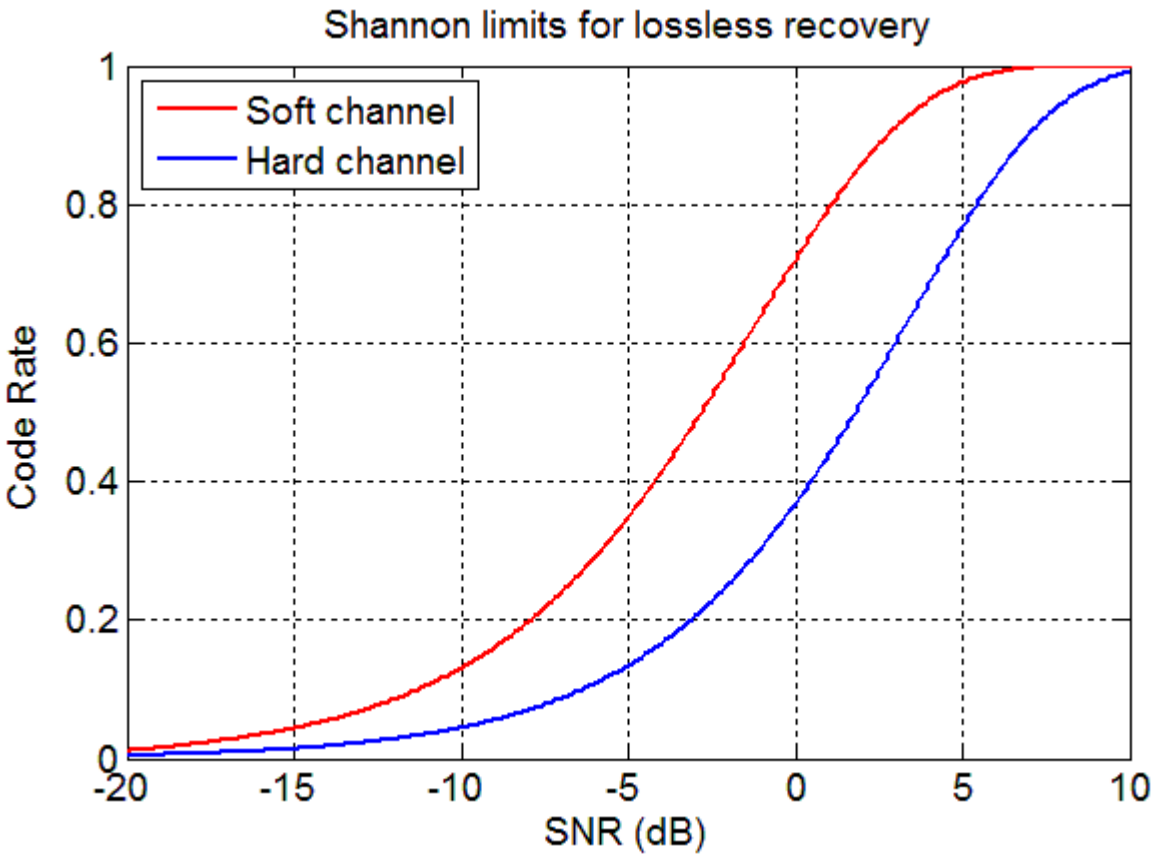
IMPROVING FLASH RELIABILITY



- 3 Major components to improve Flash reliability:
  - Data Management
  - Error Correcting Codes
  - Statistical Digital Signal Processing (S-DSP)

SHANNON LIMIT

- Shannon limit is the theoretical limit on the code rate that enables error free transmission/data recovery
- Our goal is to get as close as possible to the Shannon limit



ERROR CORRECTING CODES

- BCH codes are running out of steam
  - complexity dramatically increases with “t” (correction capability)
  - can’t take advantage of soft-data
  - Its performance is limited to the Shannon limit for hard channel
- LDPC codes
  - Smart implementation of LDPC codes are low power and cost effective
  - Near Shannon-limit performance
  - Take advantage of soft-data
  - Have been proven in communication and HDD spaces
  - FPGA implementations are available
- Other Codes
  - Remember, we can’t cross Shannon-limit
  - Cost of implementation is generally higher than LDPC

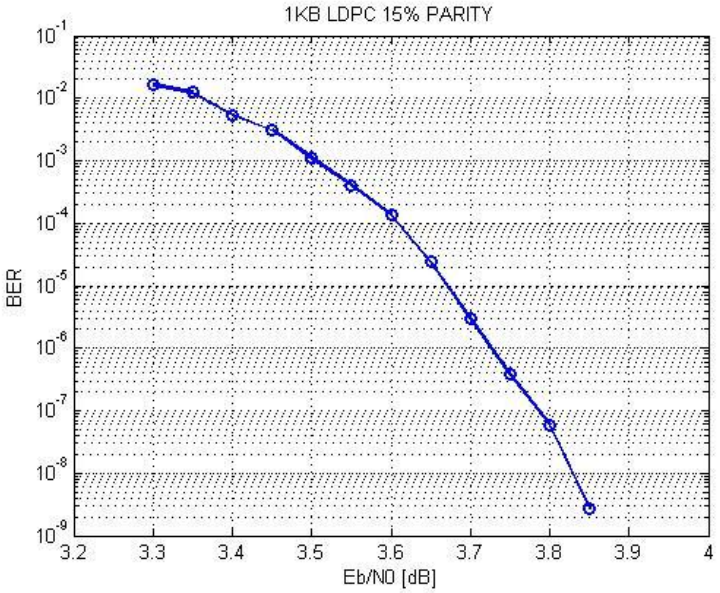
FLASH LDPC VS. COMMUNICATION STANDARDS AND HDD

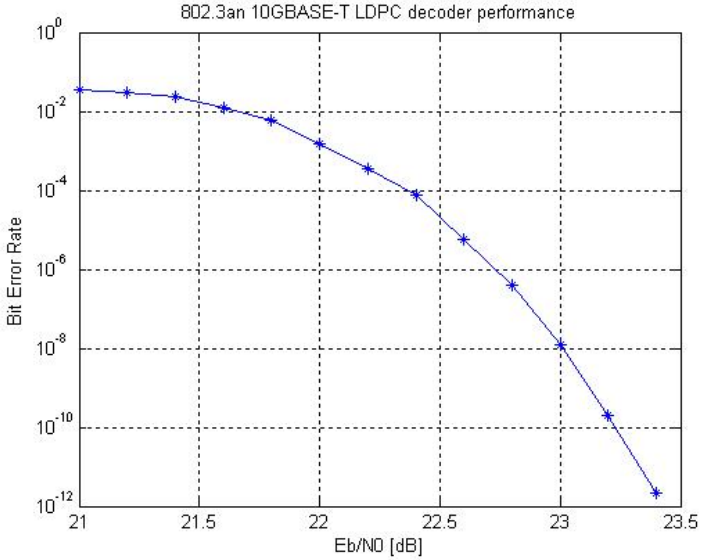
IEEE Standard	Application	CW Size (Byte)	Parity (%)	Data Rate (Mbyte/s)	Comments
802.11n	Wireless LAN	81, 162, 243	50, 33, 25, 17	75	Optional but used by everybody
802.11ac	Wireless LAN	81, 162, 243	50, 33, 25, 17	866	Mandatory
802.15	UWB	150, 165	50, 37.5, 25, 20	125	
802.3an	10G Ethrnet	256	15.5	800	
No Standard	HDD	0.5KB to 4KB	10 to 13	up to 500	
No Standard	FLASH	1KB to 4KB	5 to 15	400-4000	access to manufacturer secret commands required

- Reference: IEEE standard publications

FLASH LDPC VS. COMMUNICATION STANDARDS (2)

- 10GBaseT (IEEE 802.3an) SNR Plot vs. a custom code generated for Flash
- Flash works at a much lower SNR





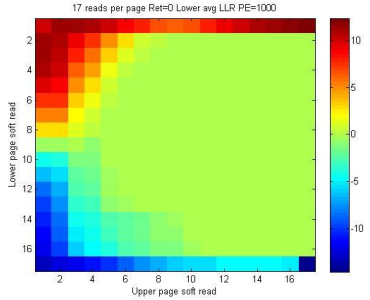
LDPC CODE FOR FLASH

- We need LDPC code that is optimized for Flash
- LDPC codes based on communication standards will not work for Flash
  - All are based on fixed codes (matrix) provided by IEEE
  - CodeWord size is usually very small
  - Amount of parity is usually very high
- To get the best out of LDPC for Flash it should work together with Statistical Digital Signal Processing (S-DSP)

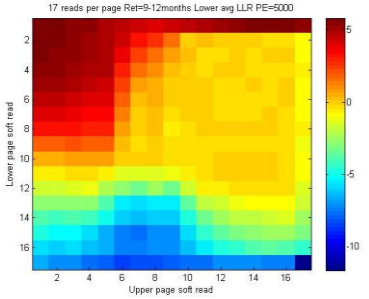
STATISTICAL-DSP: FLASH VARIABILITY

- Capturing statistical variation among different Flash vendor samples and operating conditions

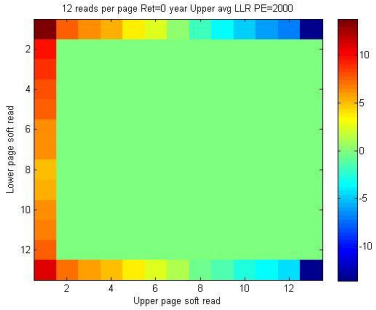
Flash Vendor A,
Consumer 1Xnm MLC, P/E=1000



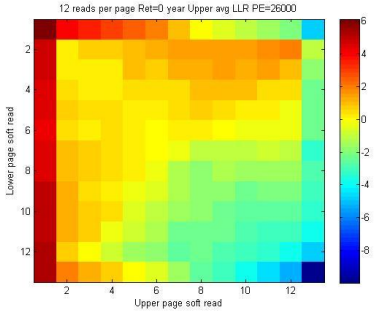
Flash Vendor A,
Consumer 1Xnm MLC, P/E=5000



Flash Vendor B,
Enterprise 2Ynm MLC, P/E=2000



Flash Vendor B,
Enterprise 2Ynm MLC, P/E=26000



STATISTICAL-DSP AND LDPC CODES

- Statistical Digital Signal Processing guarantees LDPC to always work close to Shannon limit
- Improves quality of LLRs (Log Likelihood Ratio) that is used as input of LDPC decoder
- S-DSP uses adaptive algorithms to maintain optimal performance
  - Monitors the performance and behavior of the Flash memory
  - As Flash degrades over time the S-DSP adapts to achieve maximum reliability

FLASHPRO MEDIA MANAGER

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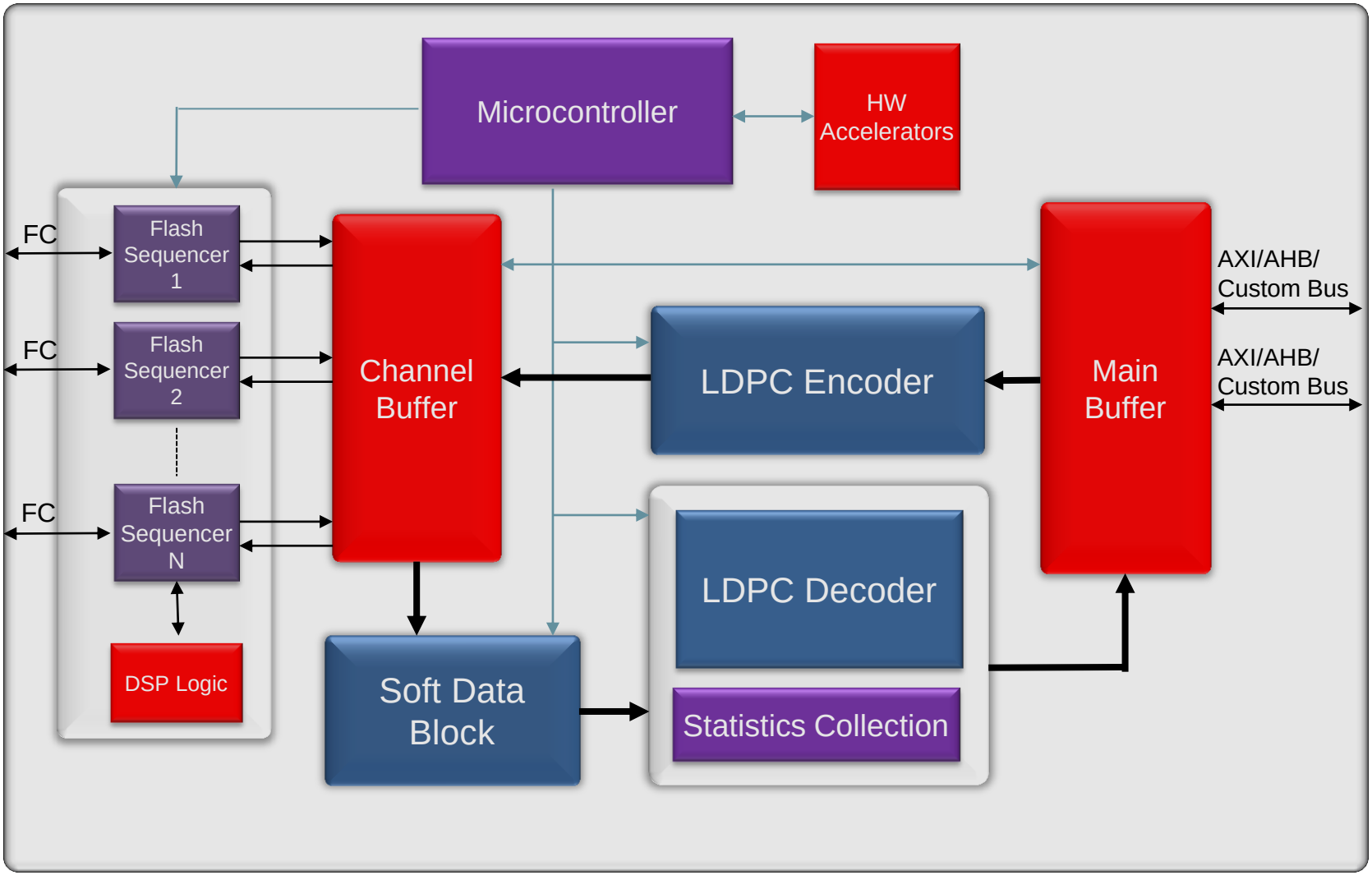
FLASHPRO MEDIA MANAGAER BLOCK DIAGRAM

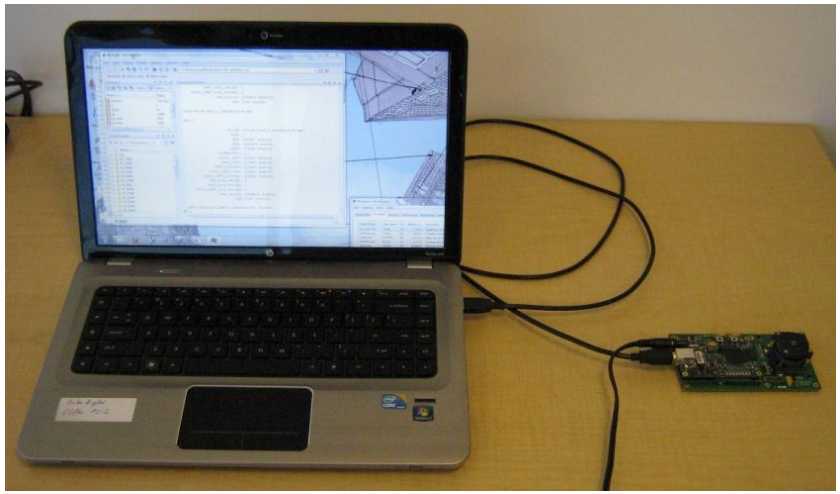


FLASHPRO MEDIA MANAGER

- FLASHPRO implements a high reliable media manager for FLASH Controllers
  - Advanced data management
  - LDPC Decoder and Encoder optimized for FLASH applications
  - Statistical Digital Signal Processing (S-DSP)
- Flexible data-rate for encoder and decoder
  - Supports up to 4 GB/s per instance
- Standard or custom high speed interfaces for host side
  - Custom DMA bus or ARM AXI/AHB is supported for easier integration
- Reliability firmware runs on a local processor

FLASHPRO REFERENCE DESIGN SYSTEM

- Complete reference design for FlashPRO Reliability System Solution



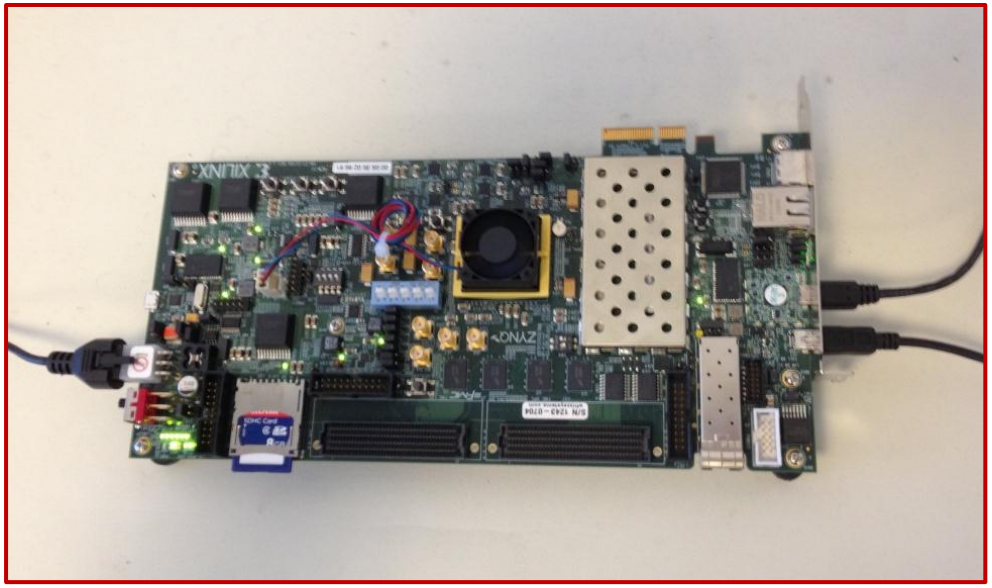
BGA-152

BGA-132

TSOP-48

LDPC AND ERROR FLOOR

- Error Floor: With very low probability LDPC codes can fail even at high SNR
- Error floor should be analyzed to guarantee unrecoverable error rate
- FLASHPRO based Error Floor System allows analyzing error floor below 10^{-15} bits
  - Guarantees system has no error floor below 10^{-15}
  - Implementation is based on ZYNQ ZC706



LDPC DECODER IMPLEMENTATION EXAMPLES

IP	Freq (MHz)	Throughput (GByte/s)	Cell Area (sq mm)	Memory (KByte)	Gates Total Power (mW)	Gates Total Power (mW)
					Beginning-of-Life	End-of-Life
Consumer	500	0.38	0.026	15.9	13	33
Enterprise	800	4.31	0.197	17.7	127	328

- Lowest power LDPC decoder
- TSMC 28nm HPM technology
  - Implementation is based on 8 metal layer (8LM6X1ZUTRDL)
  - Only HVT cells are used
  - Timing is closed for SS corner, 0.81V, and 125C
- Codeword size is 1KB
- Total power is measured at TT, 0.9V, 25C

CONCLUSION

- There are three major components to increase Flash reliability
  - Data Management
  - Error Correction Codes
  - Statistical Digital Signal Processing
- Best Error Correction Codes can operate close to Shannon limit
  - LDPC together with S-DSP will work close to Shannon limit
- Communication Standards requirements for LDPC Codes are significantly different from Flash systems
- FLASHPRO implements a complete flash reliability solution
  - Lowest area and power
  - Implementation available on ASIC, FPGA, Structured ASIC

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THANK YOU