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Designing a Configurable NVM Express Controller/Subsystem

Amit Saxena, VP, Engineering

"The IP enabled solutions provider"

AGENDA

- Company Overview
- NVMe SSDC Subsystem
- NVMe Features & Configurability
- Configurable IP Components
- Summary

The Mobiveil Team

- **Leadership**
  - Management with 25+ years experience in Semiconductor/Silicon IP/Systems software
  - Previously founded GDA Technologies, Inc and grew to strong IP and Services group , 500+ engineers strong.

Key differentiators

Developed several highly configurable key high speed IP blocks in the last 10+ years (PCI Express, Hyper Transport, Serial RapidIO, SPI4.2, DDR4/3,Flash Controllers etc)

Locations

Headquarters in Milpitas, CA
India design centers: Chennai & Bangalore
Sales: Offices/Reps worldwide

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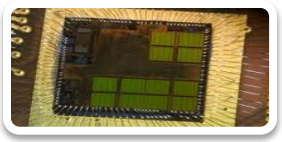
Mobiveil IP Advantages



Market leading & most exhaustively proven cores in the market: *Industry leaders are using these cores*

Consortium Participation : *RIO – Member, PCISIG – Member, HMC - Member*

Superior Technical Solution: *Most Feature rich IP, Complete Customization and delivery Solution*

Support: *Clear IP Focus & Worldwide Support*

3rd Party Partnerships for complete Solution: *(Verification and PHY IPs)*

Standard Body Certified Cores: *All Mobiveil IPs are validated and certified: PCI Plug fest, UNH, RTA*

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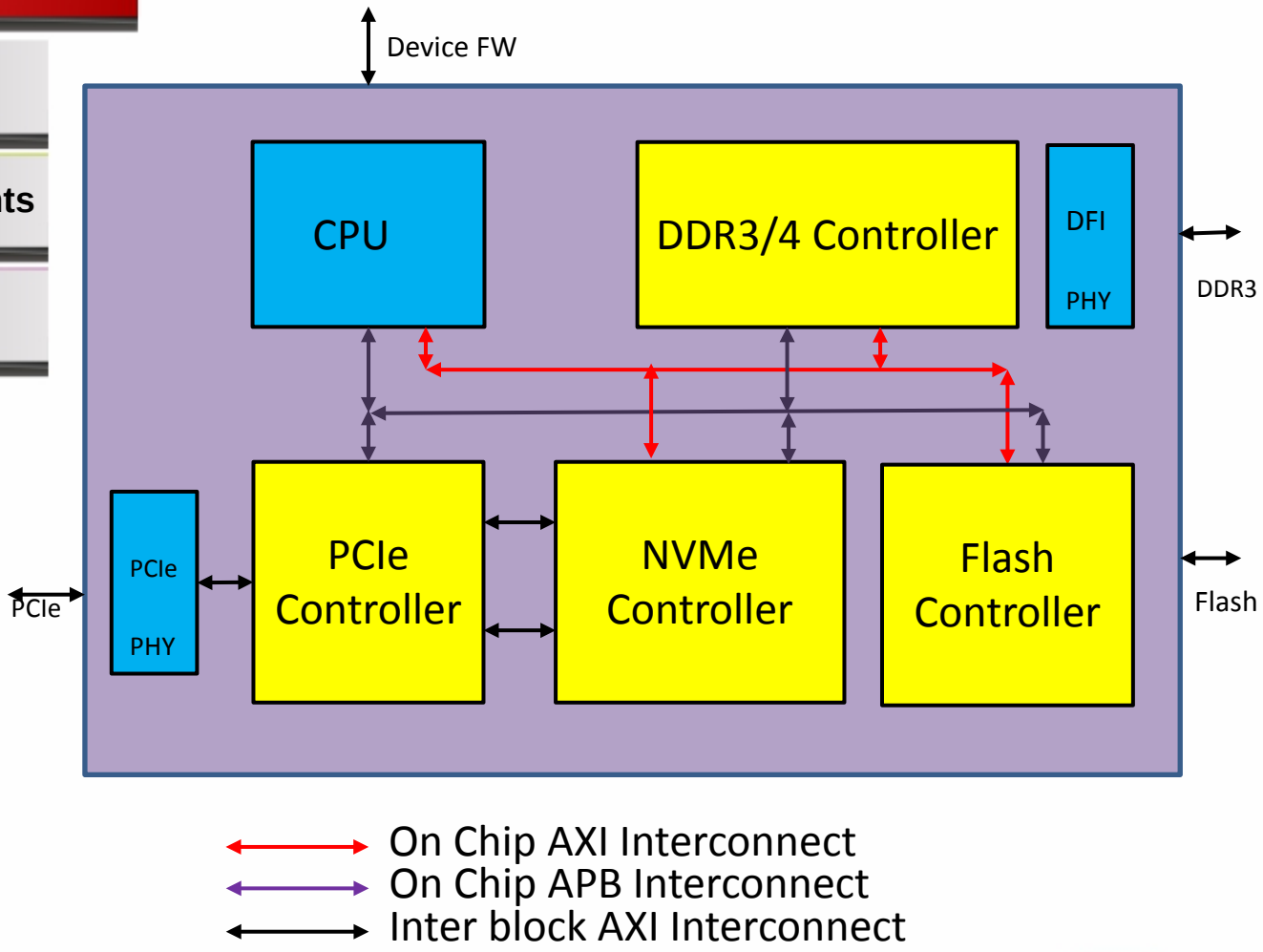
NVMe SSDC Subsystem

NVMe SSDC Subsystem



NVMe - Features

- A Register level interface that allows host software to communicate with a non-volatile memory subsystem
- Defines a standard command set for use with the NVM subsystem
- Optimized for Enterprise and Client solid state drives, typically
- attached to the PCI Express interface
- Defines Pair of Submission and Completion IO Queues
- Defines parallel operation by supporting up to 64K I/O Queues with up to 64K commands per I/O Queue.
- Defines many Enterprise capabilities like end-to-end data protection, enhanced error reporting, and virtualization
- Supports differentiated services, i.e., different qualities of service (QoS)Targets
- Supports Multi-Path IO and Namespace Sharing capabilities
- Supports Reservations
- Supports multiple name spaces

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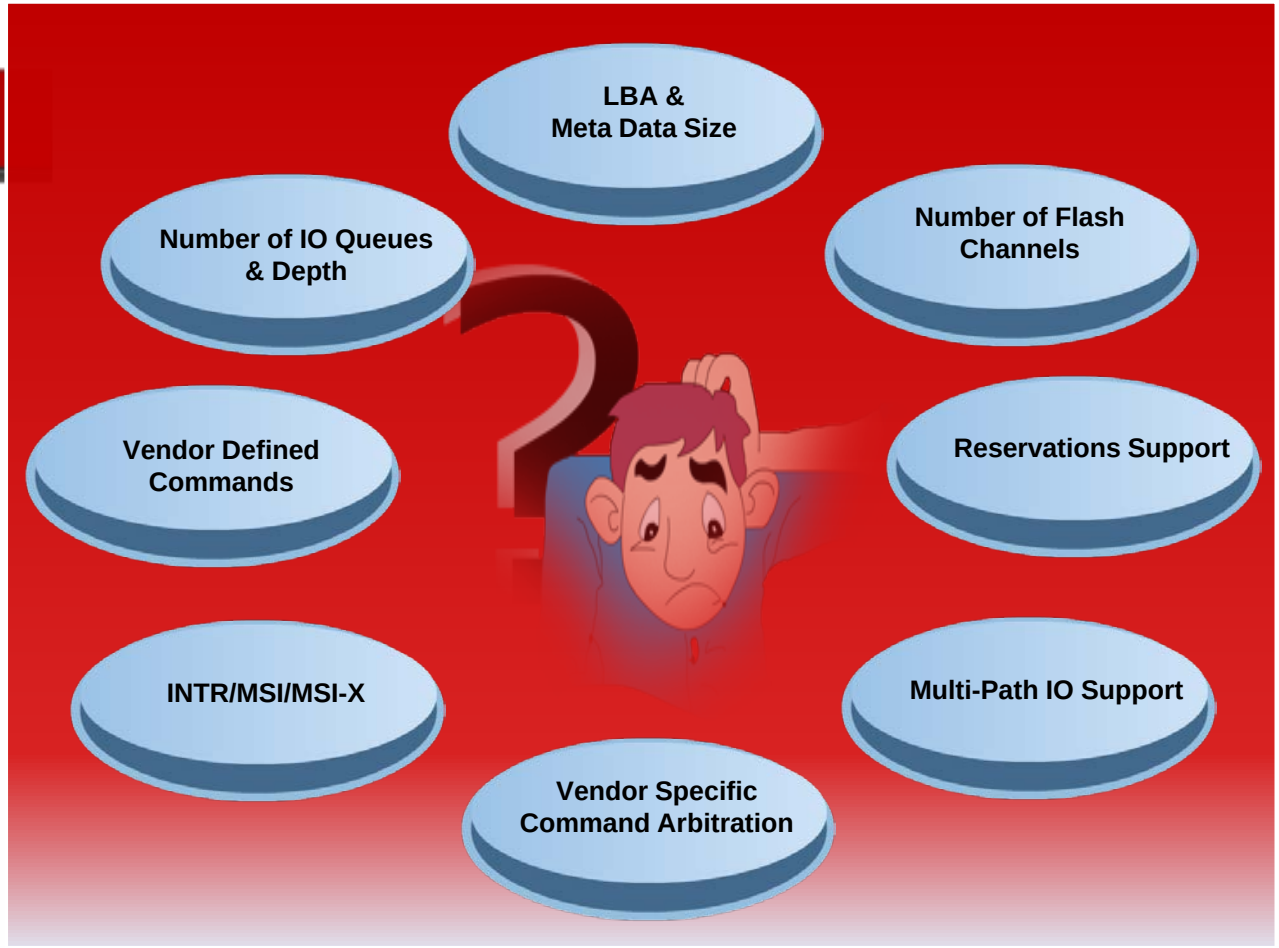
NVMe Configurability



nvm EXPRESS

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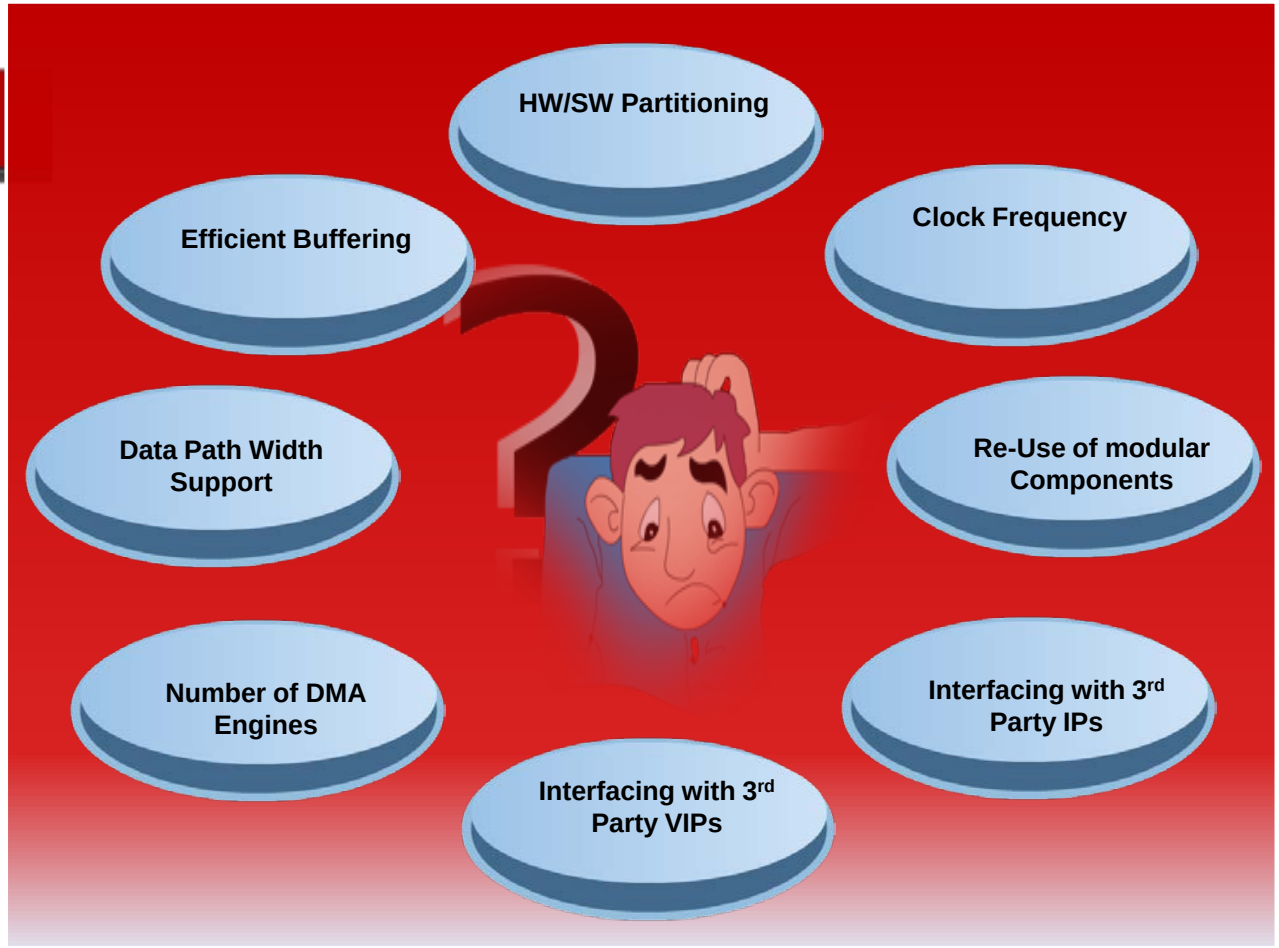
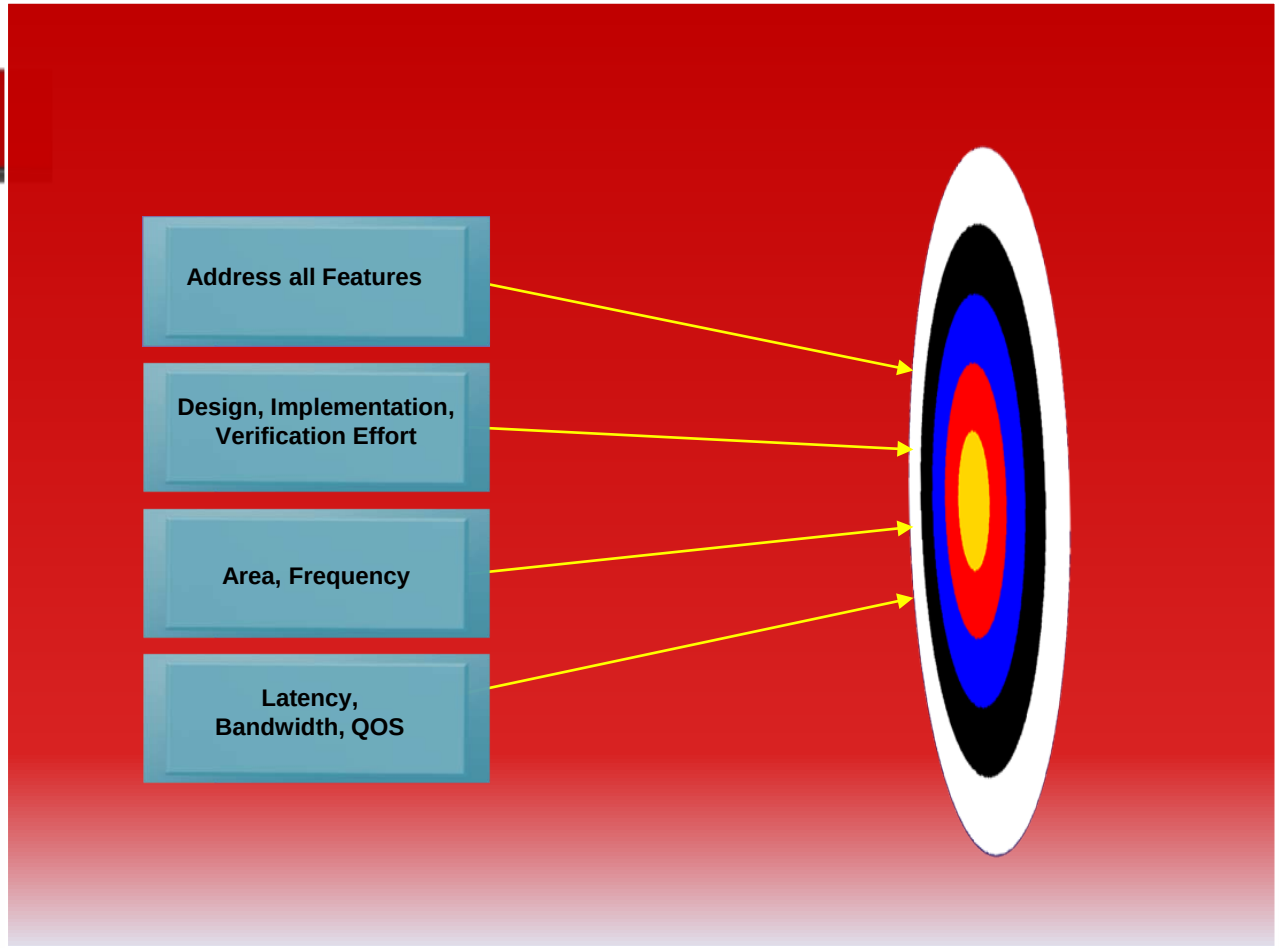
NVMe Configurability



Configurable NVMe Controller



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Configurable IP Components

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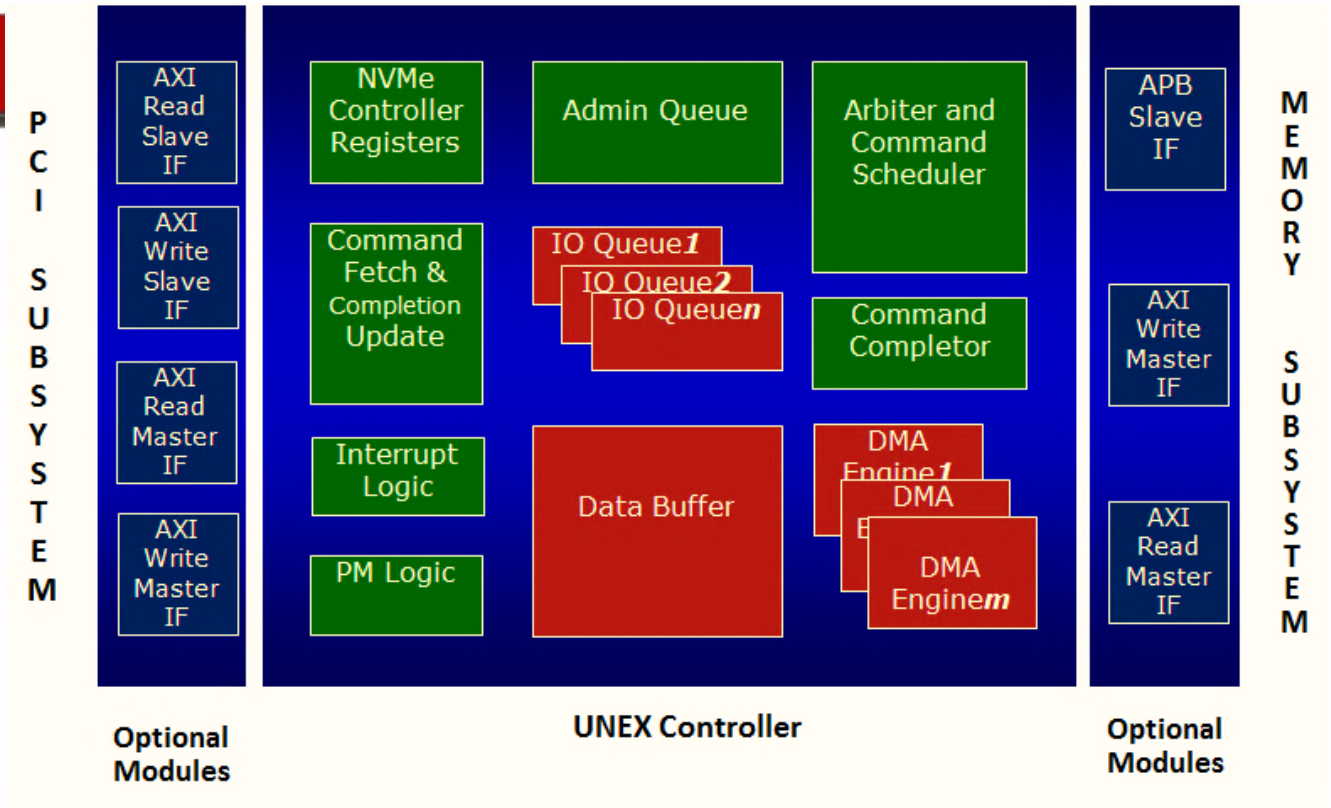
NVM Express Controller (UNEX)

NVM Express (UNEX) Controller

- ✓ Highly Configurable
- ✓ Technology Independent



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UNEX Features

- Compliant to NVM Express 1.1 specification
- Supports configurable number of IO Queues
- Supports configurable Queue depth
- Supports Round Robin or Weighted Round Robin with Urgent Priority arbitration mechanism
- Host memory page size support of 128MB
- Efficient and Streamlined Command handling
- Supports Fused Operations
- Supports All Optional Admin Commands
- Supports All Optional NVM Commands
- Supports Multi-Path IO and Namespace Sharing capabilities
- Supports Reservations
- Supports multiple name spaces
- Optional AXI interfaces for NVMe implementation in SoC
- Well defined Command Interface for local CPU to perform subsystem initialization and to handle all non-hardware accelerated commands
- Targets FPGA, Structured ASIC and Standard Cell technologies

✓ **Highly Configurable**
✓ **Technology Independent**

nvm EXPRESS

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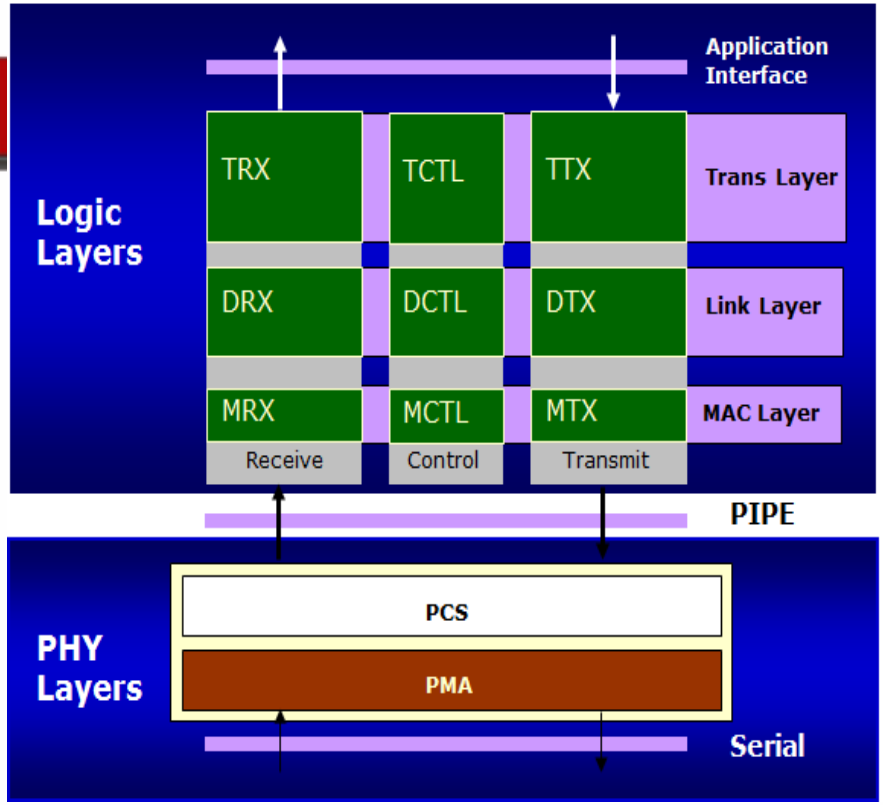
PCI Express Controller (GPEX)

PCI Express (GPEX)

- ✓ Highly Configurable
- ✓ Technology Independent
- ✓ System Validated



PCI EXPRESS™

Gen1, Gen2 & Gen3
Endpoint
Root Complex
Dual mode
Switch port
Switch
OCB Solution

x1 to x32
180nm to 28nm

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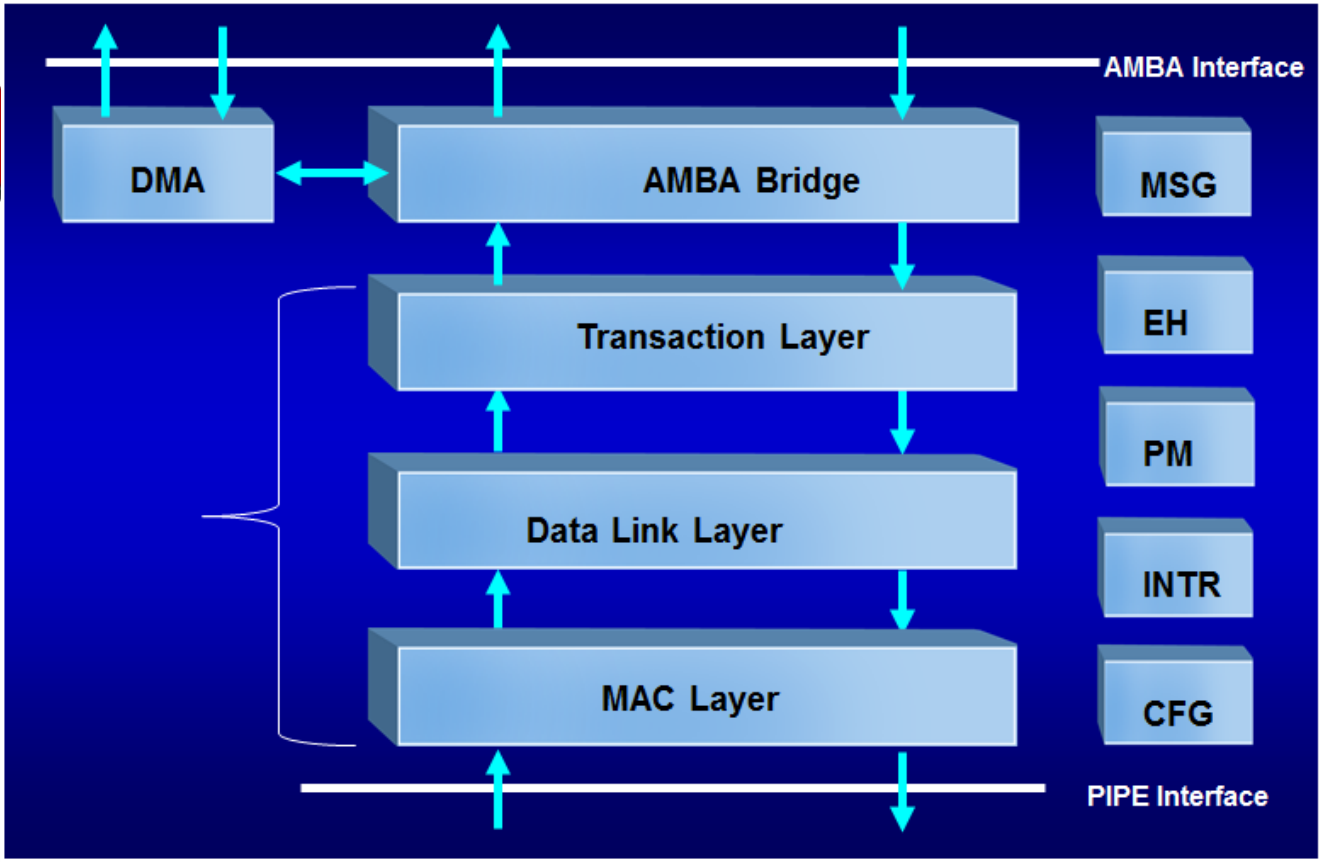
PCIe-AMBA Bridge

- ✓ Highly Configurable
- ✓ Technology Independent
- ✓ System Validated

PCI EXPRESS™



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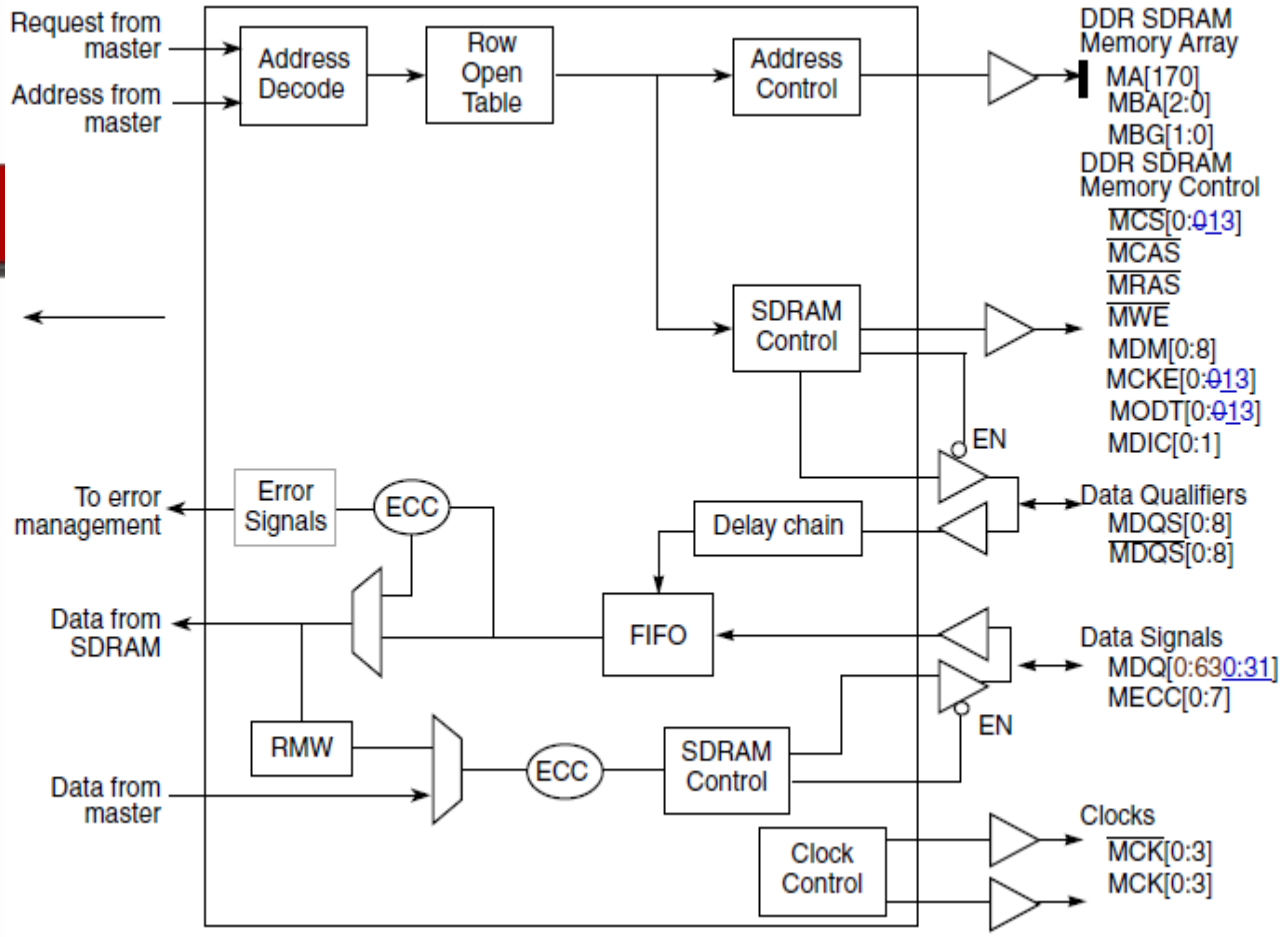
DDR3/4 Memory Controller

DDR3/4 Memory Controller

- ✓ **Highly Configurable**
- ✓ **Technology Independent**

Silicon Proven



- ✓ Highly Configurable
- ✓ Technology Independent

Silicon Proven

DDR3/4 Controller Features

- Support for DDR3 and DDR4 SDRAM
- 64-/72-bit SDRAM data bus, 32-/40-bit SDRAM, 16-/24-bit SDRAM
- Supports Chip select interleaving
- Supports Partial array self refresh
- Support for data mask signals and read-modify-write for sub-double-word writes
- Support for double-bit error detection and single-bit error correction ECC (8-bit check word across 64-bit data)
- Open page management (dedicated entry for each logical bank)
- Automatic DRAM initialization sequence or software-controlled initialization sequence
- Write leveling supported for DDR3 memories
- Support for up to eight posted refreshes

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Integrated Flash Controller

Integrated Flash Controller

- ✓ **Highly Configurable**
- ✓ **Technology Independent**

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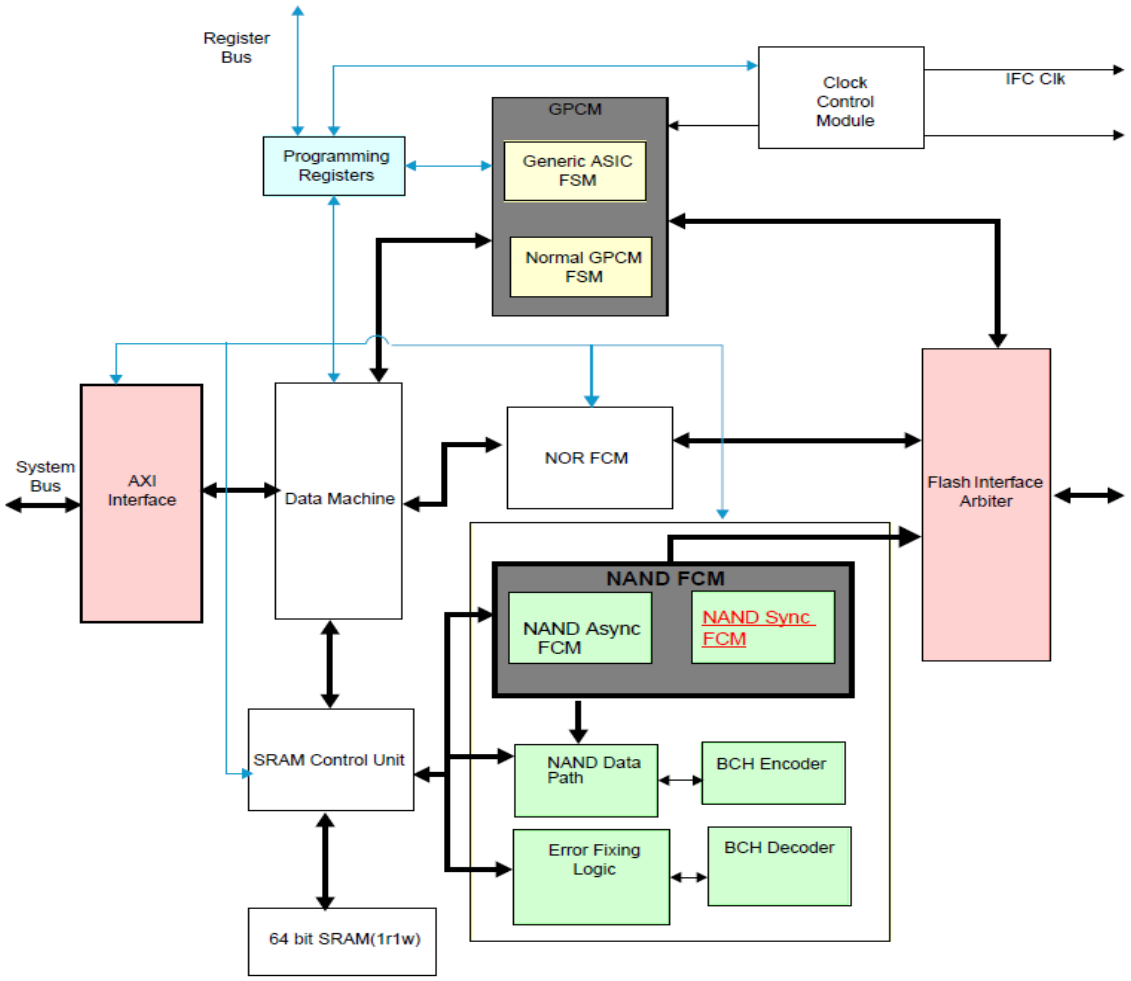

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Integrated Flash Controller Features

- Flash Controller with eight chip selects
- AXI V1.0 Slave Interface
- Separate Bus Interface for register access
- Support for error and debug registers
- Supports NAND, NOR and GPCM (SRAM and ROM) devices
- Support memory banks of size 64KByte to 4 GBytes
- Write protection capability (only for NAND and NOR)
- Provision of Software Reset
- NAND Flash Features
  - x8/ x16 NAND Flash Interface
  - Support for ONFI-2.2 Asynchronous interface (8/16 Bit)/Source Synchronous interface (8 bit) and mandatory commands.
  - BCH code for 4 bit & 8 bit Error correction per sector of 512 bytes (Using GF-2^13 Galois field) and 24 & 40 bit ECC per sector of 1K bytes (Using GF- 2^14 Galois field)
  - Optional ECC generation and checking
  - Flexible timing control to allow interfacing with proprietary NAND devices
  - SLC and MLC Flash devices support with configurable page sizes of up to 8KB

✓ Highly Configurable
✓ Technology Independent

Silicon Proven

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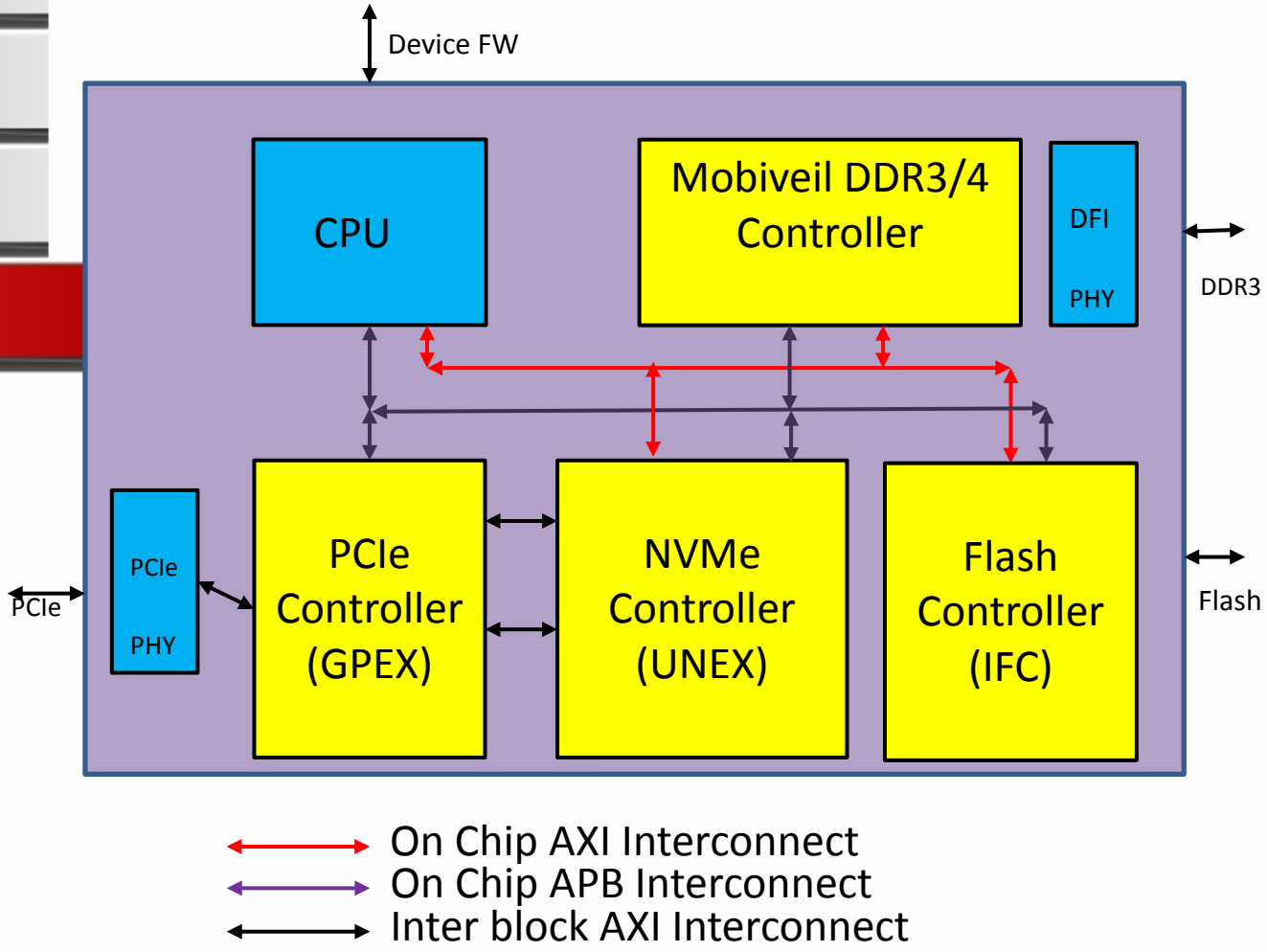
Mobiveil NVMe SSDC Subsystem



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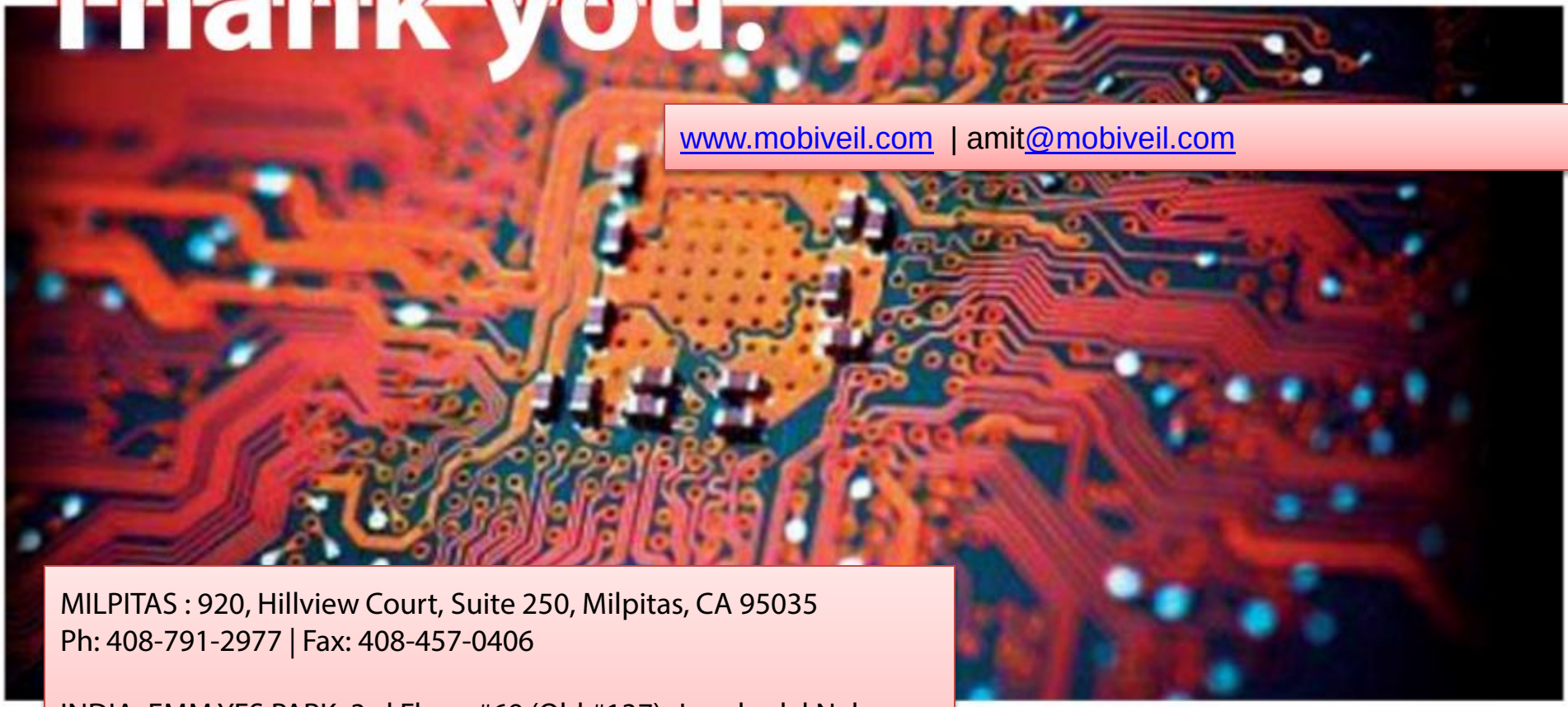

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