PCIe Storage Performance Testing Challenge

Tien Pham

SSD Applications Manager

Advantest America, Inc.

Outline

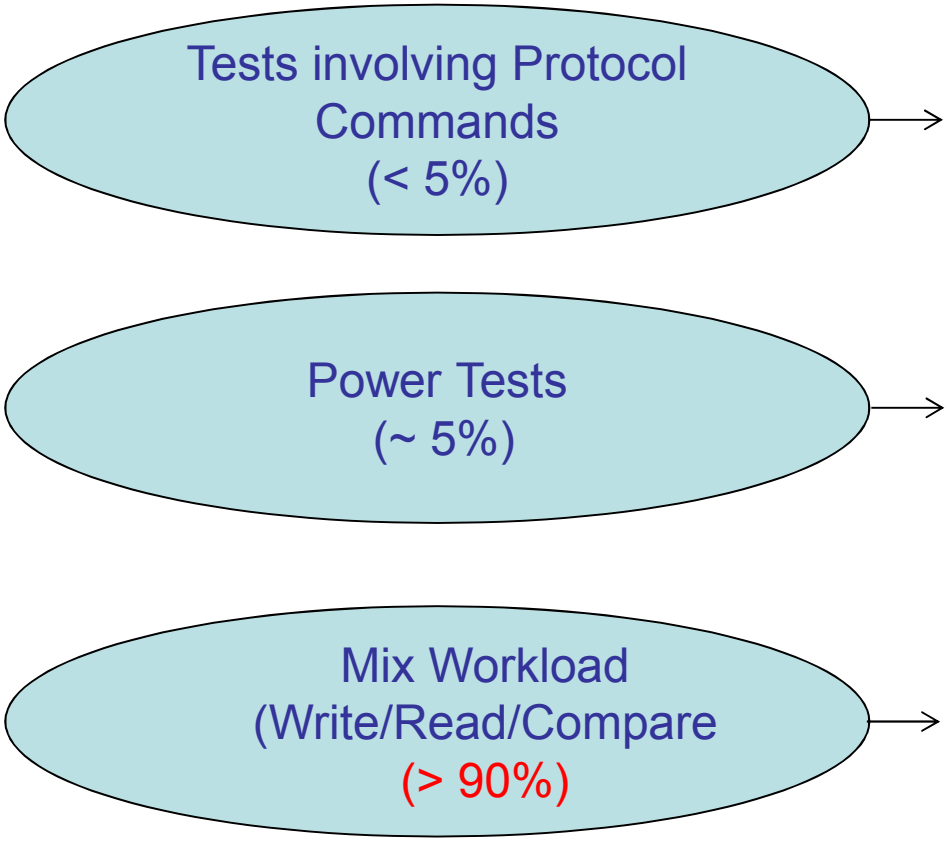
- PCIe Storage Test Challenges
- PCIe Storage Production Test Items And Bottlenecks
- Proposed Solution
- Characterization Results
- Proposed Solution Advantages

PCIe Storage Test Challenges

- Exercise PCIe DUT (Device Under Test) at device's full bandwidth. "Device limited testing vs. tester limited"
- Increased Controller and Firmware complexity prone to marginal errors and stability issues especially at full speed
- Maintaining Signal Integrity with multi-lane PCIe Gen 3 connection

  (See Eric Kushnick, Session 203-C FMS'13: "Is Your Tester Ready for PCIe Gen 3.0?")
- DUT Isolation, when tester resources are shared with multiple SSDs
- Multiple competing Host Controller Interface (HCI) and Connector standards

PCIe Storage Production Test Items And Bottlenecks.

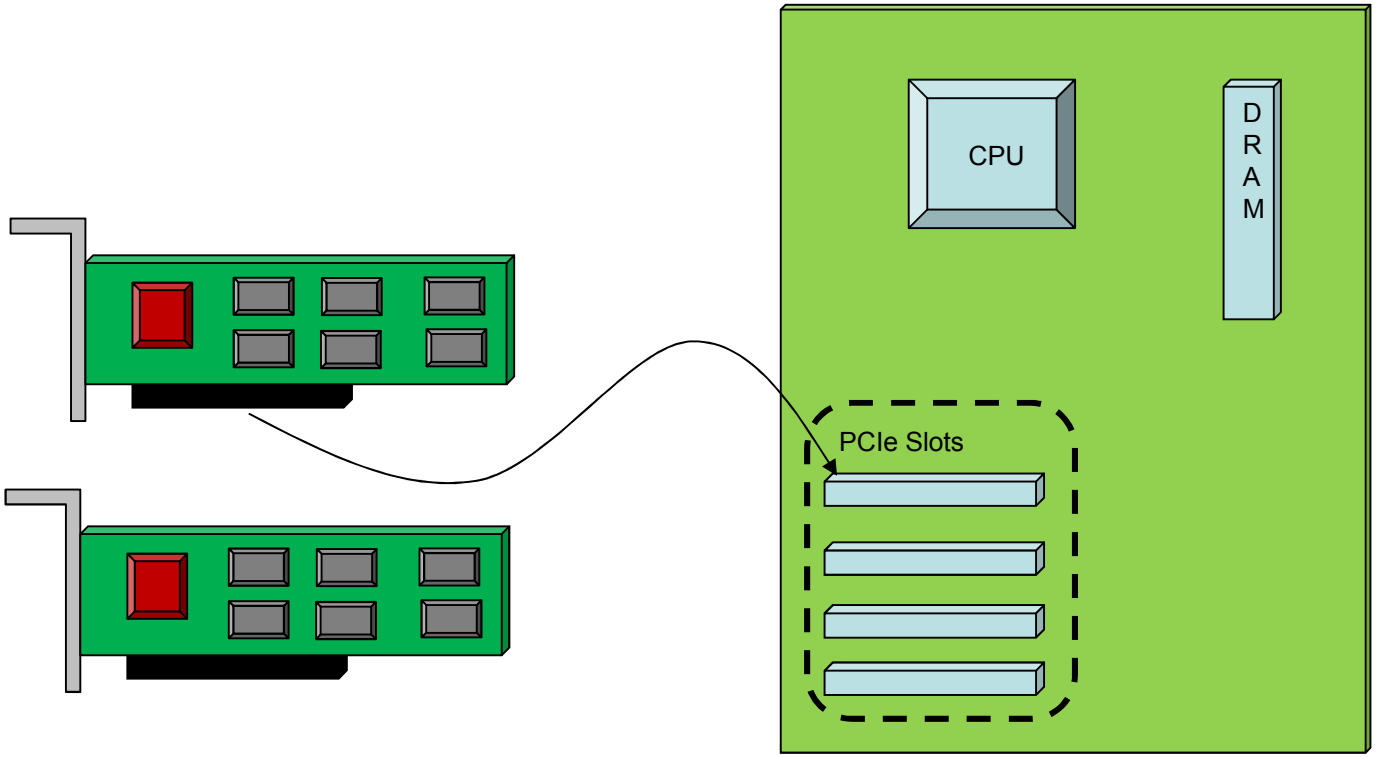


- Download Firmware
- Get Device ID / Namespace / Smart Log
- Vendor Unique commands

- Set power management mode
- Measure current/voltage
- Unplanned power shutoff during write

- Test Memory / Controller
  - Speed matters! Need to test device at speed, to fully exercise controller / memory / thermals
- Test the way user exercises device for target application (JEDEC workload, block size mix, trace based)
- Write/Read/Compare X amount of device overall capacity

PC based PCIe Storage Test Solution



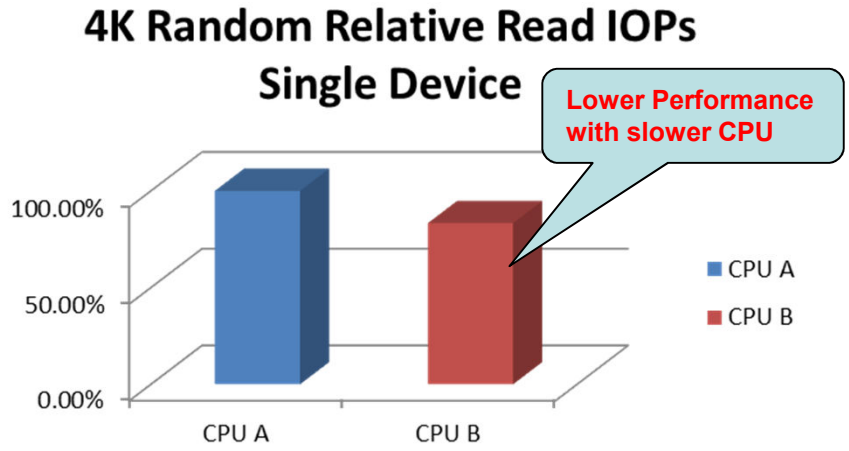
Bottlenecks Considerations - CPU Utilization

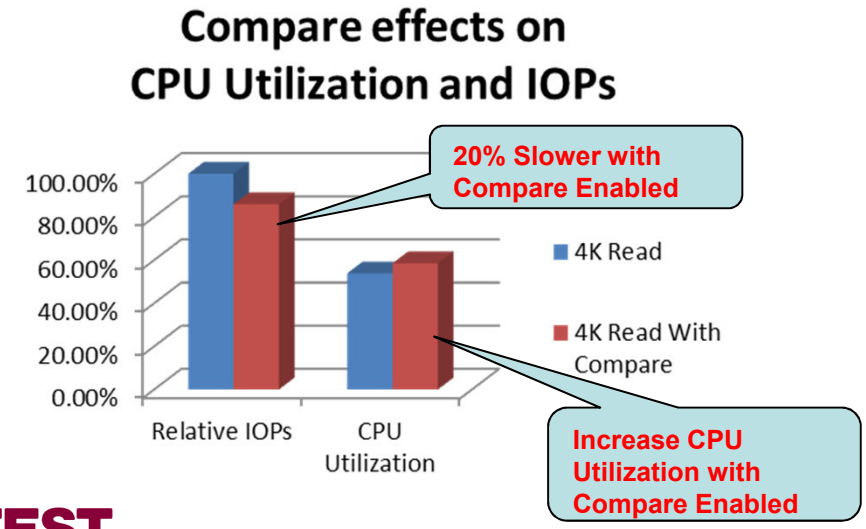
PCIe Device Performance depends on CPU

⇒Slower CPU results in slower performance

⇒Read and Compare data required additional CPU loading, resulting in slower performance

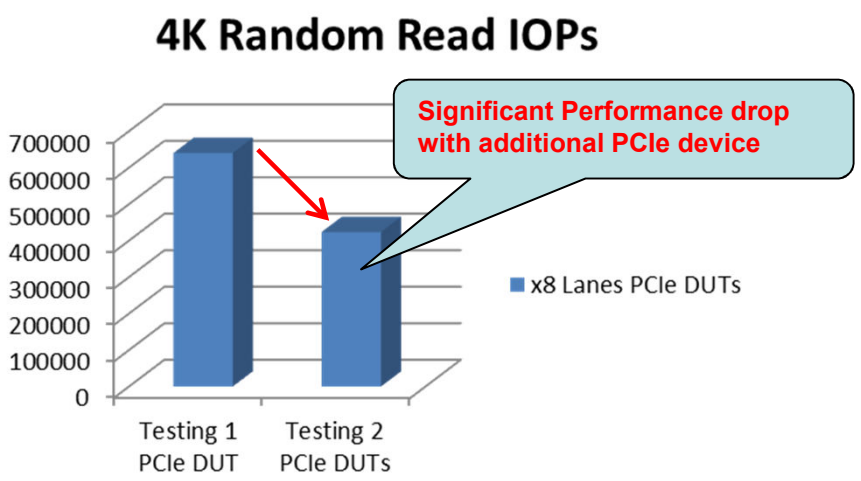
Setup: *3.7GHz i7 quad core*
PCIe 2.0 host interface
Windows Server with Iometer

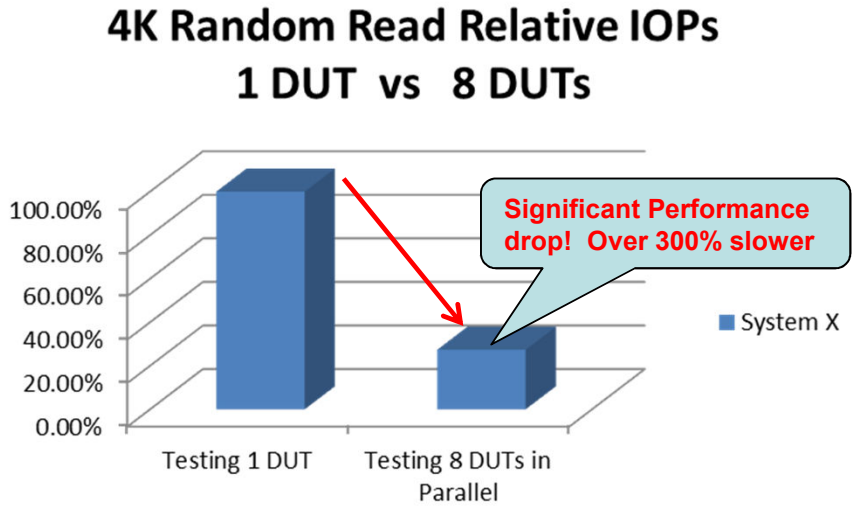




Bottleneck Considerations - Increase in Parallelism

- PCIe Device Performance depends on # of devices tested in parallel
  => More sharing of CPU or of PCIe bus results in slower performance (i.e. longer test time)





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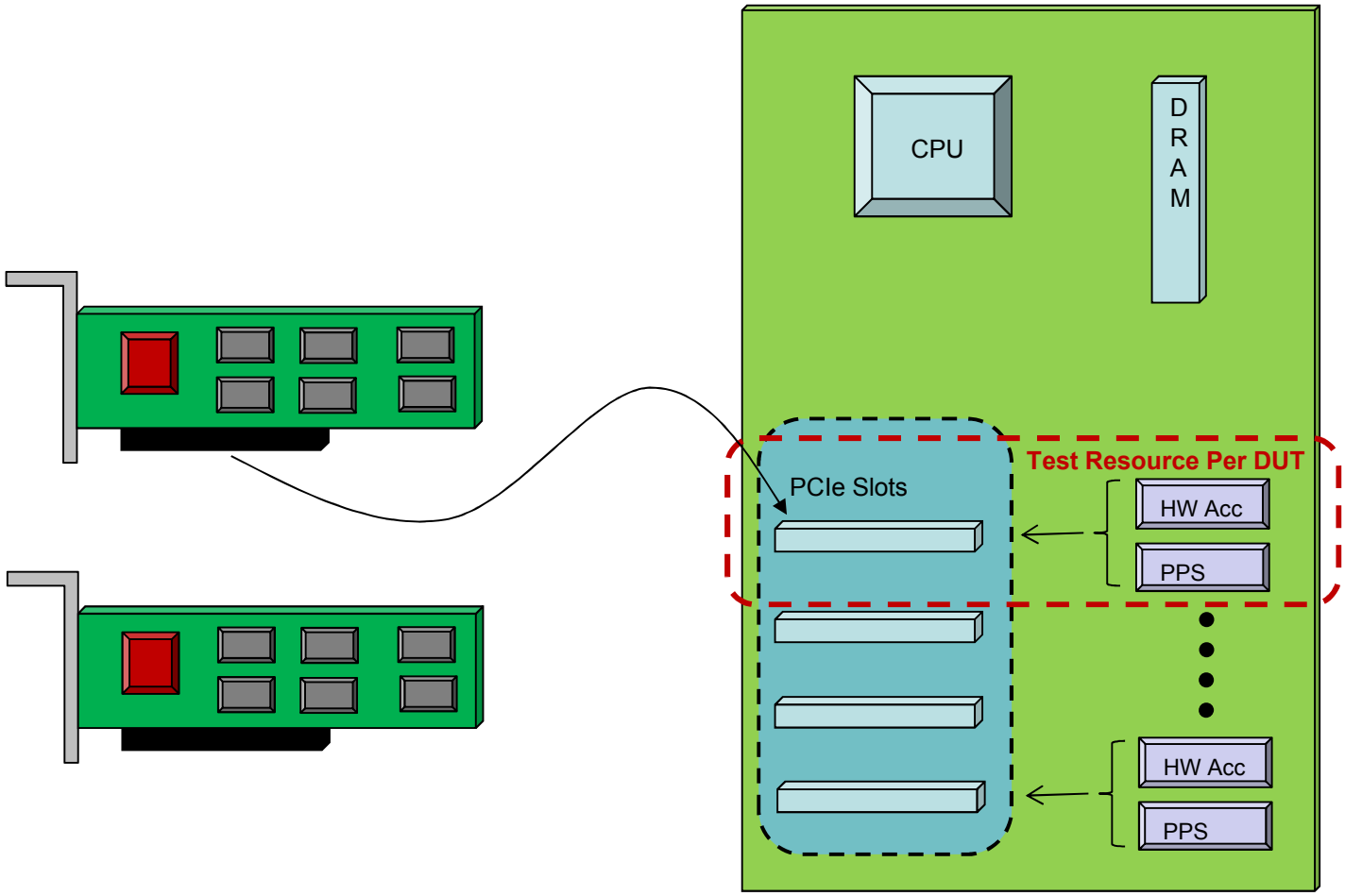
Issues with PC based PCIe Storage Test Solution

- Performance of PCIe device is limited by CPU of test system, need powerful CPU to keep up with device
- Does not scale. Testing multiple DUTs while sharing the same CPU will result in significant performance degradation and slower test time
- Stability Issues of test system when CPU utilization maxed out

Proposed Solution

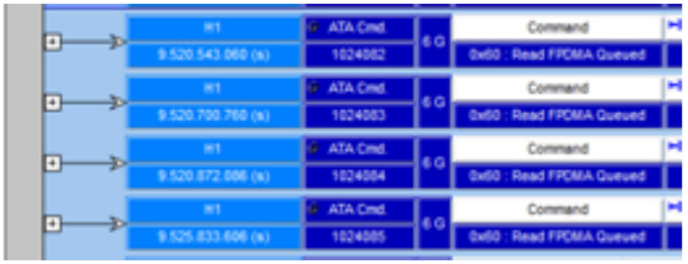
- System Architecture designed to minimize CPU dependency during heavy device workload operations (read/write/compare)
- Scalable design (minimum test time penalty with parallelism increase)
- Tester-Per-DUT architecture to minimize cross contamination between DUTs
- Flexibility to handle different standard protocol testing

Proposed PCIe Storage Test Solution

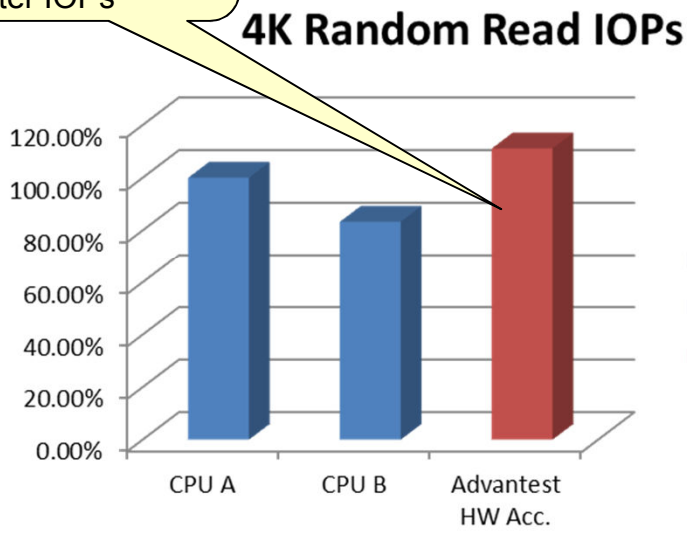


Characterization Results

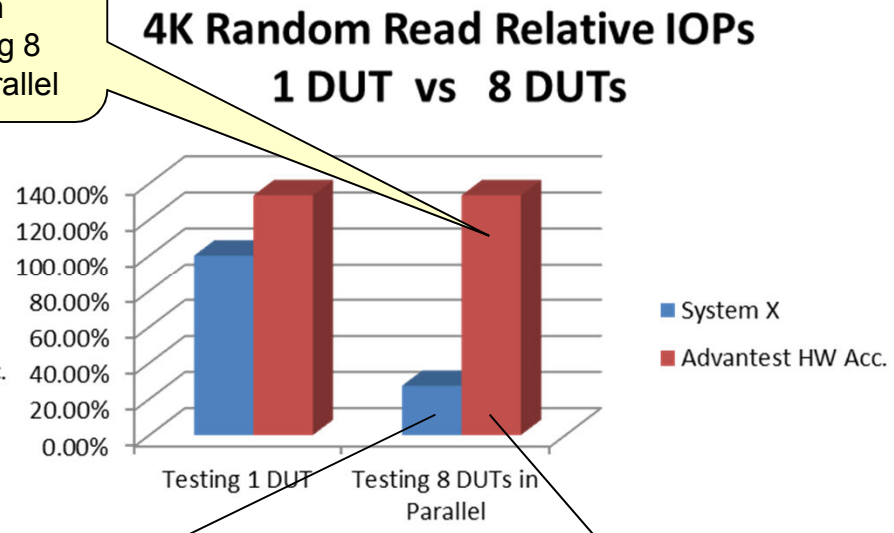
Validate data/performance using protocol analyzer

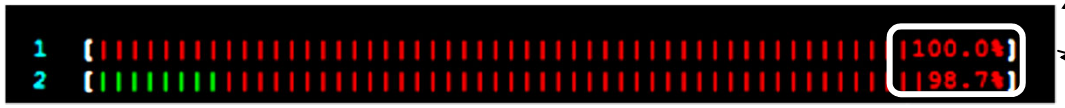


Advantest HW Acc. reduces latency, allowing better IOPs



No Performance degradation when testing 8 DUTs in parallel





Standard PC, CPU Max ed Out when testing 8 DUTs

Advantest HW Accelerator, Minimal CPU load when testing 8 DUTs

Solution Advantages

- **Improve Test Quality Through Higher Test Coverage**
  - Test more with given test time budget
  - Stress device more, when testing at speed (controller/memory interaction, thermals)
- **Improve Time to Market**
  - Detect failures earlier, through more stringent tests
  - Faster test execution
- **Higher Device Reliability**
  - Better product reputation
  - Help enhance SSD adoption
- **Improve Cost of Test**
  - Shorter production test time
  - Lower cost of retest

AT System

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