# Session 101-A: SSD Testing Challenges, Part 1 (Testing Track)

## PCIe Protocol Analysis for SSDs

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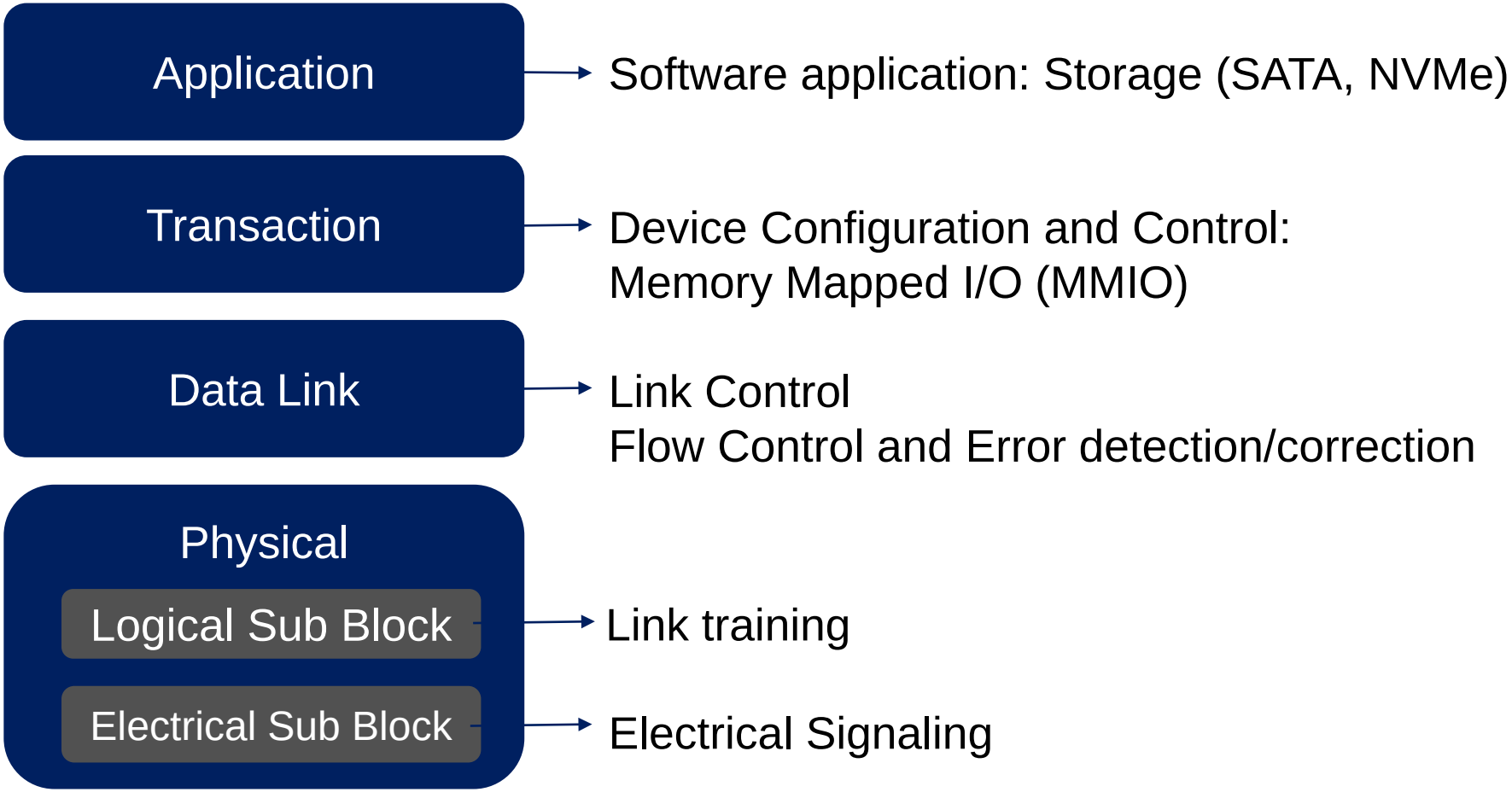
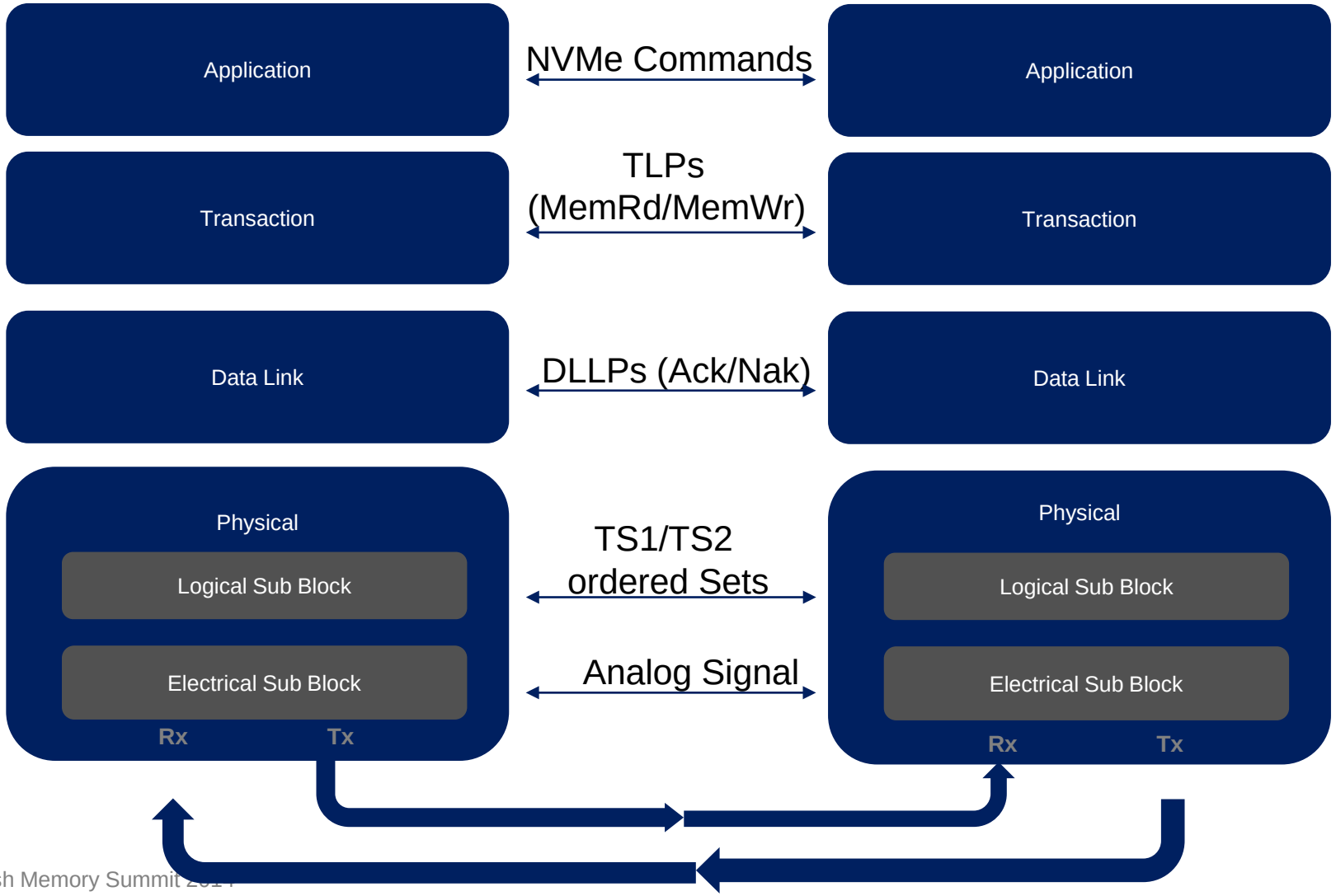
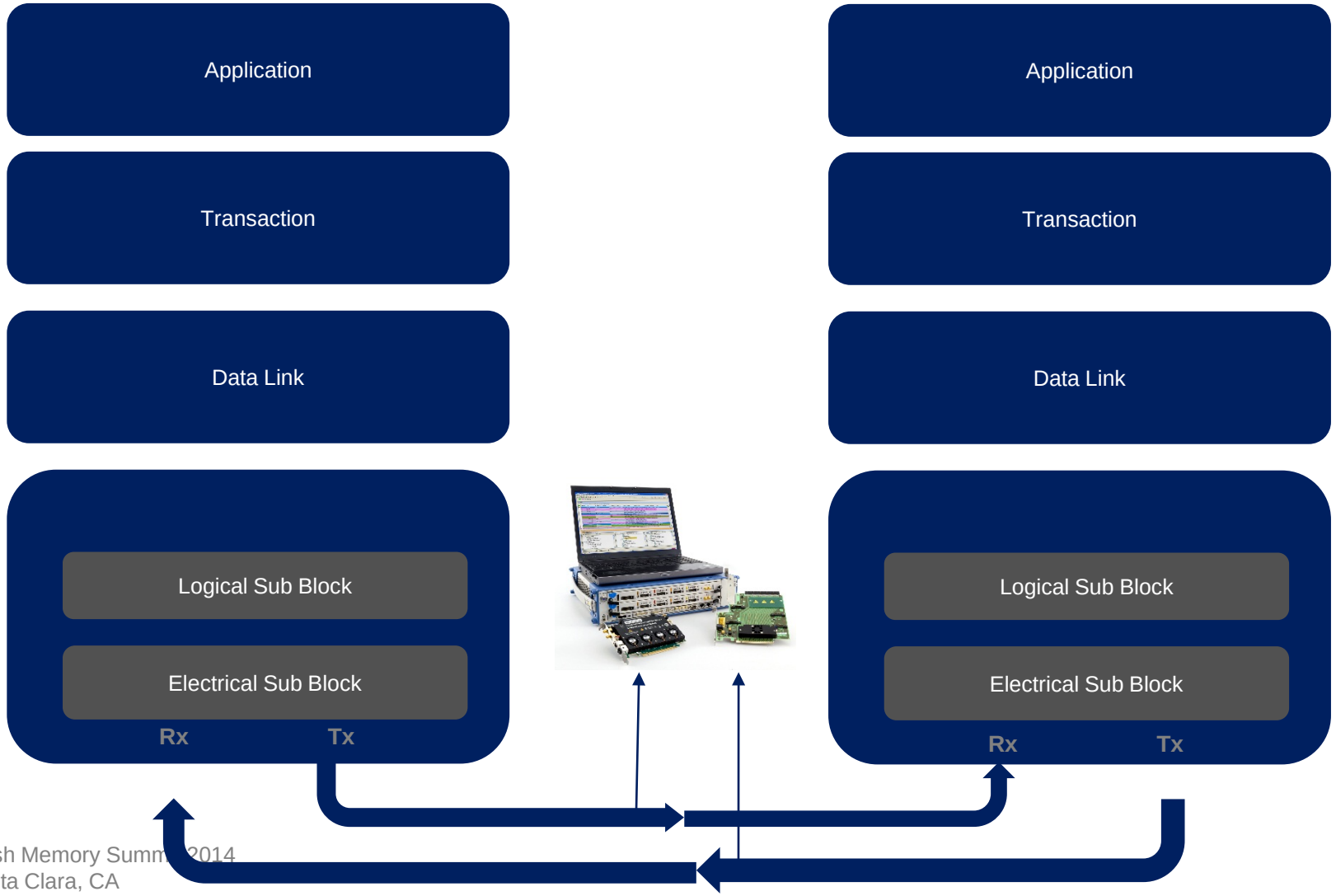
# PCI Express : Layered Protocol



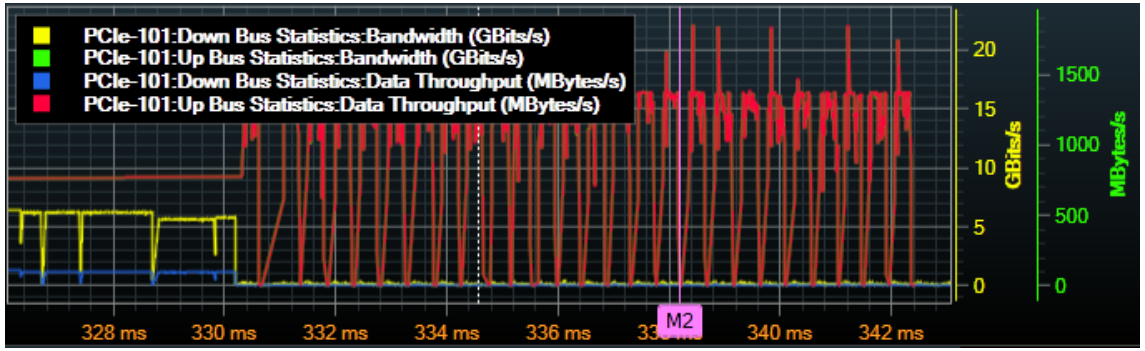
# Communication of commands



# Interposer Connection

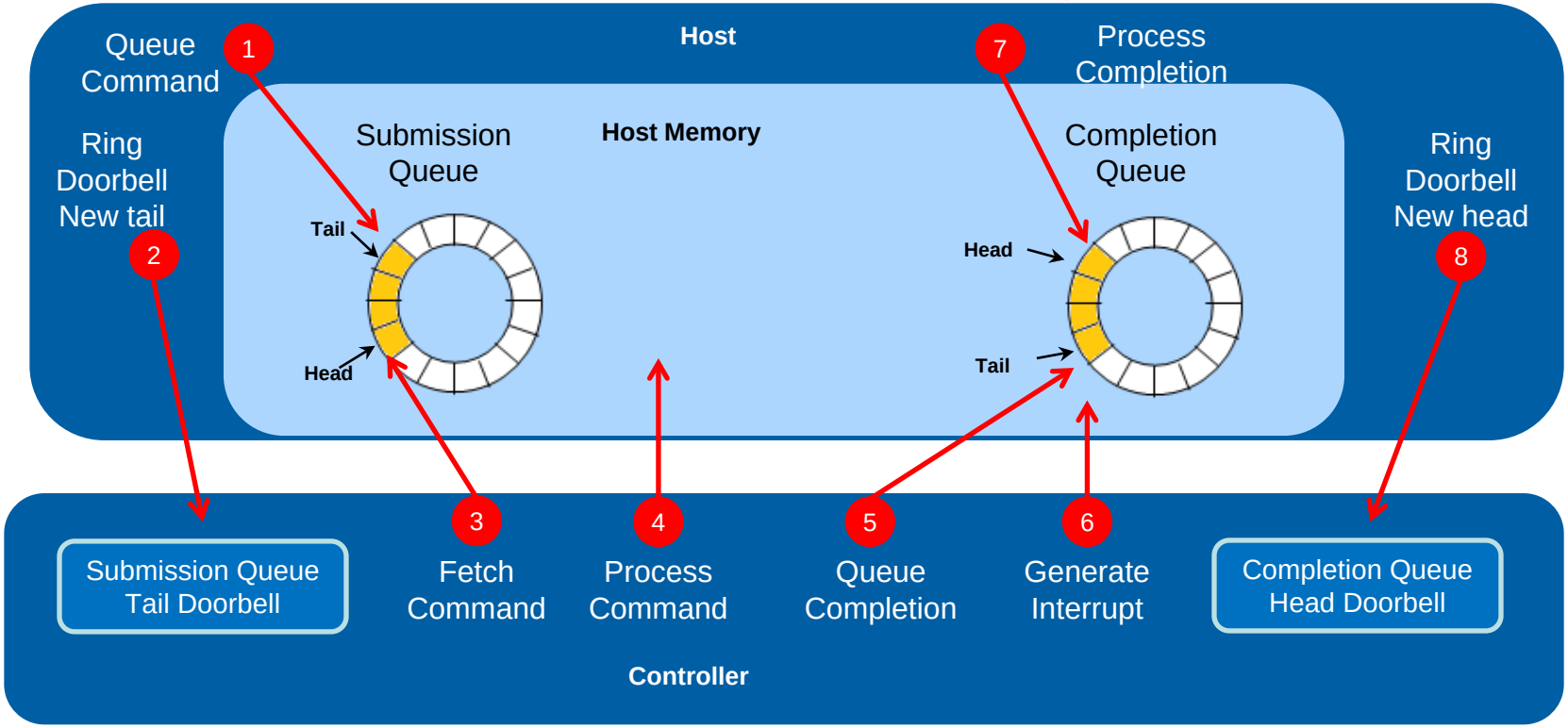


# Why PCIe Transport?




- **PCIe is high performance**
  - Lowest latency (no HBA overhead)
  - Full duplex, multiple outstanding requests
  - Scalable port width (x1 to x16)
  - Scalable link speed (2.5 /5.0 /8.0 Gb/s/per lane)
- **PCIe is low cost**
  - High volume/commodity.
  - Eliminates Host Bus Adaptor (HBA) cost
- **PCIe power management capabilities**
  - Direct attach to CPU eliminates HBA power
  - Various low power levels (L0s, L1, L2) --- New* L1 substates
- **Maturity**
  - PCIe has been shipping for years and is a mature technology.

# NVMe Queue Interface for Command Processing




**Command Submission**

1. Host writes command to submission queue
2. Host writes updated submission queue tail pointer to doorbell

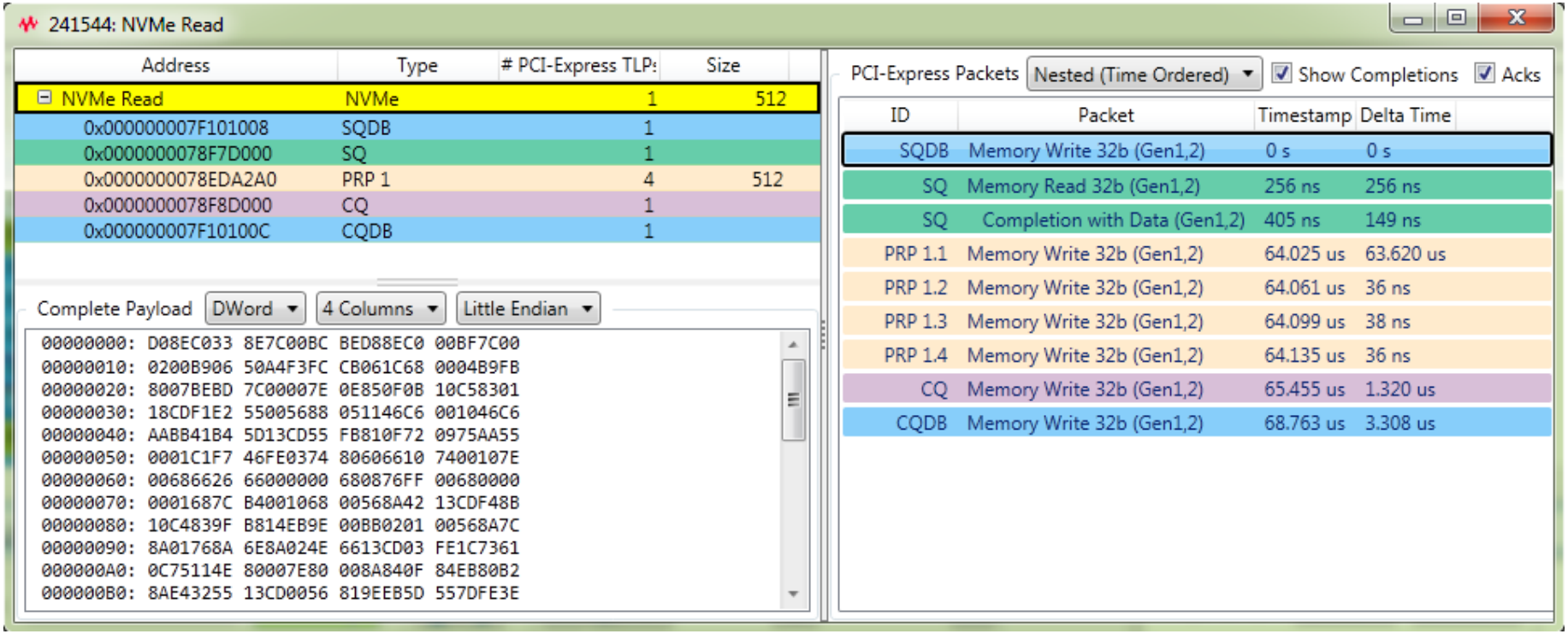
**Command Processing**

3. Controller fetches command
4. Controller processes command

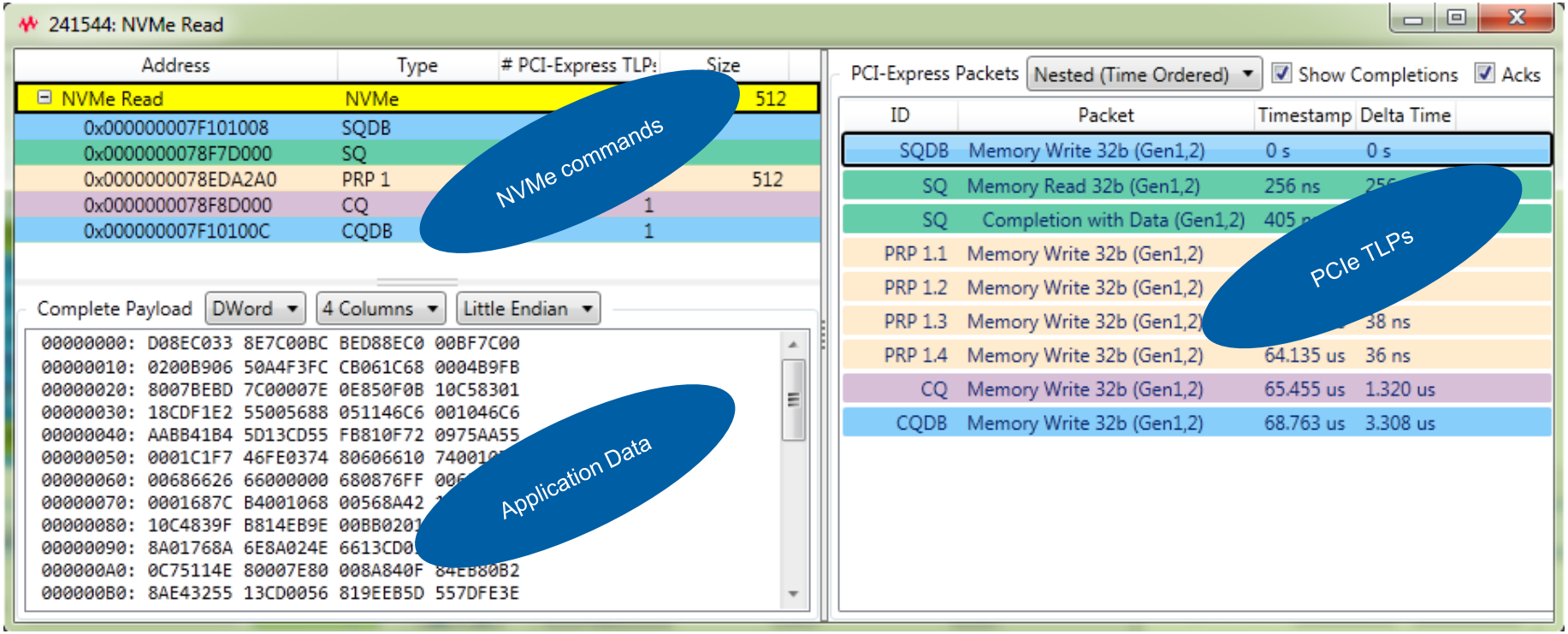
**Command Completion**

5. Controller writes completion to completion queue
6. Controller generates MSI-X interrupt
7. Host processes completion
8. Host writes updated completion queue head pointer to doorbell

# Example of a NVMe Read operation



# Example of a NVMe Read operation

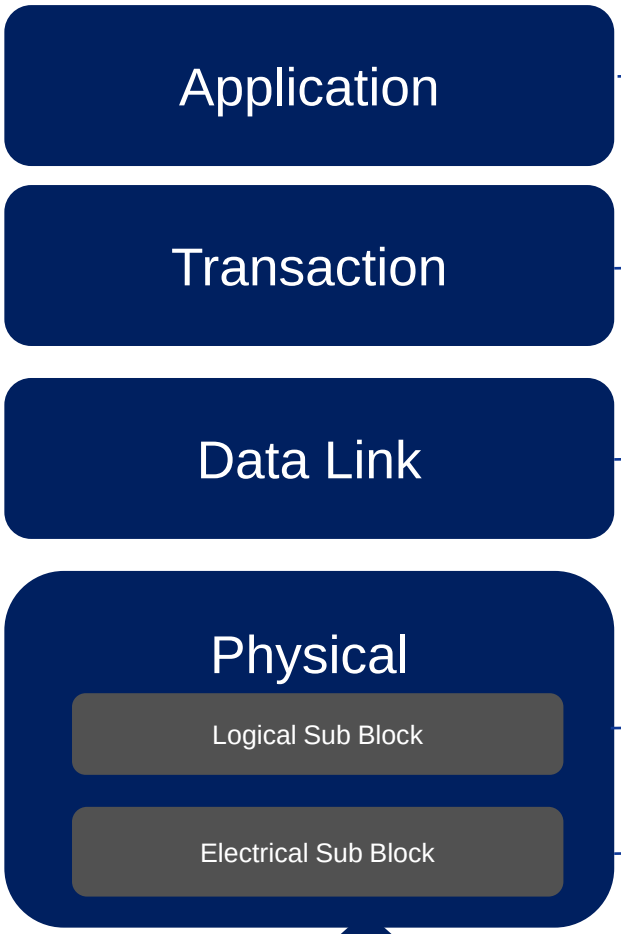


# Key PCIe tests

- **Equalization testing:** Signal quality is critical for success operation at Gen3 8GT/s
- **LTSSM analysis:** State transitions to handle link up, recovery, and power management
- **Packet capture and decode:** PCIe packets, responses, configuration and device enumeration
- **Performance Analysis:** Response times and process delays can greatly impact data throughput
- **Flow Control analysis:** Included in the performance analysis, clearly identify and track credit starvation issues.

| Sampl | Time | Downstr | Ups | Lin | Seq | T | Le | Address, Register | H | Payload |
|---|---|---|---|---|---|---|---|---|---|---|
| 245039 | 33.748789316 s | CfgRd_0 | | Gen2 | D36 | 00 | 001 | Register Number=32 | | |
| 238808 | 33.748791840 s | | CplD | Gen2 | 4DE | 00 | 001 | | | 018AE005 |
| 245040 | 33.748792416 s | CfgWr_0 | | Gen2 | D37 | 00 | 001 | Register Number=32 | | 018A00CA |
| 238809 | 33.748795151 s | | Cpl | Gen2 | 4DF | 00 | 000 | | | |
| 245041 | 33.748796444 s | MemWr_32 | | Gen2 | D38 | 00 | 001 | Address=7F10 2000 | | FEE00000 |

# Protocol Analysis of NVMe




Capture TLPs to decode NVMe Commands,
Review Queue
configuration, operation and performance

Device Configuration, memory mapping,
Data transfer

Link Control
Flow Control and Error detection/correction

LTSSM, Power management

Electrical Signaling

Interposer connection