Design Challenges Using the New Device Sleep (DevSlp) Standard

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SATA Low Power

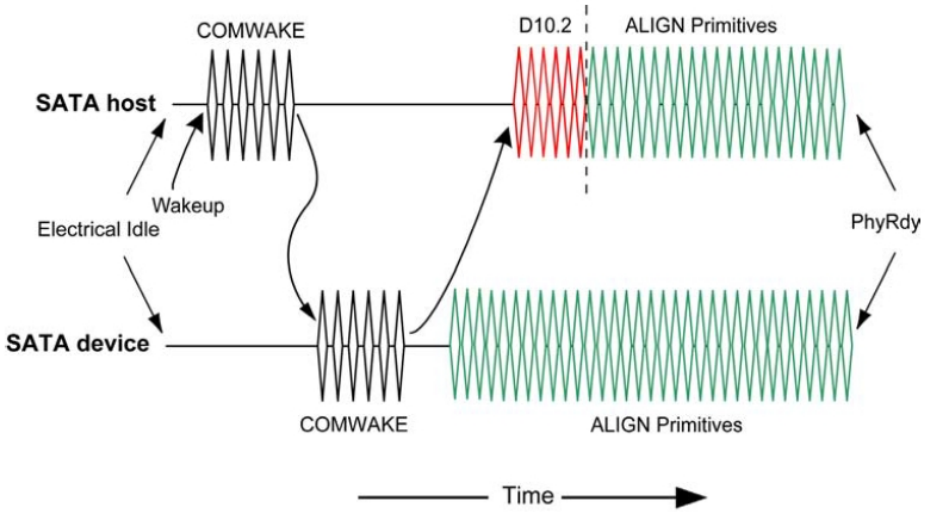
- SATA specification provides two power management modes for the SATA interface
  - Partial
    - Phy remains powered
    - Recovery time is maximum of 10 microseconds
  - Slumber
    - Phy remains powered
    - Circuits such as the clock recovery circuit can be shut down
    - Recovery time can be up to 10 milliseconds
- SATA power management can be either Host or Device initiated

SATA Power Management Entry

- Host Initiated Entry
  - HBA's upper protocol layers request that Link layer enter Partial or Slumber state.
  - SATA_PMREQ_P or SATA_PMREQ_S are generated and passed to the Physical Layer. Primitives will be generated until a SATA_PMACK or SATA_PMNACK is received
  - Physical layer transmits primitives to drive
  - Drive receives primitives and passes primitives to Link layer
  - Drive's upper protocol layers tell Link layer to accept or reject request by generating SATA_PMACK or SATA_PMNACK (min 4 max 16) and passing to the physical layer
  - Upon receipt of the PMACK or PMNACK, the host stops transmitting requests
- Drive Initiated Entry
  - Same as for the Host, but reversed

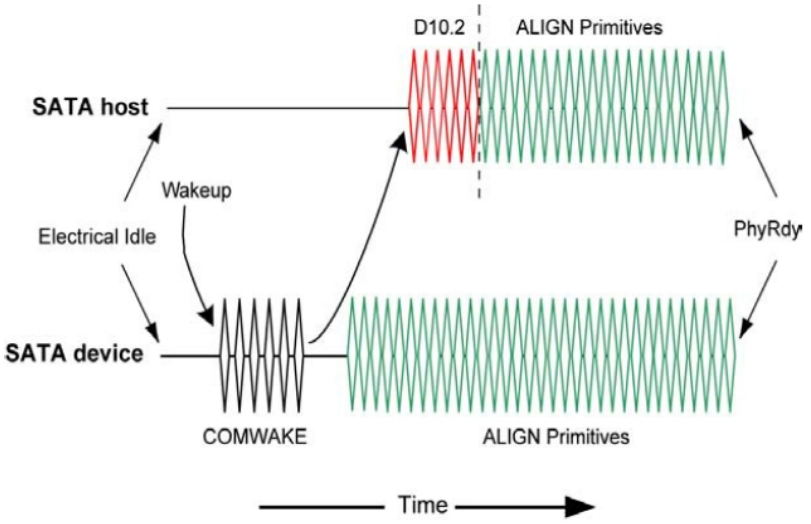
SATA Power Management Exit

- HBA Initiated Wakeup
  - HBA triggers wakeup by sending COMWAKE OOB
  - Device responds by sending COMWAKE
  - HBA Detects end of COMWAKE and transmits D10.2 values until it detects ALIGN primitives
  - HBA begins sending ALIGN
  - When the HBA and Device are both transmitting and receiving aligns the link can begin transmitting

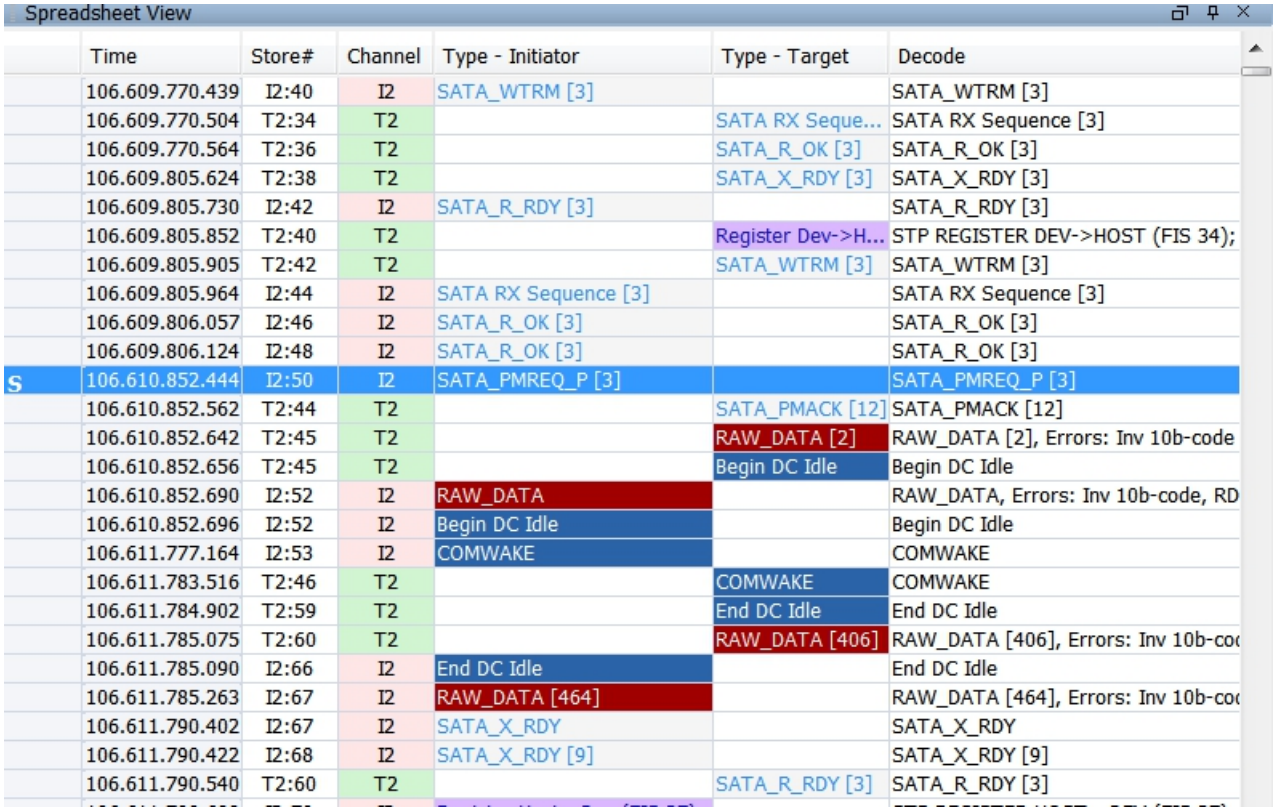


SATA Power Management Exit

- Device Initiated Wakeup
  - Device initiates wakeup by transmitting a COMWAKE followed by ALIGN primitives
  - HBA detects the COMWAKE and begins transmitting D10.2 until it detects ALIGNs
    - When the HBA and Device are both transmitting and receiving aligns the link can begin transmitting



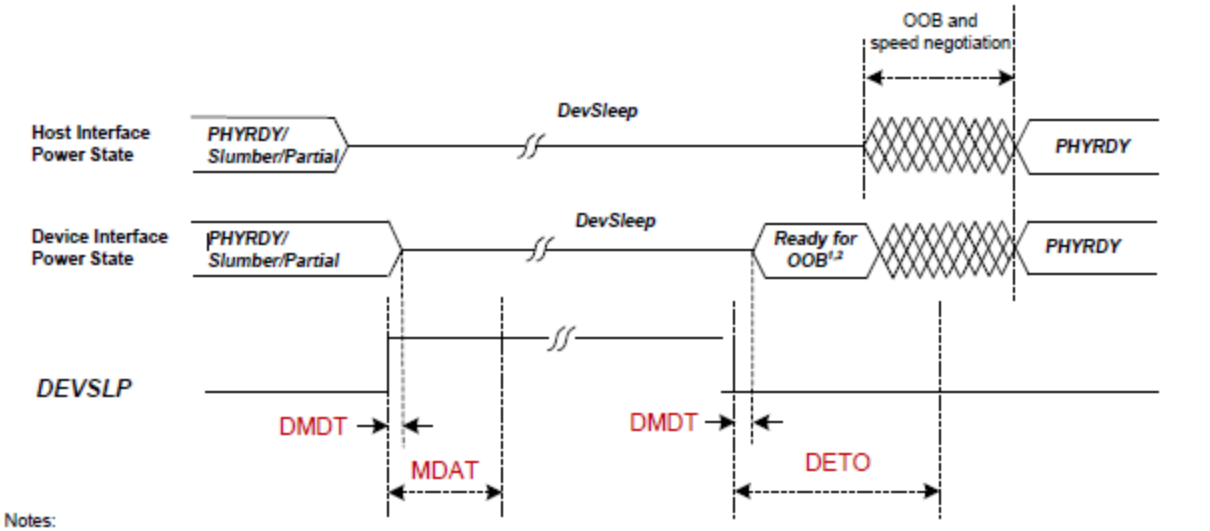
SATA PM – Entry and Exit


Spreadsheet View

	Time	Store#	Channel	Type - Initiator	Type - Target	Decode
	106.609.770.439	I2:40	I2	SATA_WTRM [3]		SATA_WTRM [3]
	106.609.770.504	T2:34	T2		SATA RX Seque...	SATA RX Sequence [3]
	106.609.770.564	T2:36	T2		SATA_R_OK [3]	SATA_R_OK [3]
	106.609.805.624	T2:38	T2		SATA_X_RDY [3]	SATA_X_RDY [3]
	106.609.805.730	I2:42	I2	SATA_R_RDY [3]		SATA_R_RDY [3]
	106.609.805.852	T2:40	T2		Register Dev->H...	STP REGISTER DEV->HOST (FIS 34);
	106.609.805.905	T2:42	T2		SATA_WTRM [3]	SATA_WTRM [3]
	106.609.805.964	I2:44	I2	SATA RX Sequence [3]		SATA RX Sequence [3]
	106.609.806.057	I2:46	I2	SATA_R_OK [3]		SATA_R_OK [3]
	106.609.806.124	I2:48	I2	SATA_R_OK [3]		SATA_R_OK [3]
S	106.610.852.444	I2:50	I2	SATA_PMREQ_P [3]		SATA_PMREQ_P [3]
	106.610.852.562	T2:44	T2		SATA_PMACK [12]	SATA_PMACK [12]
	106.610.852.642	T2:45	T2		RAW_DATA [2]	RAW_DATA [2], Errors: Inv 10b-code
	106.610.852.656	T2:45	T2		Begin DC Idle	Begin DC Idle
	106.610.852.690	I2:52	I2	RAW_DATA		RAW_DATA, Errors: Inv 10b-code, RD
	106.610.852.696	I2:52	I2	Begin DC Idle		Begin DC Idle
	106.611.777.164	I2:53	I2	COMWAKE		COMWAKE
	106.611.783.516	T2:46	T2		COMWAKE	COMWAKE
	106.611.784.902	T2:59	T2		End DC Idle	End DC Idle
	106.611.785.075	T2:60	T2		RAW_DATA [406]	RAW_DATA [406], Errors: Inv 10b-coc
	106.611.785.090	I2:66	I2	End DC Idle		End DC Idle
	106.611.785.263	I2:67	I2	RAW_DATA [464]		RAW_DATA [464], Errors: Inv 10b-coc
	106.611.790.402	I2:67	I2	SATA_X_RDY		SATA_X_RDY
	106.611.790.422	I2:68	I2	SATA_X_RDY [9]		SATA_X_RDY [9]
	106.611.790.540	T2:60	T2		SATA_R_RDY [3]	SATA_R_RDY [3]

SATA Device Sleep

- New addition to the SATA specification calling for lower power than slumber mode
- Uses external signal (DEVSLP) to enter and exit low-power mode allowing PHY's and other circuitry to be powered down
- Recovery time is specified as a maximum of 20 milliseconds



Notes:
1. The interface power state is in Partial/Slumber if DevSleep_to_ReducedPwrState = 1 and DEVSLP was asserted while device was in Partial/Slumber.
2. The interface is in active state if DevSleep_to_ReducedPwrState = 0 or DEVSLP was asserted while device was in active state.

Issues Facing Validation of DevSlp

- Is DevSlp present?
- Validate specification mandated timing
- Emulate HBA functionality for drive validation

Is DevSlp Present?

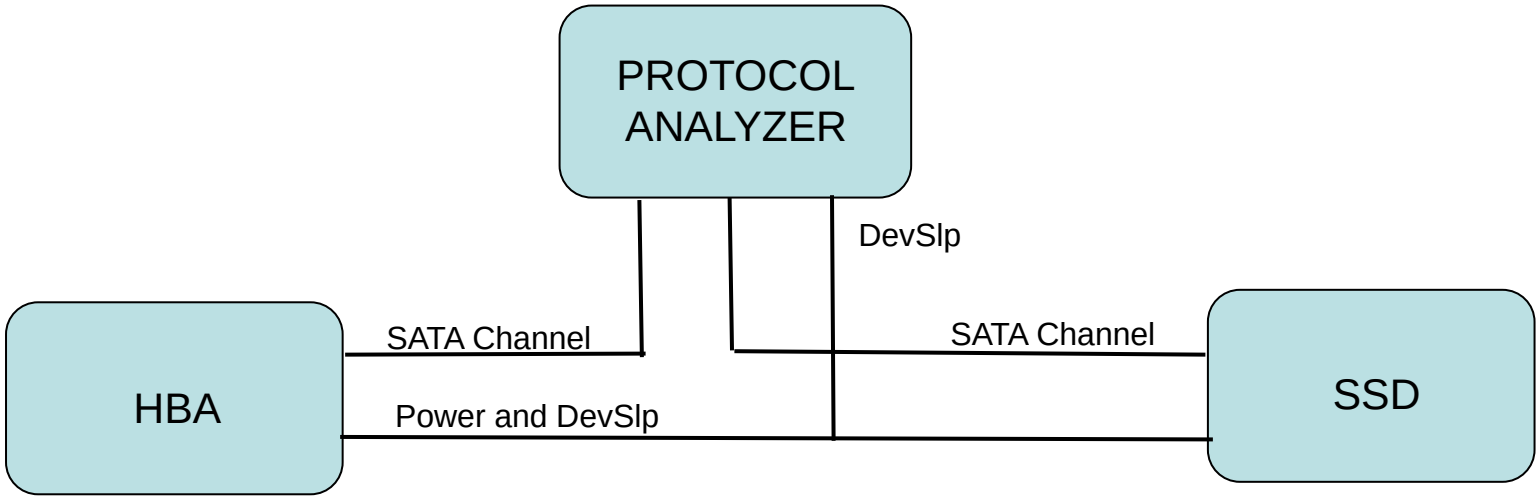
- A more difficult question than first appearances
- Trivial to check with an oscilloscope
- Must ask the question “Was DevSlp asserted properly when drive was in a PM state?”
- Caution! – DevSlp is asserted via a high-value (1Mohm or greater) pull-up resistor
  - Slooooow rising signal
  - Can cause multiple triggering in a fast scope or voltage comparator
  - Hysteresis circuit is recommended

Does DevSlp Meet Timing?

- DevSlp is an out of band signal
- Dedicated pins on SATA and M2 power connector
- Requires measurement to SATA data stream events
- On DEVSLP Assertion
  - Host must assert DEVSLP for >= 10ms, or as specified in Identify Device Data Log;
- On DEVSLP Negation
  - Device must detect OOB in <= 20ms, or as specified in Identify Device Data log

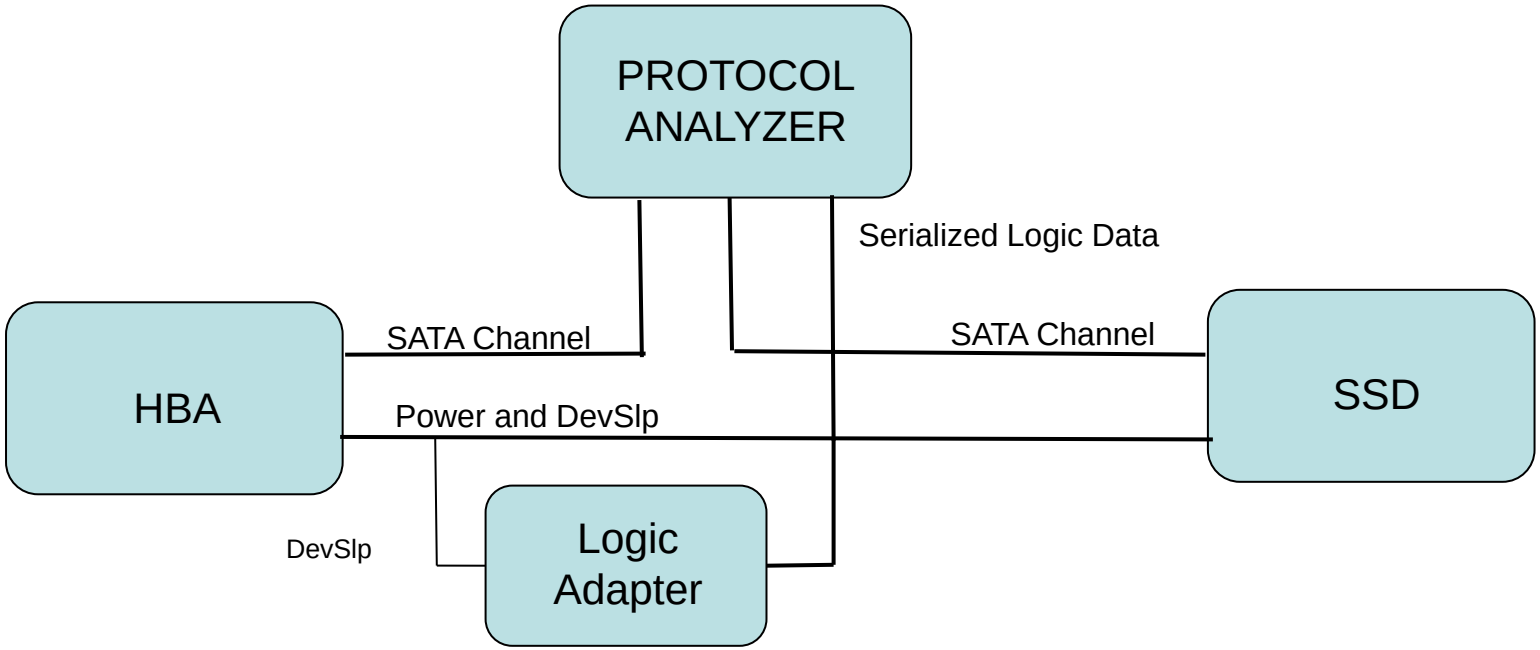
DevSlp Timing Analysis

- Traditional Approach to DevSlp Analysis



DevSlp Timing Analysis

- "New" Approach to DevSlp Analysis



SerialTek Logic Adapter

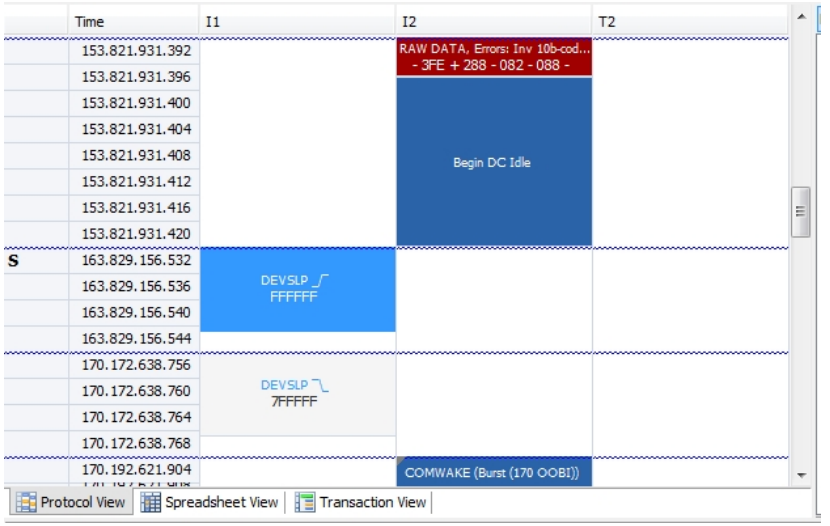
- SerialTek LA-3ST-24 Logic Adapter
  - SATA DEVSLP Support
  - Simultaneous Serial and Logic Analysis
  - 24 Logic Inputs per Adapter
  - Adjustable VoltageThreshold
  - Works with BusXpert Analyzer and Software
  - Self-contained with Built-in Universal Power Supply

Setting up the Logic Adapter

- Setup
  - Connect the SATA port” on the Logic Adapter to any port on the analyzer
  - Power adapter cable is connected between the HBA and the drive
  - DEVSLP breakout wire is connected to bit 23 of the Logic Adapter
  - Adjust the input threshold setting appropriately
  - Connect the SATA port of the Host to any input port of the analyzer and the drive to the corresponding target port of the analyzer.

Viewing the Trace

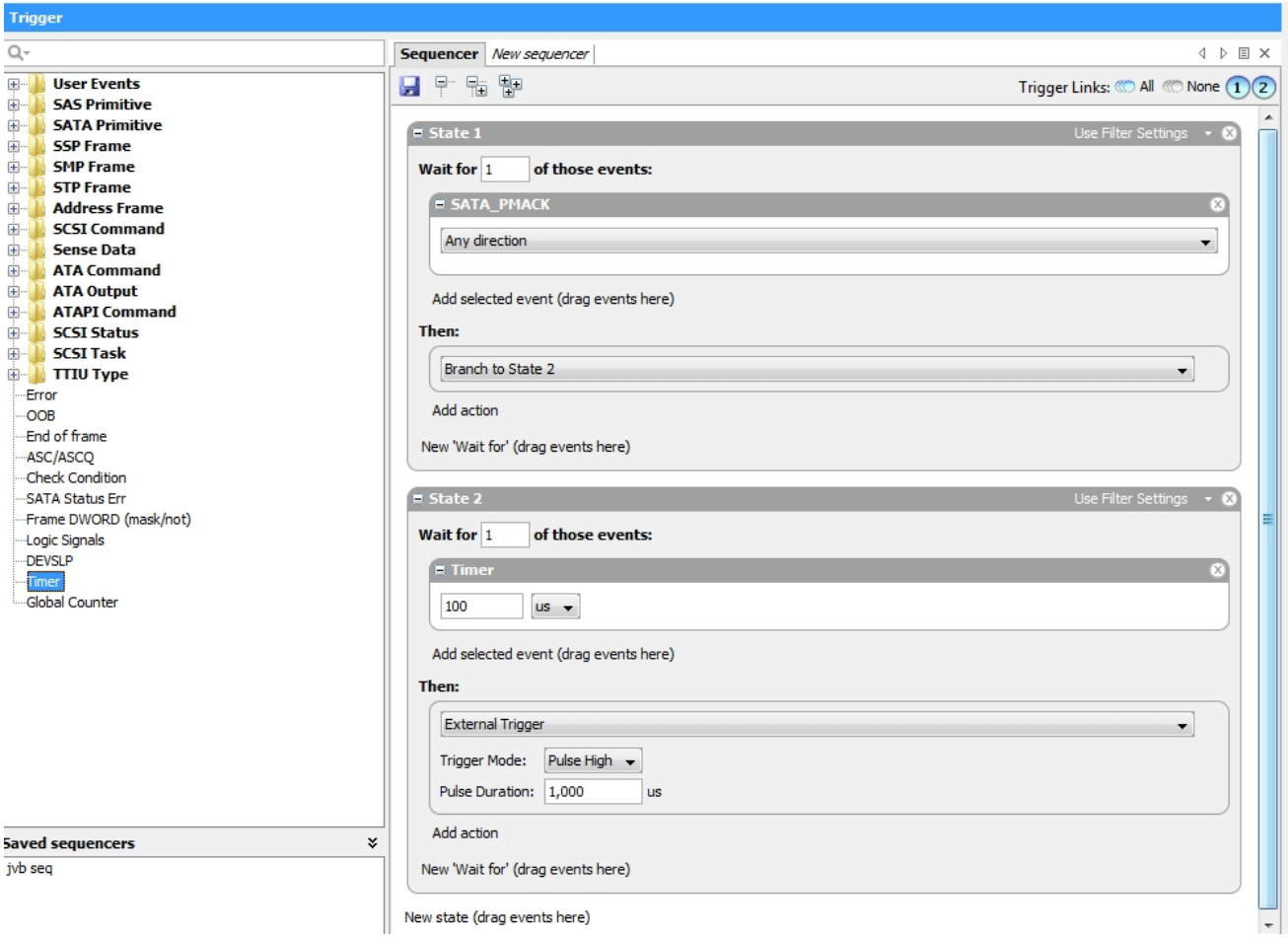
- Logic signals can ve seen Protocol, Spreadsheet and Histogram views.
- Protocol View
  - Devslp (bit 23) transitions will be indicated with a graphical waveform and titled “DEVSLP”
  - Transitions of any other logic signal (bits 0 – 22) will be titled “LOGIC SIGNAL”
- Spreadsheet View
  - Transitions are labeled “DEVSLP” or “LOGIC SIGNAL” as appropriate
- Histogram View
  - No distinction between Devslp and logic signals



How Can I Generate a Devslp Signal

- The “Trigger Out” action can be used to generate a signal that simulates the Devslp signal.
- Using Trigger Out as the action, the analyzer waits for the trigger event.
- SATA_PMACK can be used as the trigger event as this would allow the Devslp signal to be asserted without interfering with normal SATA activity
- The illustrated trigger waits for SATA_PMACK, delays for a short time and then issues a logical high pulse for 1 millisecond

Generating Devslp - Example



Conclusion

- Evaluating “out of band” signals such as DevSlp is possible using state of the art analysis equipment.
- “Out of band” signals will continue to be present in specifications and must be accounted for in validation and verification
  - i.e. #CLKREF in PCIe
- THANK YOU!