Overcoming Challenges in 3D Architecture Memory Production

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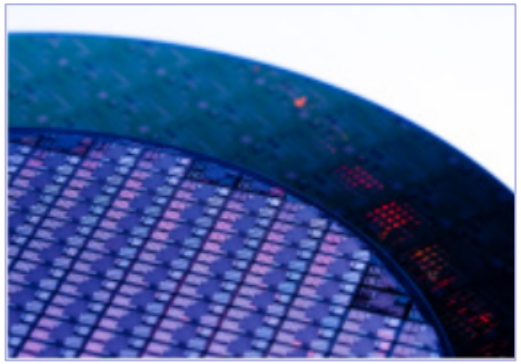
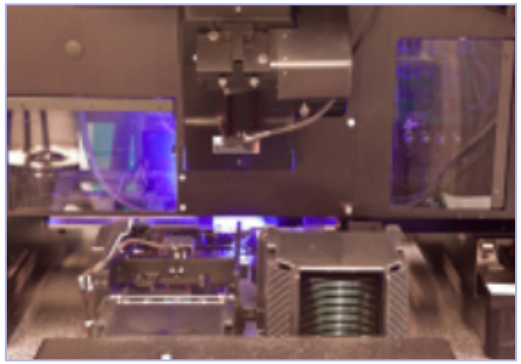
3D Flash – Current State

- **3D-Flash will replace 2D by 2016**
  - All leading NAND players support this trend
- **Planar NAND is being replaced because the market requires:**
  - Higher density
  - Higher capacity


2D -> 3D with Current NAND

Any 3D technology that replaces 2D has to meet the following requirements:

- Performance of the cell should be comparable or better
- A significant increase in density
- Lower cost/ bit than 2D

3D Flash – NAND Challenges

Performance

- Comparable to current 2D cell which is electron based – **MLC is more challenging**

Density

- **Vertical etch technology** is doable but **comes at a cost**
  - New etch/Cleans development and equipment
  - Fab cost ~ 2x

Capacity

- **Stacking** solves this problem again **at a cost**

3D RRAM – A Simple Solution

Process Implementation

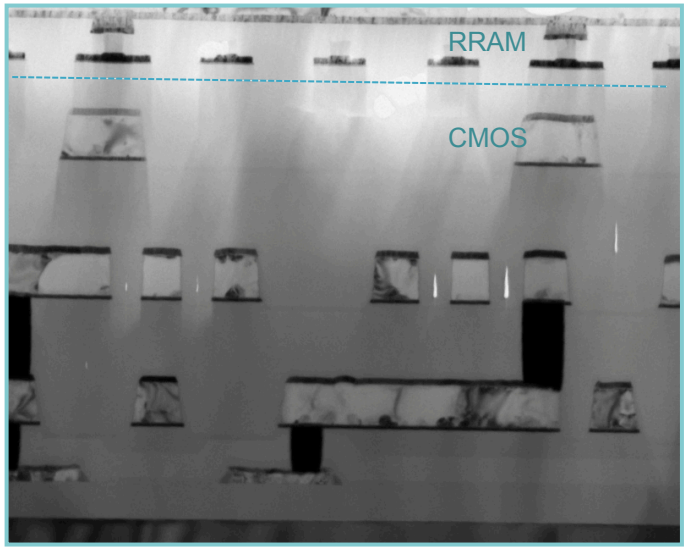
- Simple process
- Use existing toolset
- Stacking architecture is built one layer at a time

Better Cell Performance

- Filament based instead of electron based
- Ability to drive many cells with a single transistor
- Lower I_{OFF} with smaller geometries
- Higher I_{ON}/I_{OFF} enables MLC

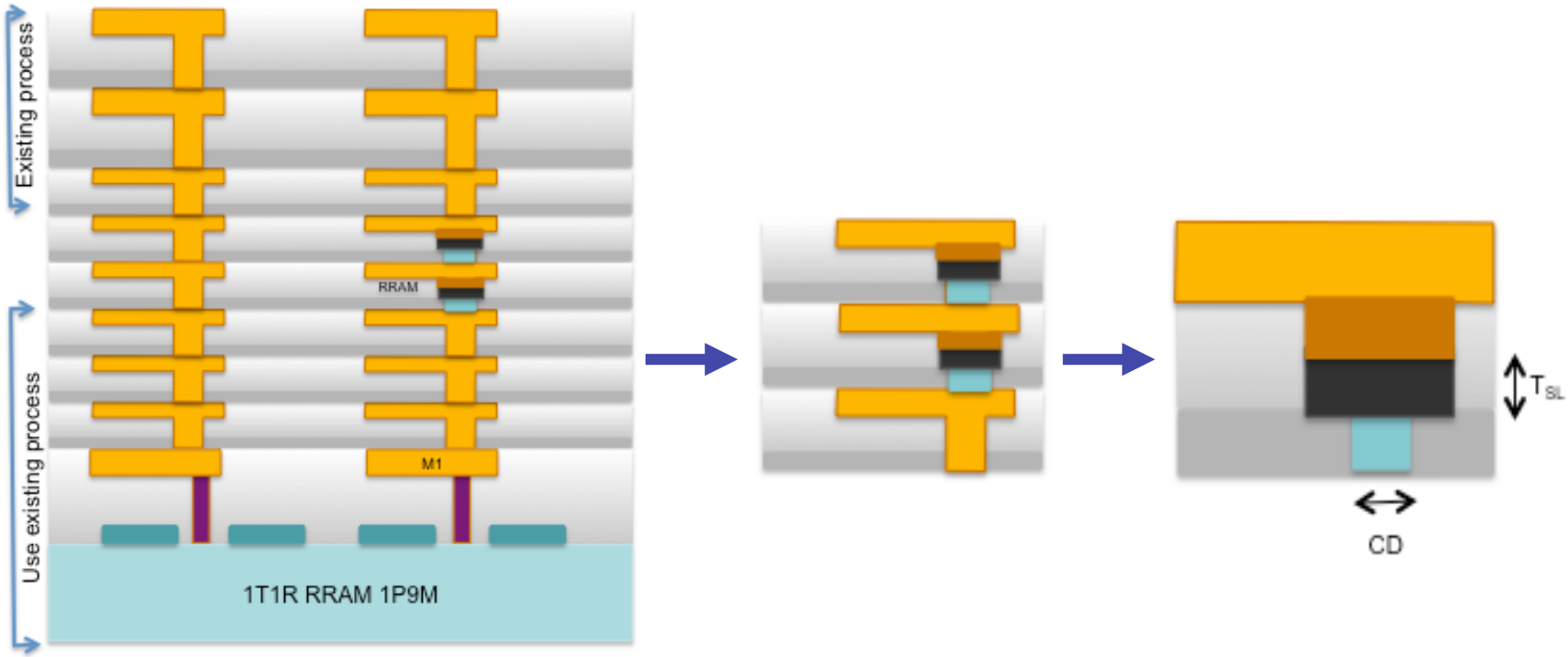
3D RRAM – Stacking

- Monolithic integration of RRAM on CMOS ✅



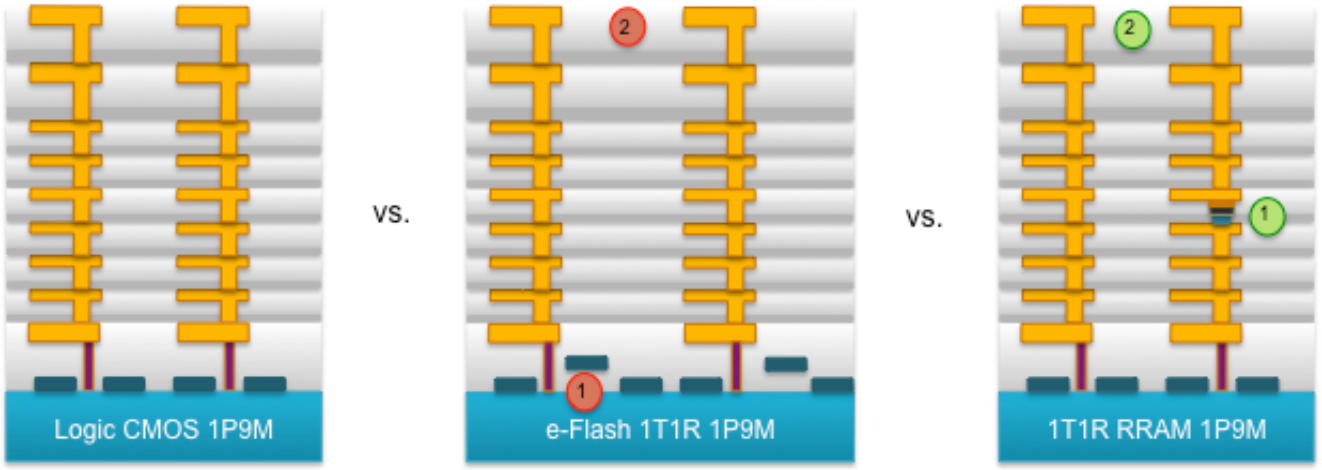
- Thermal budget requirements met for
  - RRAM on CMOS ✅
  - RRAM on RRAM ✅
- Minimal area overhead from the access transistors ✅

3D RRAM – Scaling



- Simple approach to control cell parameters using 50nm node
- CD controls I_{OFF} and T_{SL} (~10nm) the I_{ON}
- Cell proven at 8nm CD ✅

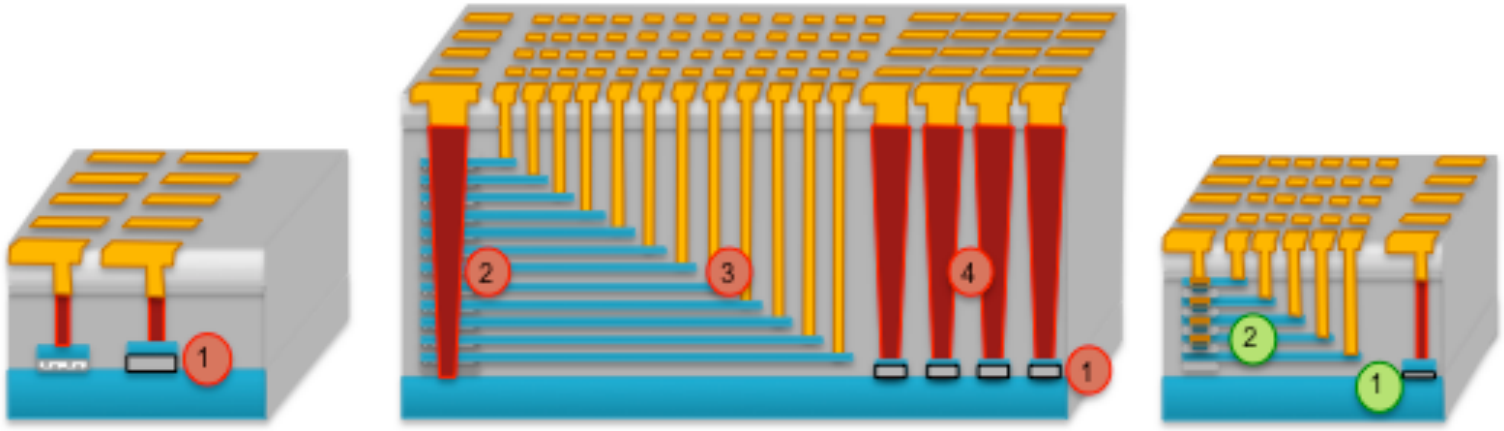
Start Simple – Adding1st RRAM Layer



Attribute	Logic CMOS	E-flash	RRAM
Masks	31	>37 (31 + at least 6)	33 (31 + 2) 1. RRAM BE Via . 2. RRAM Metal collar
Steps	~200	~ 240	~208

- Provides a solution that is far superior
  - ***Imagine the possibilities!***

3D RRAM Architecture – Multiple layers



Attribute (Impact)	Planar NAND	3D-NAND	3D-RRAM
Transistor Size (Die Size)	High Voltage ~25 V	High Voltage ~25 V	Low Voltage (<3 V)
Density Scaling (Die Size, Yield)	63 serial Transistors Below 16nm not possible	Scales Vertically to 26-32 layers Equivalent to 55nm node	Scales as CMOS logic scales with no restrictions to sub 10nm 4-8 layers equivalent to 20nm node
Via Angle Complexity (Die Size, Yield)	Low	Very high	Low
Added Cost (Fab, Materials)	None	~2x Fab cost 20% tool cost	~4% per layer No 3D etch tool cost

Summary

- **3D Flash will replace 2D Flash** to meet the market demand for density and capacity
- **3D-RRAM provides a simple solution** that is stackable, scalable and provides a Multi Level Cell with monolithic CMOS integration
- **Logic fabs can covert to Memory fabs** with minimal overhead and implement 3D memory using RRAM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