BIO: Terry Grunzke

Terry Grunzke, Principal Applications Engineer, Micron Technology

Terry's current responsibilities focus on the development of memory products and enabling activities for Micron's NAND devices. Terry has nearly 20 years of SRAM, DRAM, and NAND experience at Micron in areas of characterization, test, product, and applications engineering.

Terry has more than twenty patents or patents pending related to memory technology and is the current Chairperson for the ONFI Technical Committee.

Terry holds a BSCE from the University of Minnesota, Duluth

ONFI 4.0: Faster I/O speeds at lower power consumption

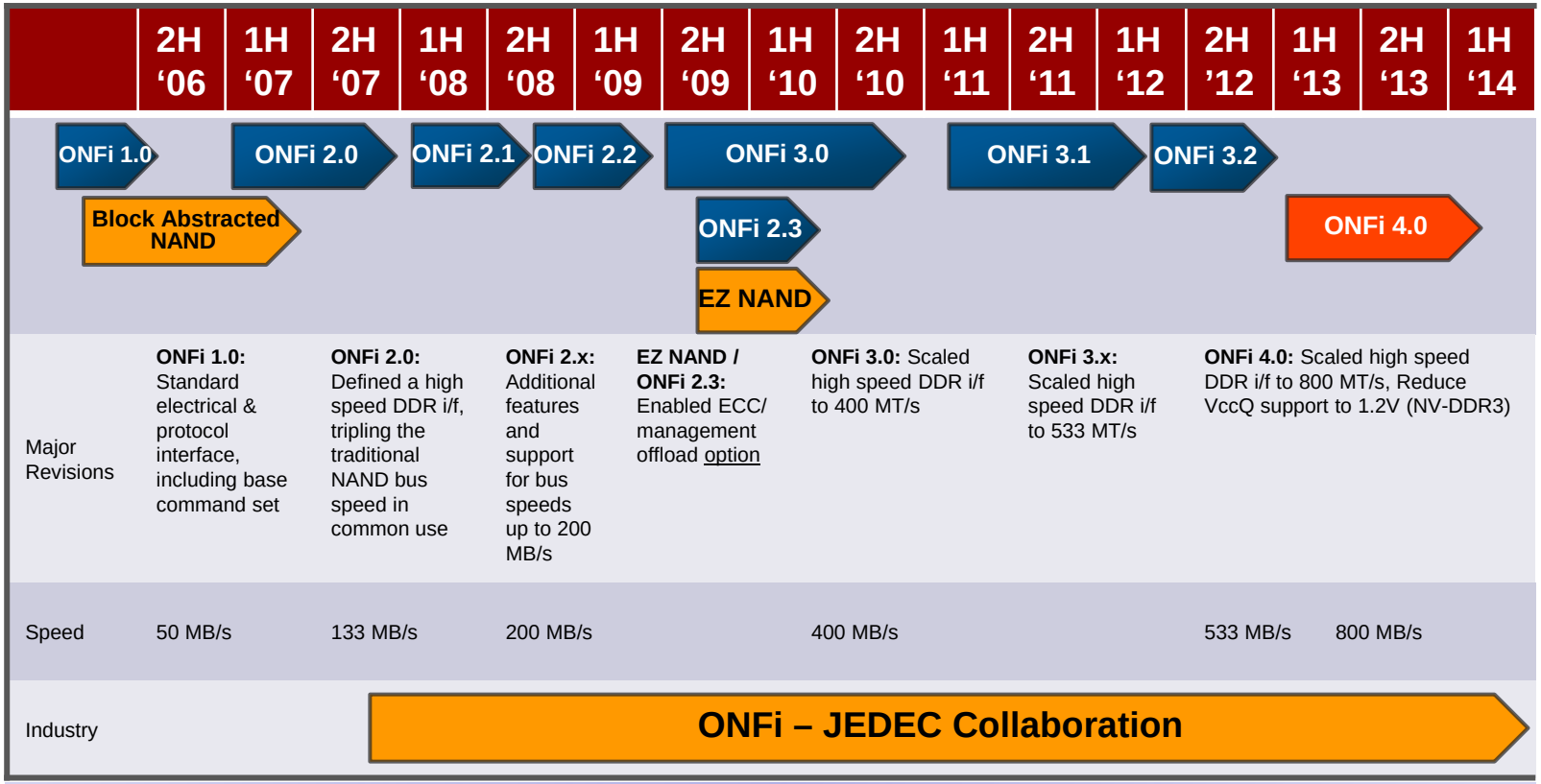
Terry Grunzke

Micron Technology

ONFI 4.0: Adopted April 2014

- Reduces I/O power consumption
  - Lower I/O voltage
  - Reduced termination requirements
- Increases I/O performance
  - Scale I/O speeds faster as NAND page sizes grow
  - Soft data requirements
  - Latency reduction
- Continues interoperability between vendors
  - Collaboration in JC42.4 ONFI/JEDEC Joint Task Group

ONFI Workgroup Continues To Produce Results!



ONFI has and continues to deliver innovation & interoperability enabling faster NAND adoption

ONFI 4.0 Features

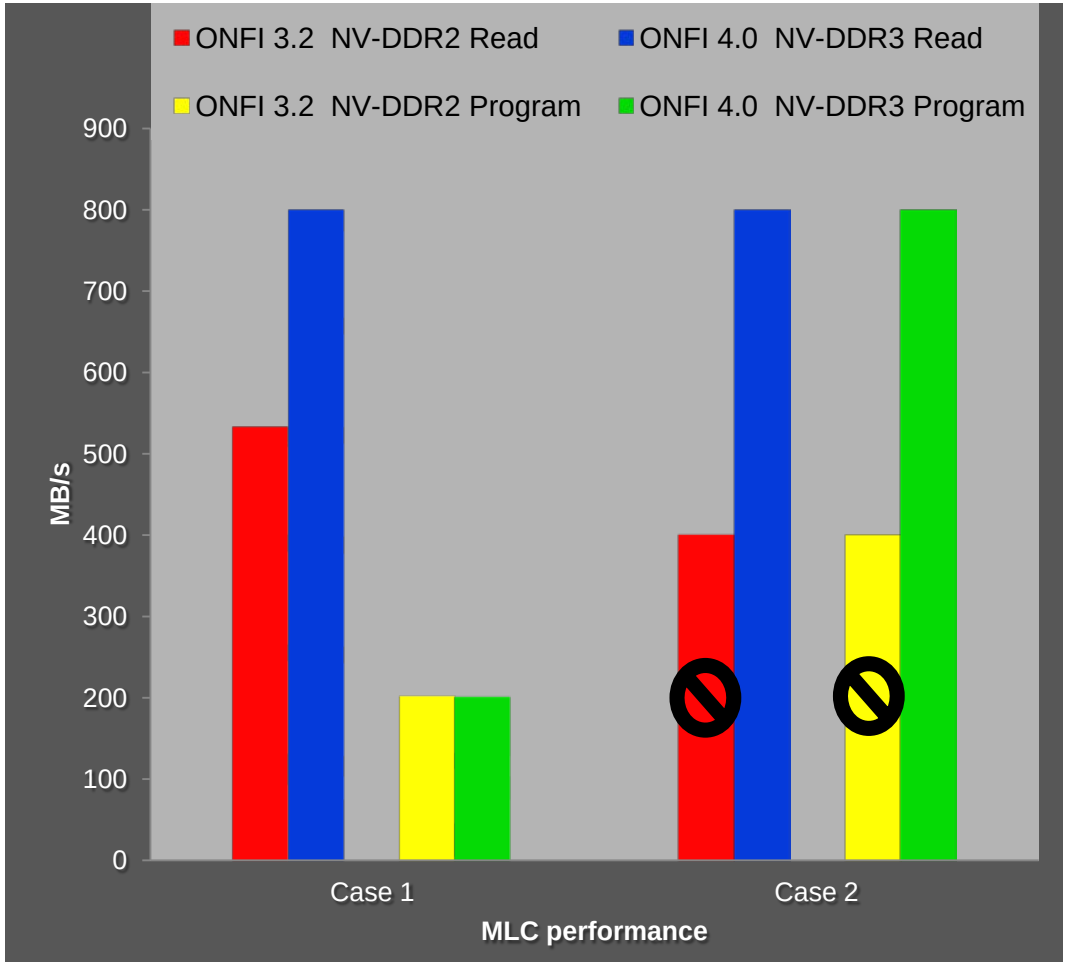
- NV-DDR3:
  - VccQ = 1.2V (1.14V – 1.26V)
  - Evolutionary interface from NV-DDR2
    - Same packaging, Opcodes, timing diagrams/parameters, etc
    - All of the ONFI 3.x features will continue to be supported
      - Matrix Termination, CE reduction, Volume addressing, Differential signaling, VPP, External VrefQ, Warm Up cycles, etc…
    - Same output drive strength and RTT settings
- Maximum I/O speeds increased
  - 667 MT/s and 800 MT/s timing modes added
- ZQ calibration supported
  - RZQ = 300 ohms +/- 1%
  - Long (F9h) and Short (D9h) Calibration commands

ONFI 4.0 Differences

- Devices that support NV-DDR3 may not support VccQ = 3.3V
- NV-DDR3 Interface will not power up in SDR (i.e. Async)
  - SDR, NV-DDR, NV-DDR2 not supported at VccQ=1.2V
  - Agnostic READ ID will provide information on power on interface
- tADL and tCCS will push out due to larger page sizes and data path design requirements to achieve faster I/O speeds
- Electrical Package Specifications for Zpk and Tpd
  - Same methodology as DRAM DDR4
- Possible reduced Driver strength settings supported

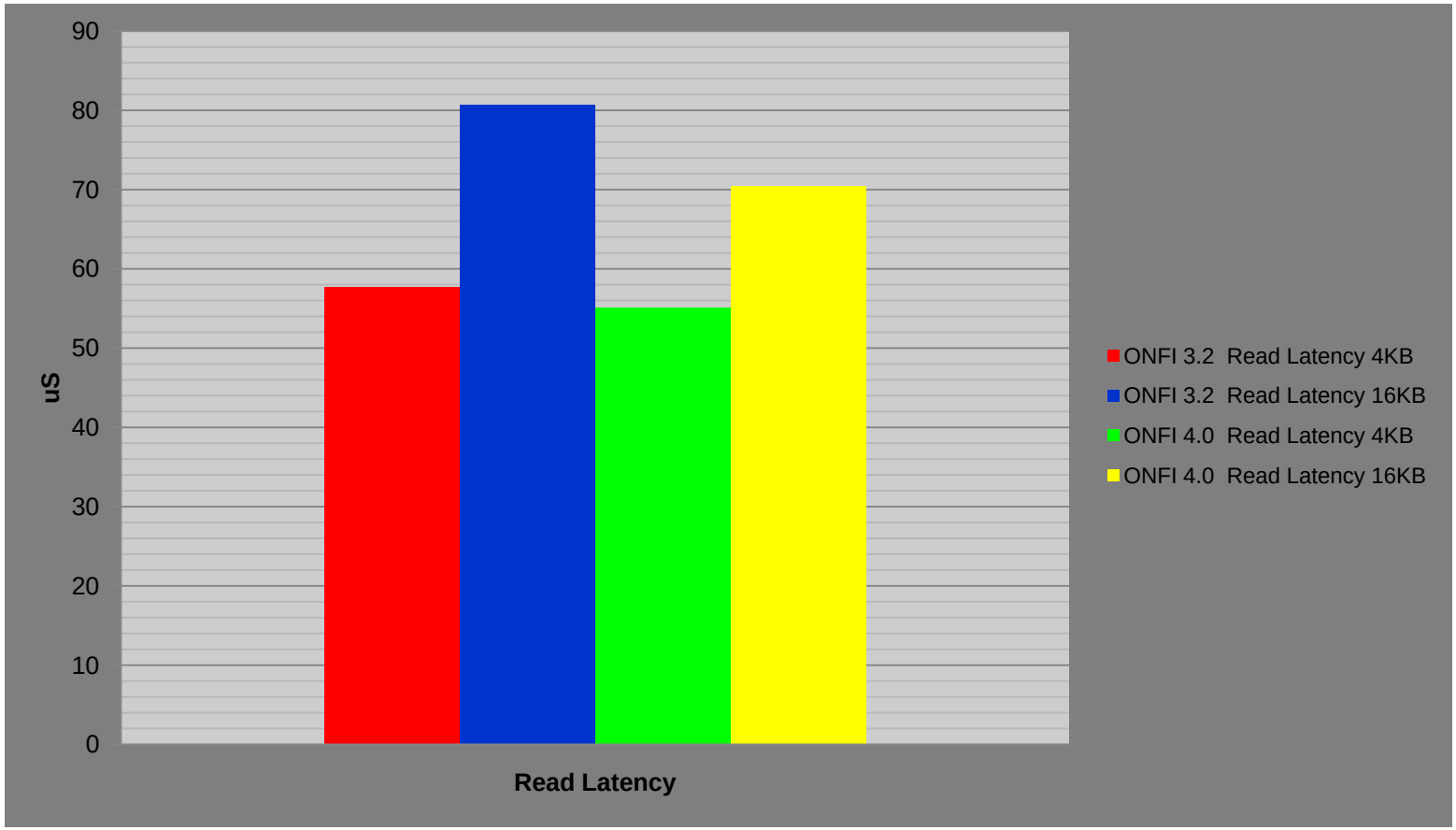
ONFI 4.0 Performance

- Numbers are highly dependent on NAND/system architecture
  - Page size / number of LUNs
  - Number of planes
  - tPROG/tR
  - Programming Algo
  - Available System buffering
- SI highly dependent on a number of factors
  - Topology
  - Channel length
  - Package Zpk/Tpd
  - PCB Design
    - Impedance
    - Trace matching
  - Available drive strengths/RTT
  - RON/RTT variance
  - Controller overshoot restrictions
  - Controller/NAND capacitance



Case 1: 32KB “super” page, tPROG(typ) = 1300us, 8 die active
Case 2: 64KB “super” page, tPROG(typ) = 1100us, 12 die active

Read Latency

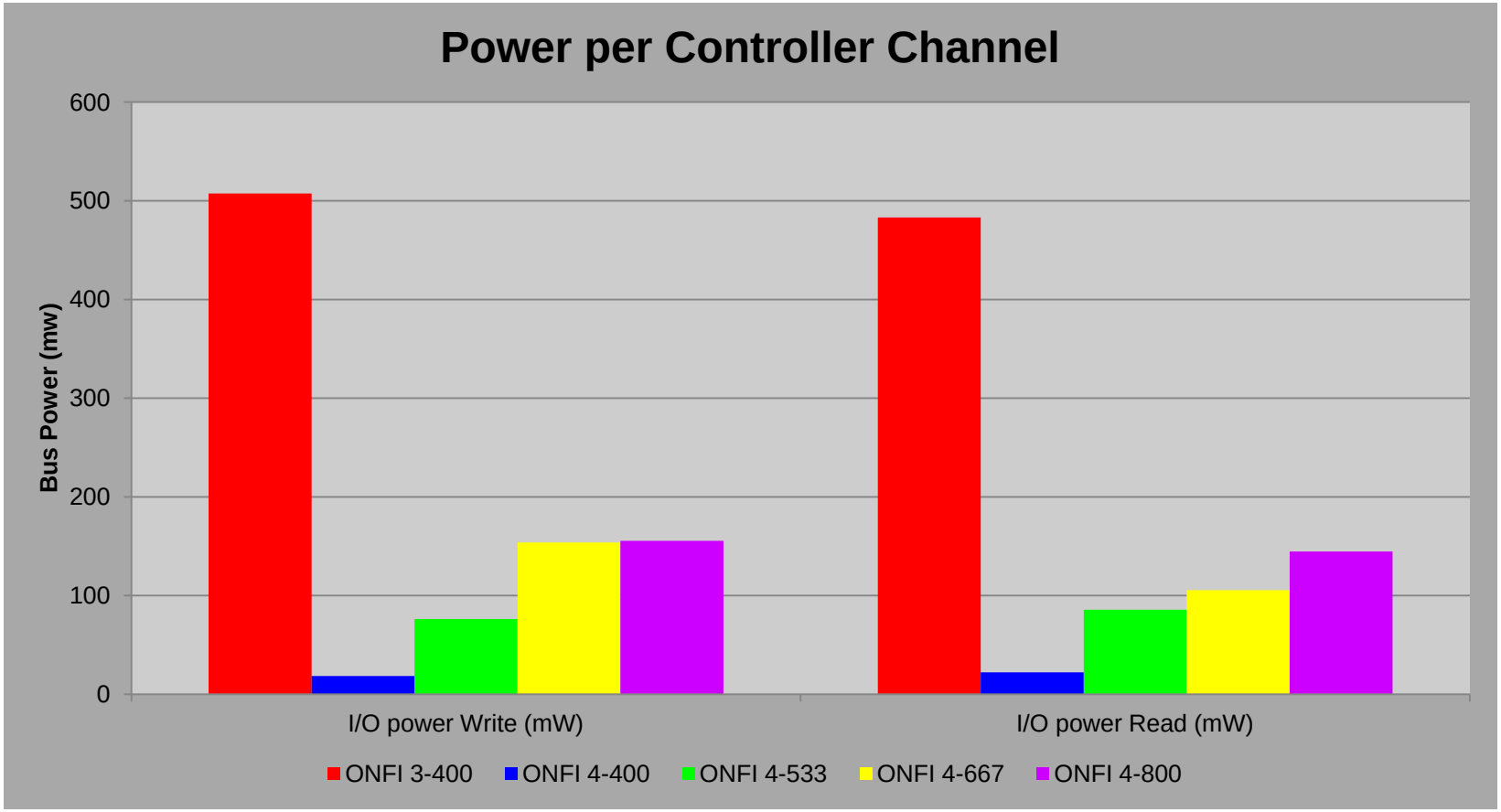


4KB read latency has diminishing returns

ONFI 4.0 Bus Power Reduction

- Switching power reduction
  - $P = FV^2C$ **V:** 1.8V -> 1.2V **C:** Significantly Reduced
- Termination power reduction
  - Rtt requirements reduced
- NAND data path power reduction
  - Can provide improved NAND data path power biasing

Power comparisons



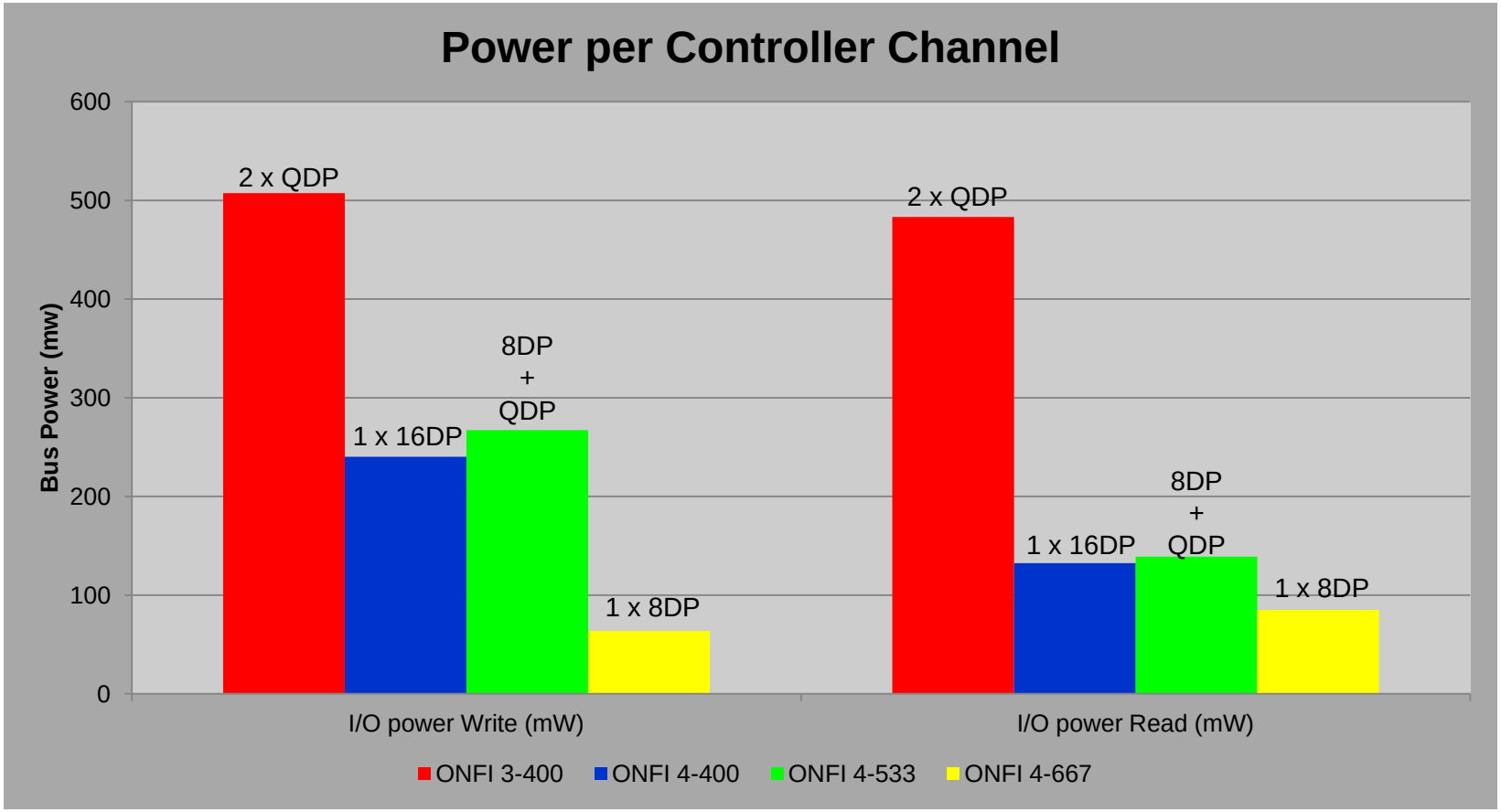
SSD topology with two QDP packages per channel (8 die)

Reduced Loading

- Reduced Die Capacitance and smaller signaling also enables new topologies and increased fan-out:
  - 8 Die per channel at 400 MT/s with no termination
  - 16 Die per channel at 533 MT/s
  - 12 Die per channel at 667 MT/s
  - 8 Die per channel at 800 MT/s

Estimates are based on Signal Integrity analysis, actual performance may vary based on a number of system variables

More LUNs per channel



At lower power consumption

Summary

- ONFI 4.0 provides:
  - I/O Performance improvements
  - I/O and NAND Power consumption improvements
  - Straightforward evolutionary enablement
  - Industry interoperability
- ONFI 4.0 specification available for download
  - www.onfi.org/specifications