What's Changing In NAND Flash

And What Isn't

Jim Handy

OBJECTIVE ANALYSIS

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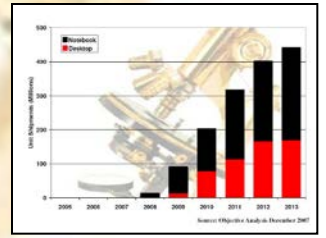
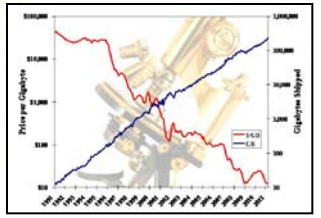
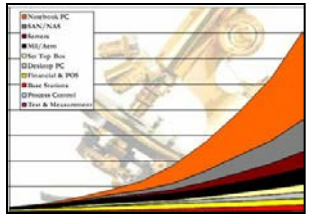
Profound Analysts

Reports & Services

Custom Consulting







Agenda

- Market Changes
- Technology changes
  - New cell structures for 1Ynm
  - 3D structures
  - When will NAND die off?
- How will this impact designers?

NAND Gigabyte Demand

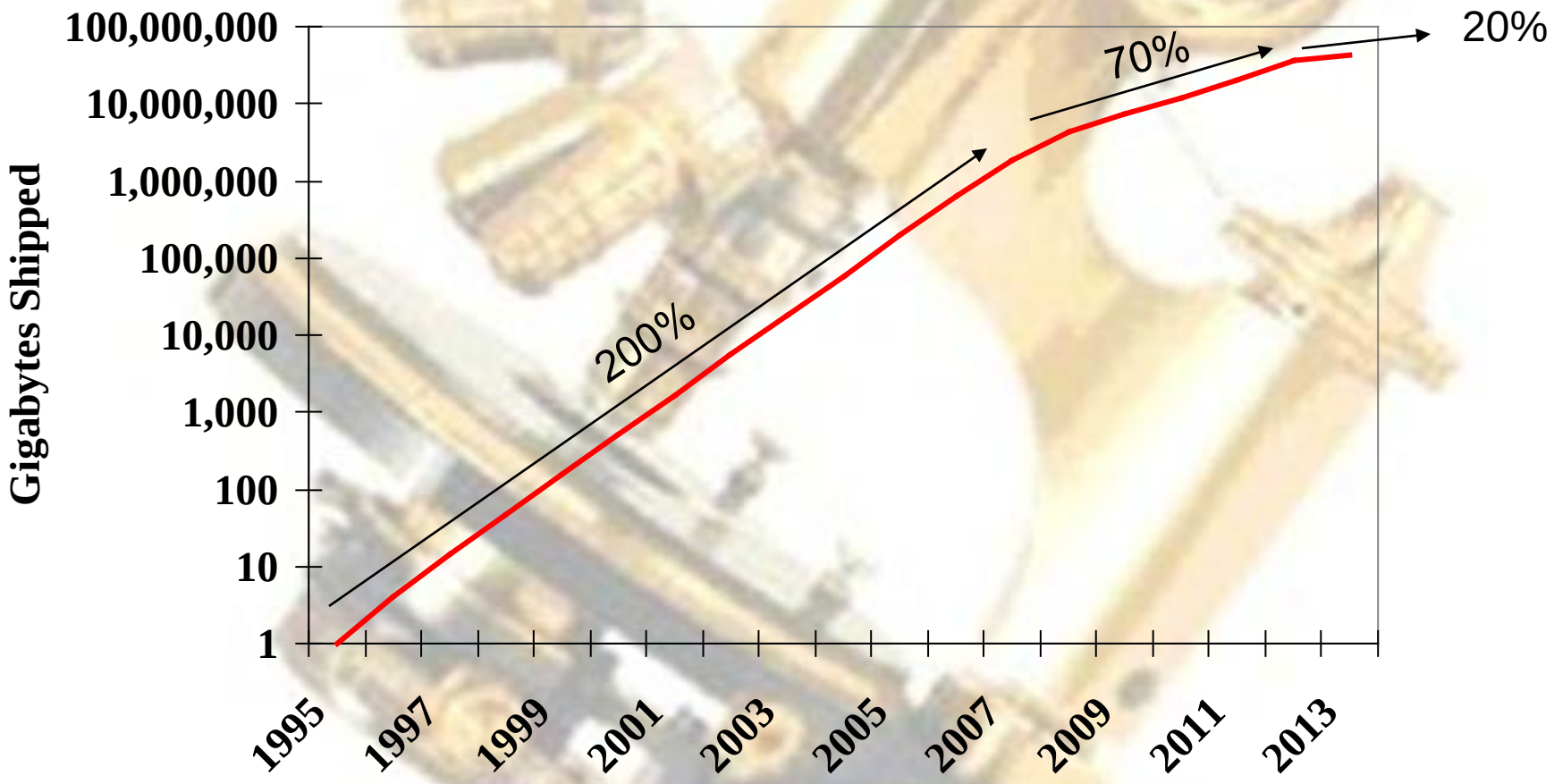
Yesterday:

- Cannibalizing established markets
  - Photo film
  - Floppy disks
  - CDs
  - Video tape
  - DVDs
- Very rapid growth

Today & Tomorrow:

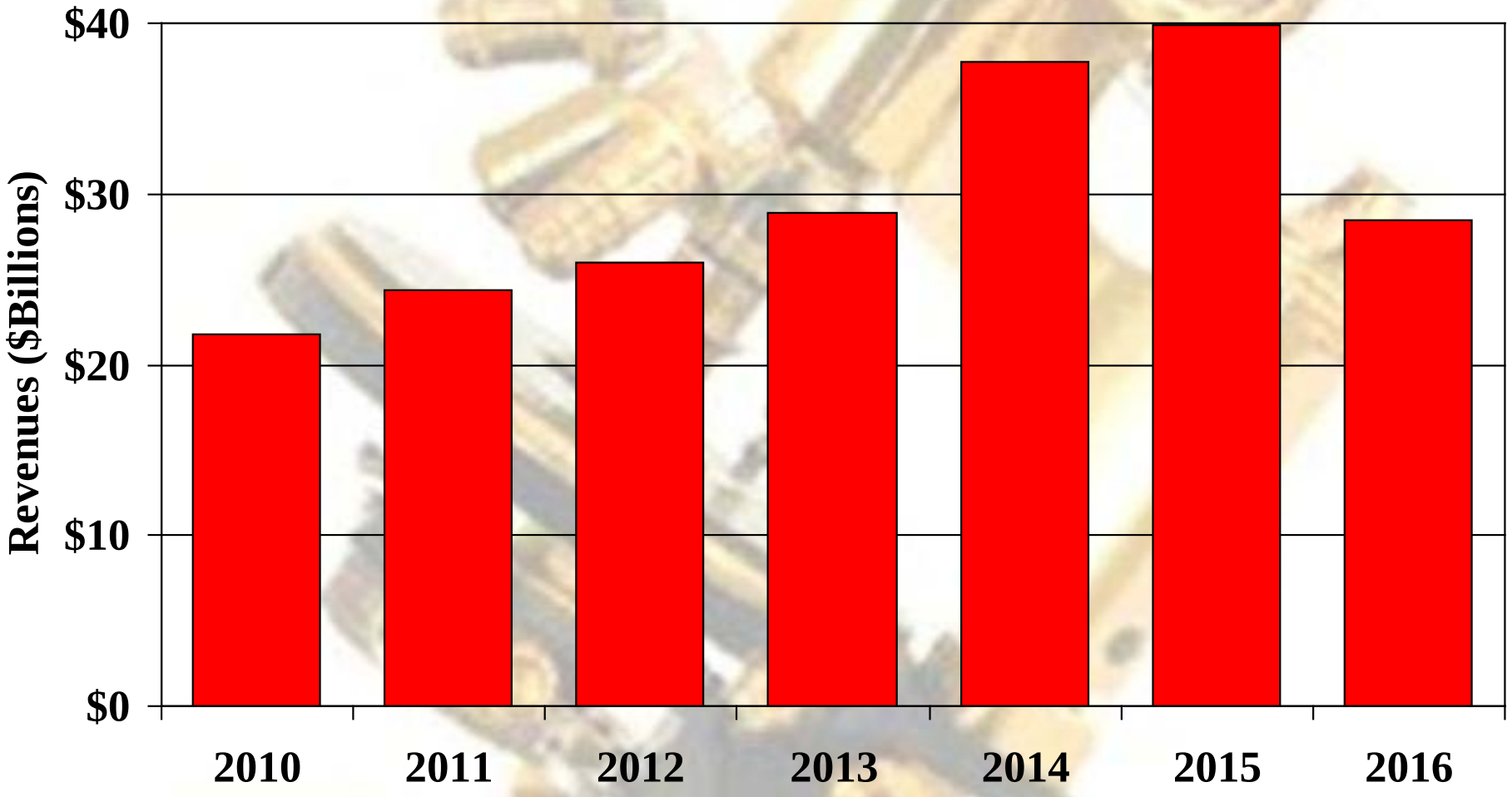
- Creating new markets
  - Smart phone
  - Tablet PC
  - Tier 0 storage
    - SSDs
    - Flash Arrays
    - Flash DIMMs & PCI
- Growth is slower in new markets

Gigabyte Growth is Slowing



But that's not a bad thing!

Typical NAND Flash Cycle Forecast



But Change Is In The Air

- Moving to 1Ynm or 1Znm is tricky!
  - Hi-k gate dielectric
  - Quad patterning
  - Yipes!
- 3D comes next
  - Scales cost by adding layers
  - Needs technologies never used before
  - Likely to stumble, a LOT
  - Massive and costly tooling changes
- This may stall production GB growth

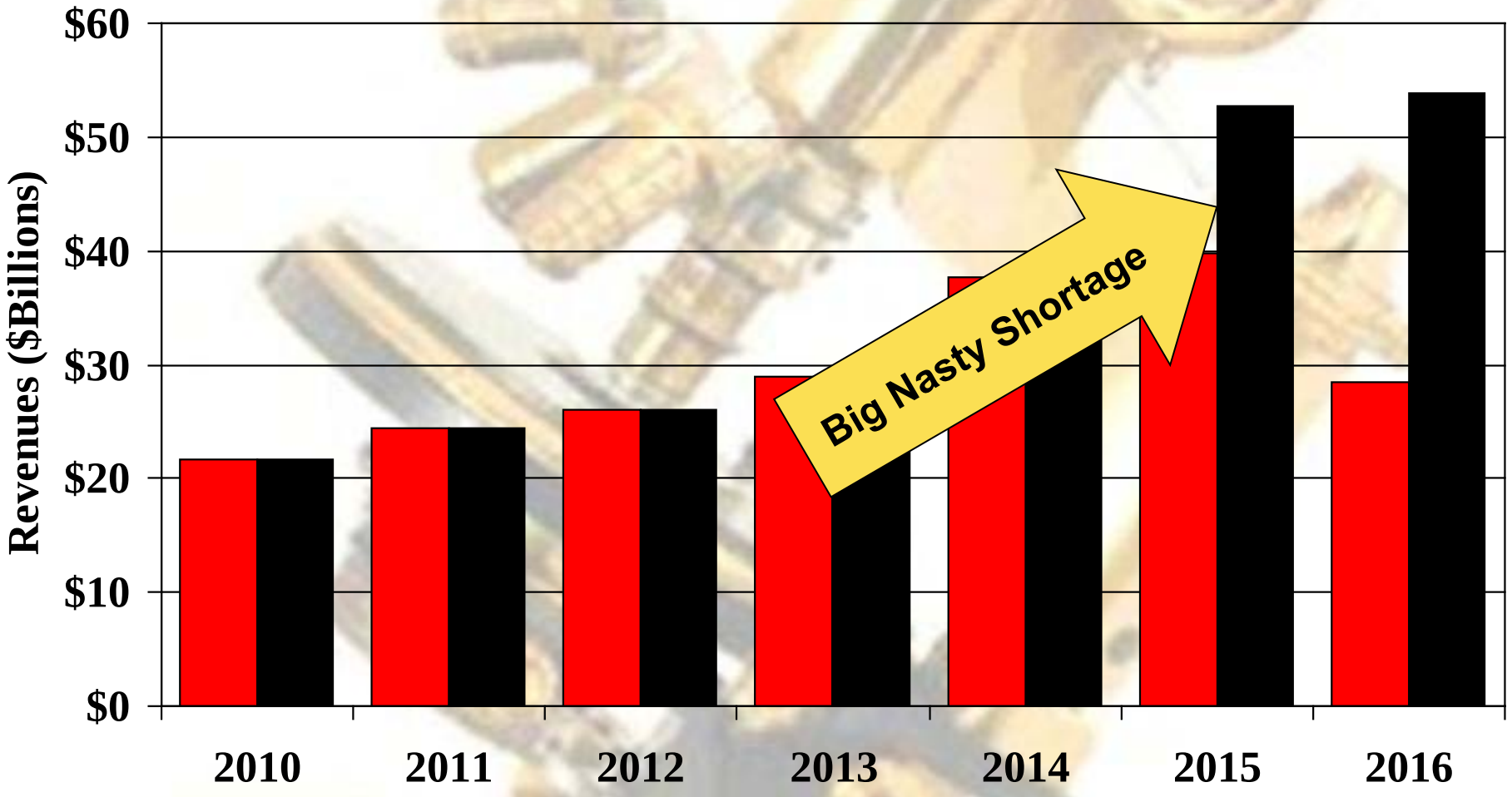
Production Bit Growth

GB growth% =

f(Wafer Growth%,GB/Wafer Growth%)

- Two factors are used to pace production to market demand:
  - Increasing wafer starts
  - Increasing GB/wafer
- The first just takes money, the second has become a big challenge

What If GB/Wafer Growth Stalls?

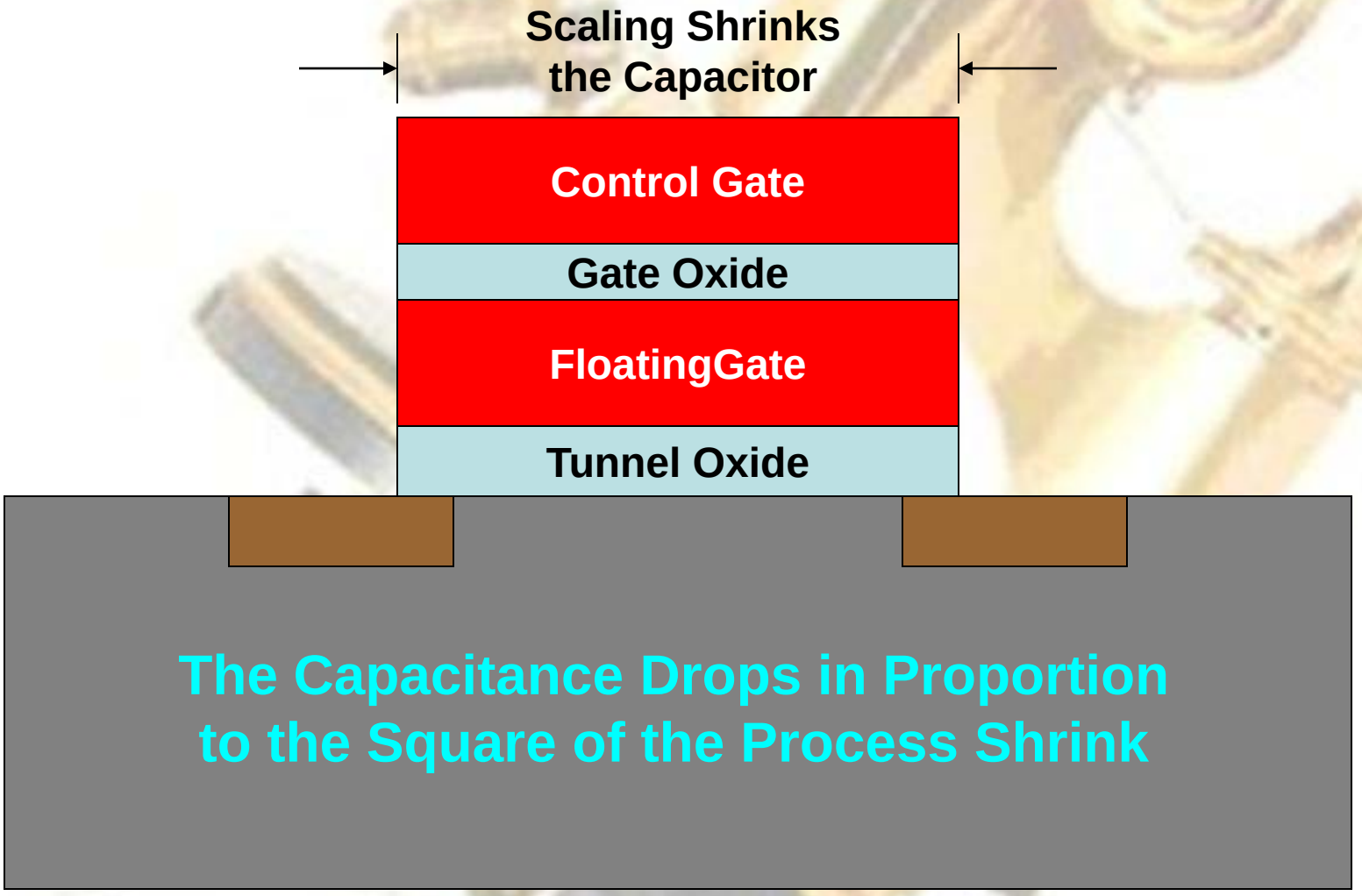


So Let's Talk About Those Issues!

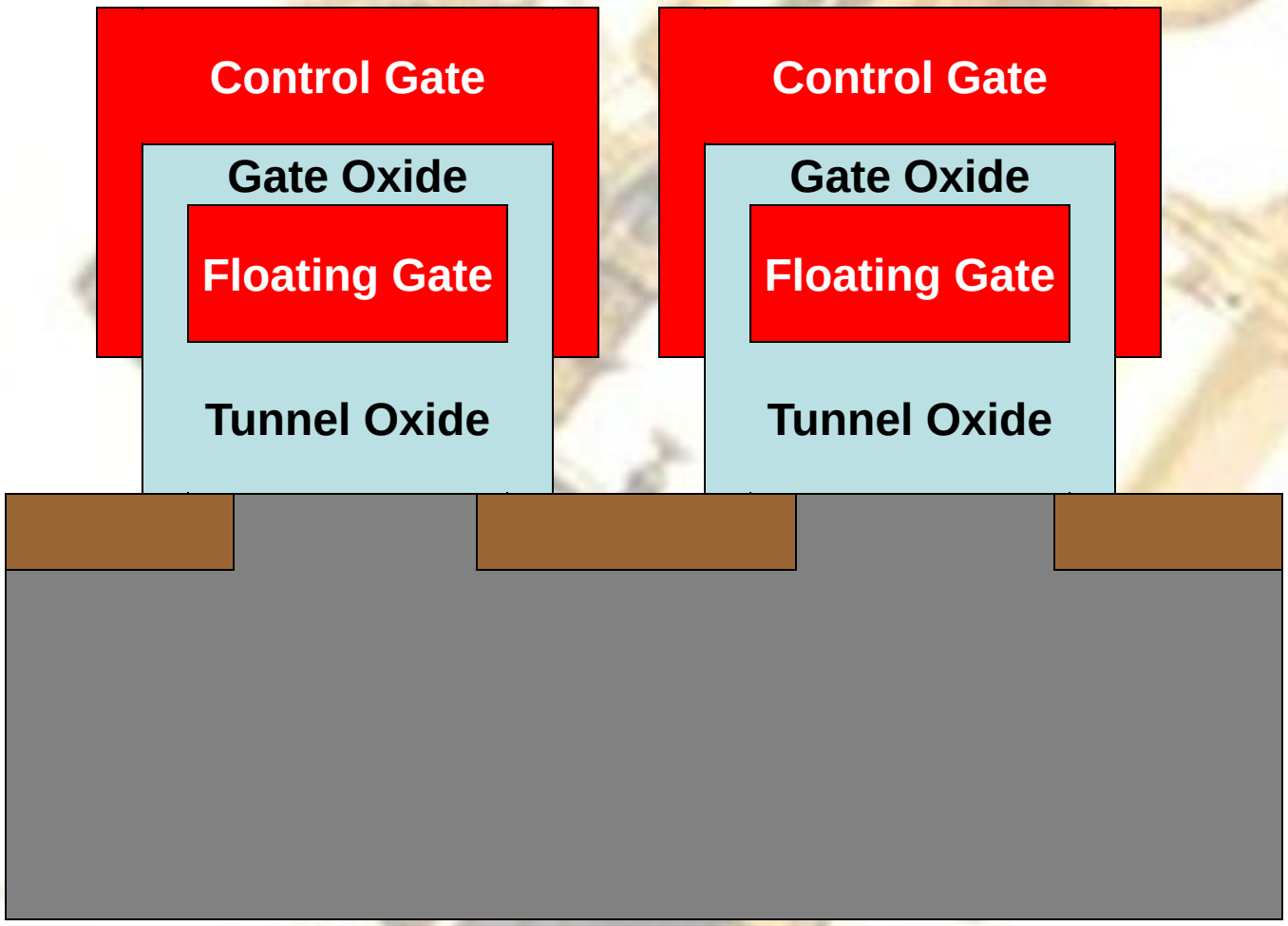
Planar NAND Issues

- Control Gate to Floating Gate capacitance
  - New structures
  - New materials
- Lithography issues
  - Immersion lithography ($$$)
  - Multiple patterning

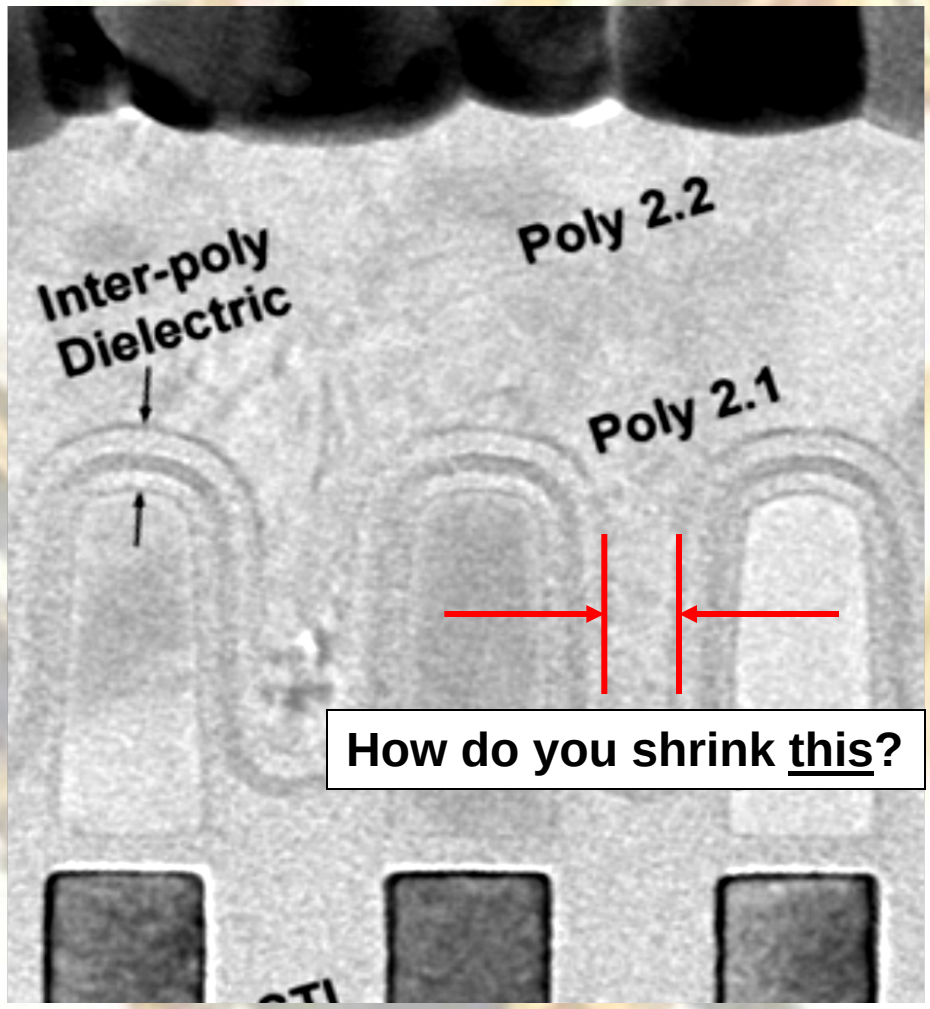
Original Floating Gate Geometry



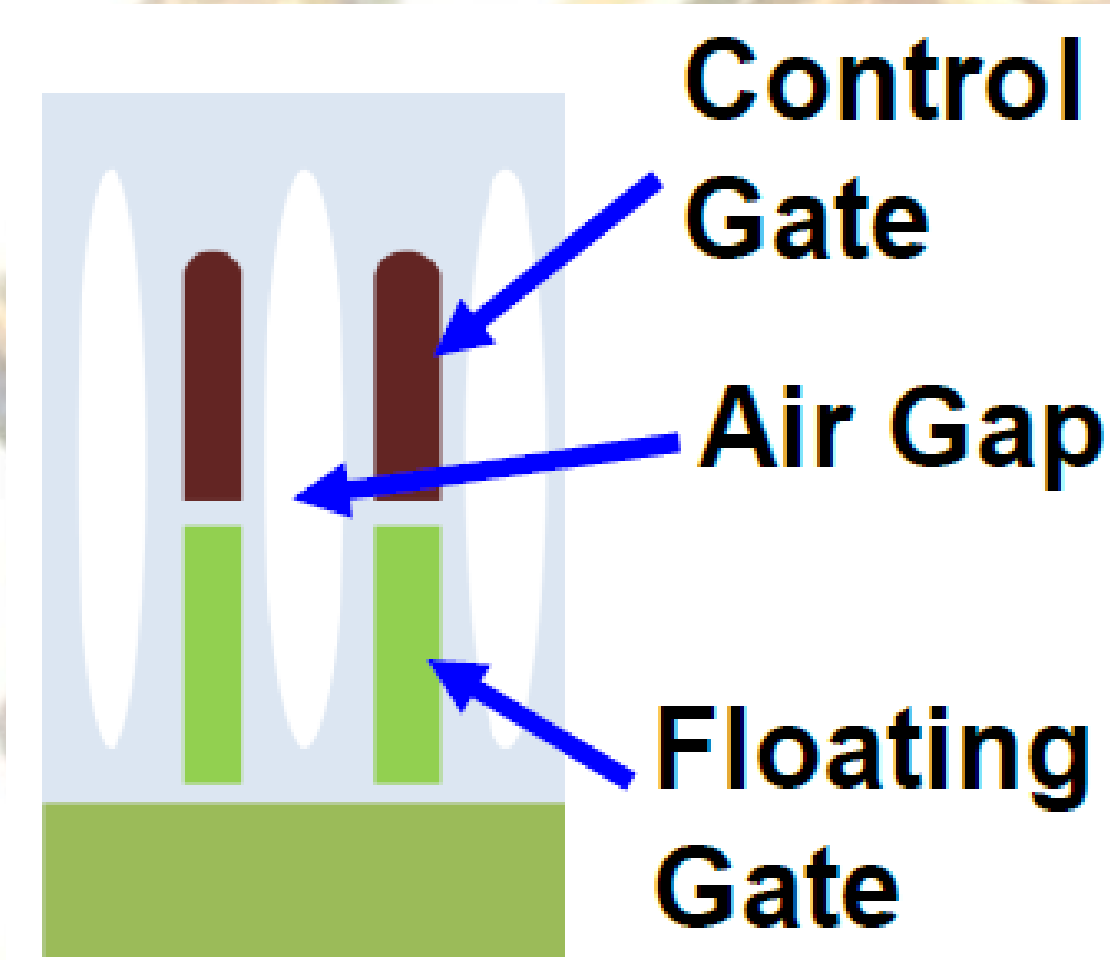
Capped Gate Maintains FG-CG Coupling



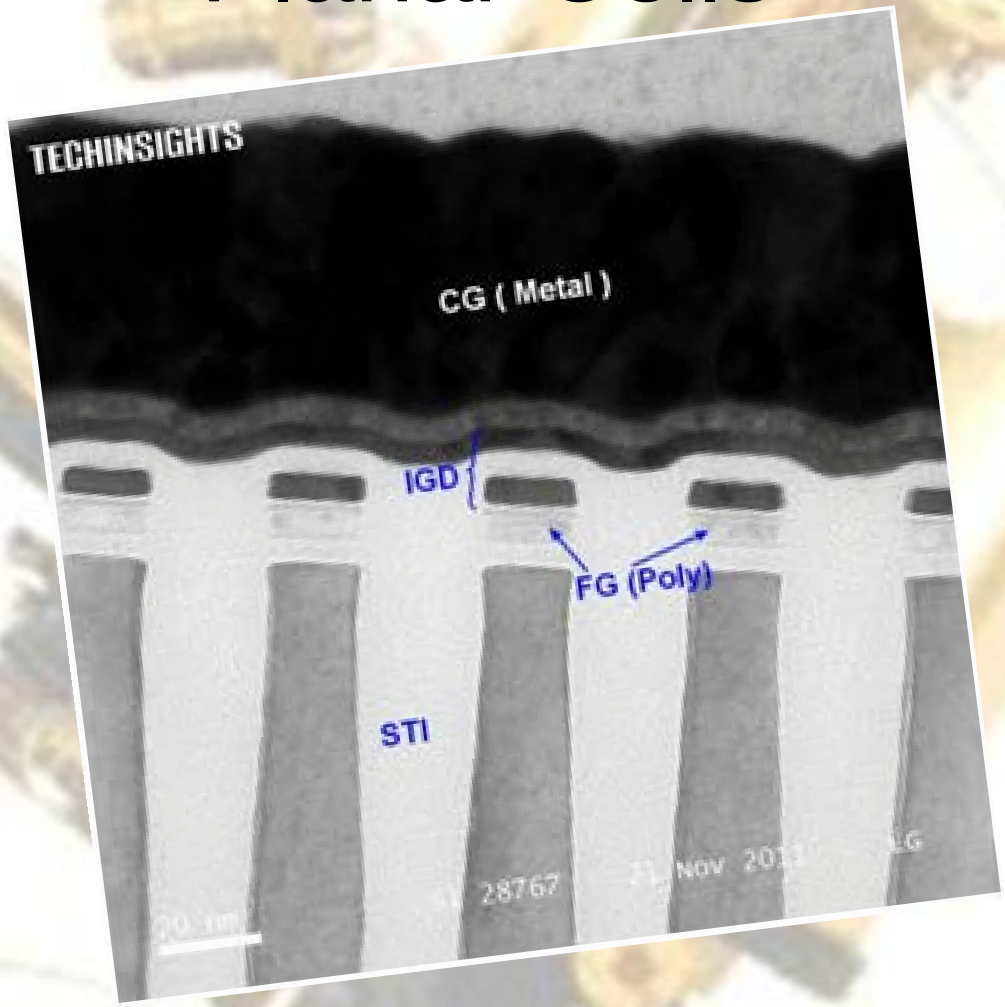
Capped Gate Scaling Challenge



Air Gaps Help Isolate FGs

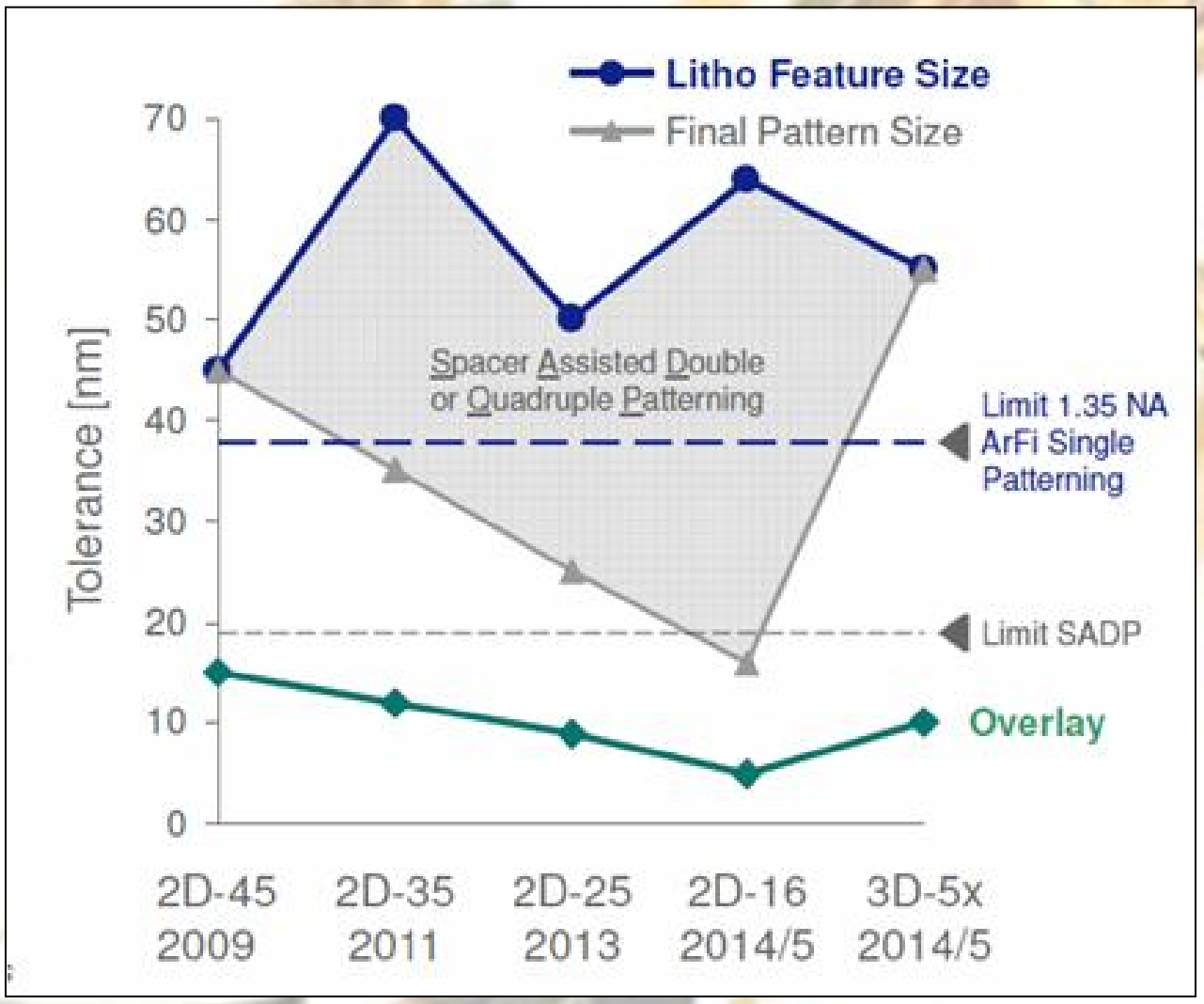


Hi-k Gate Dielectrics Support Planar Cells



But That's Not All That's Hard!

Quadruple Patterning



 Source: ASML

Agenda

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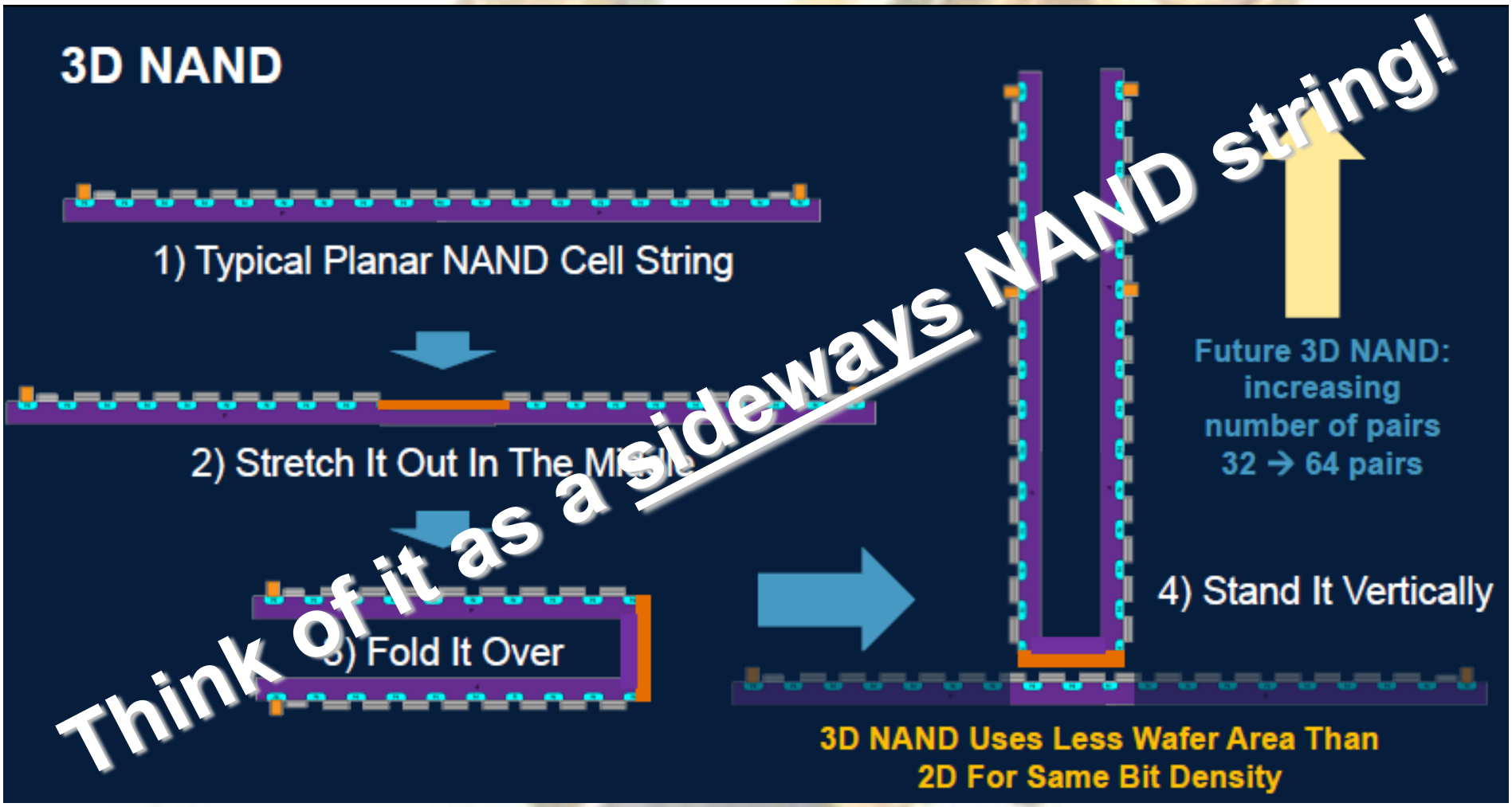
  - 3D structures
  - When will NAND die off?
- How will this impact designers?

How Do They Make 3D NAND?

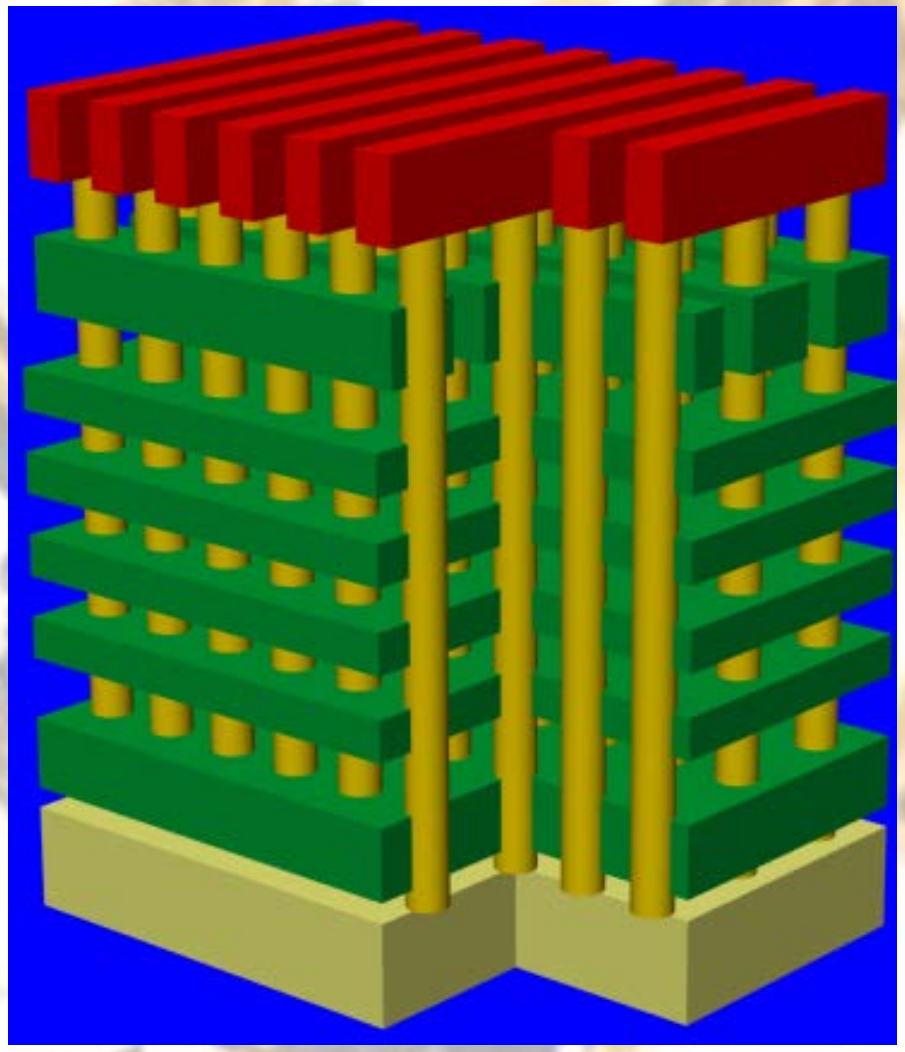
- It's a very complicated process
  - NAND strings made of thin-film transistors
  - Charge traps replace floating gates
  - Many production steps are totally new:
    - Vertical channels
    - 60:1 aspect-ratio holes
    - Polysilicon channels
    - Stairstep etch

One Way to Visualize 3D NAND



Source: Eteris

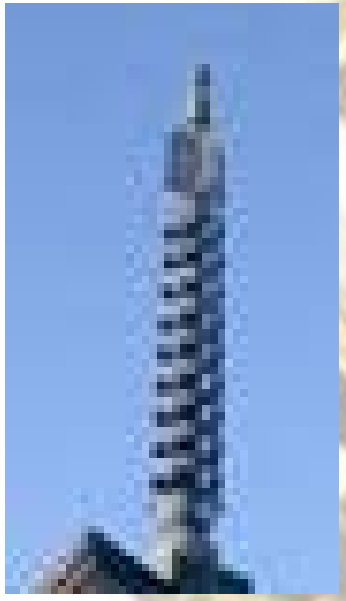
Toshiba's Initial BiCS 2007

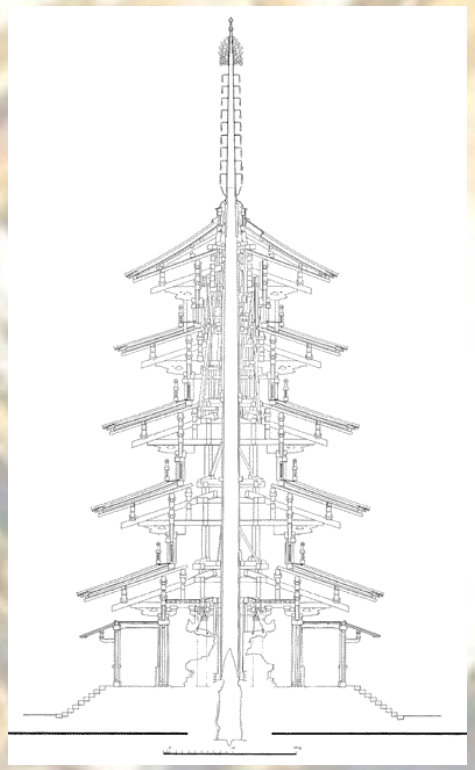


Source: Toshiba

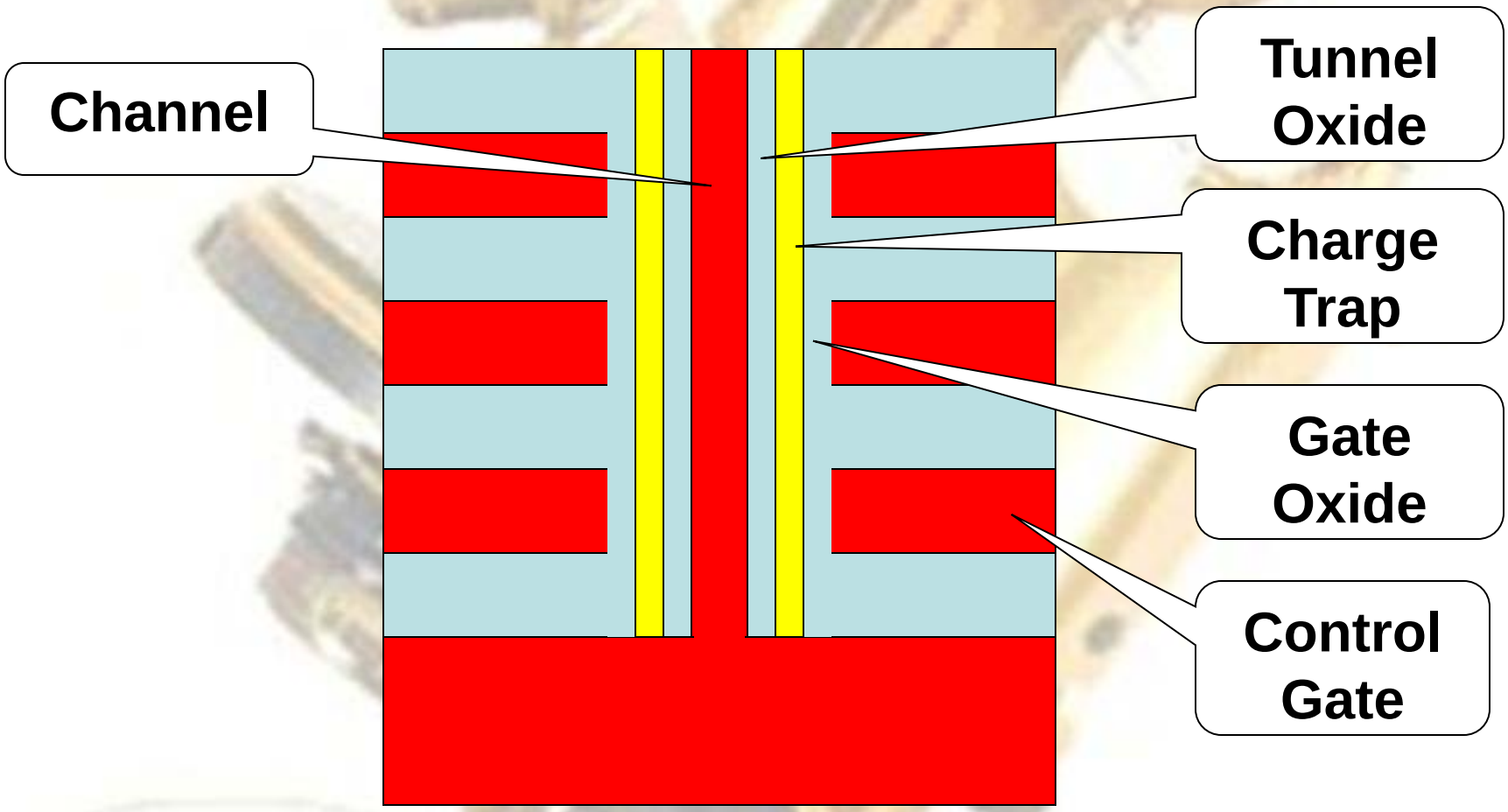
Naturally, 3D Is A Japanese Invention

東芝多重塔





Manufacturing BiCS



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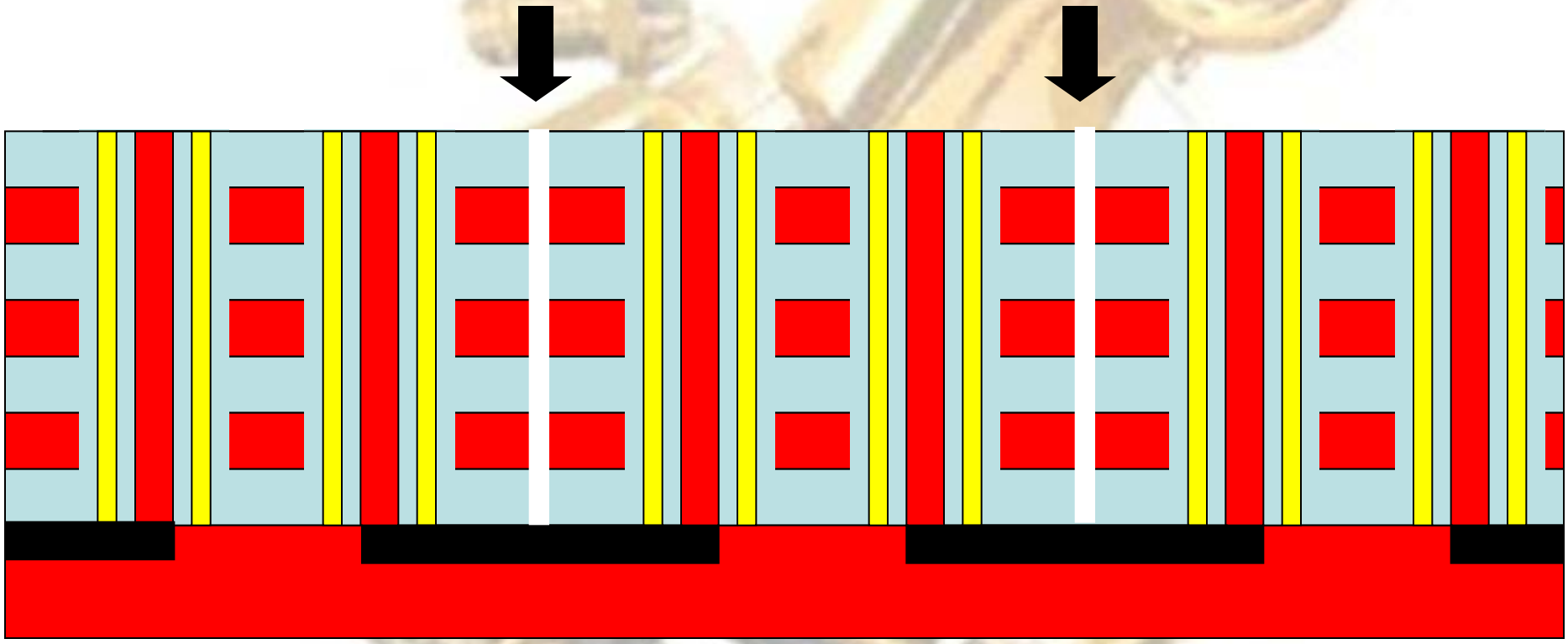
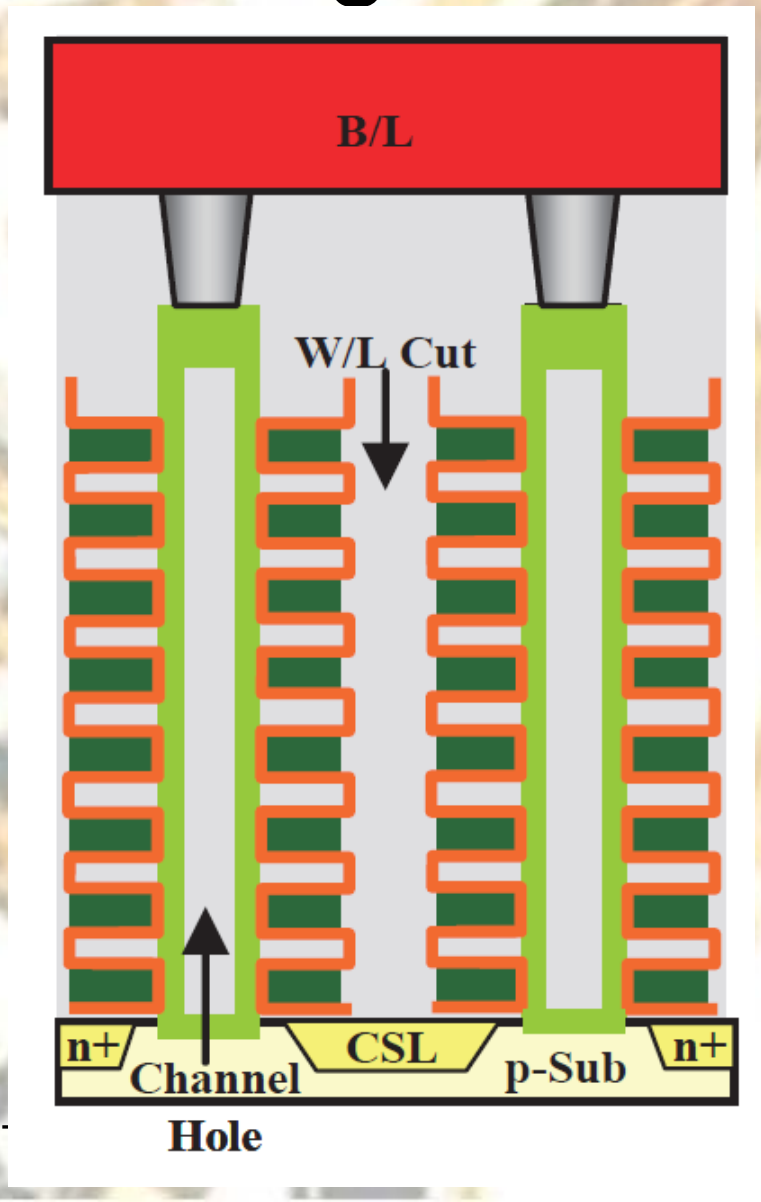
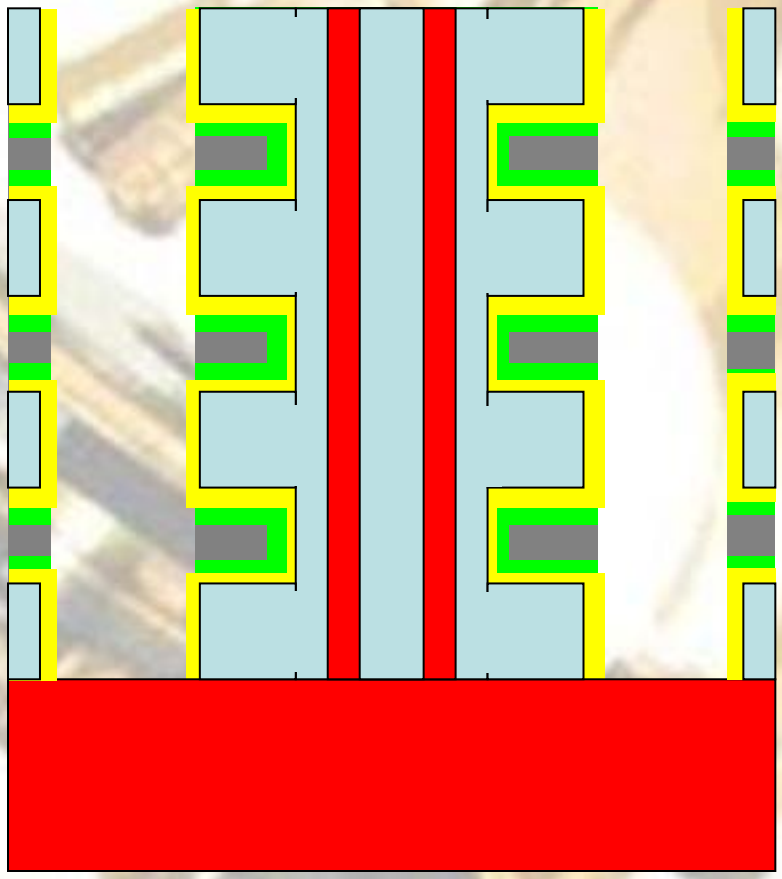


Samsung's TCAT

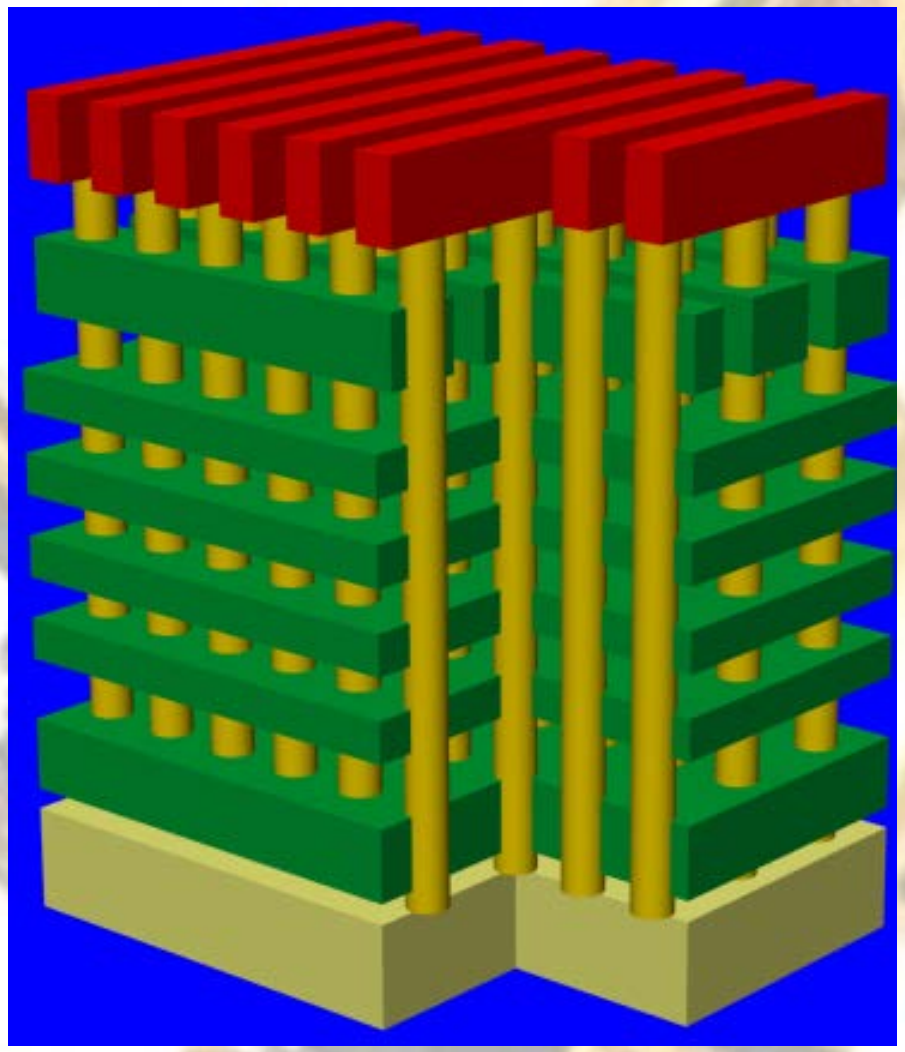


Source: Samsung

Manufacturing TCAT

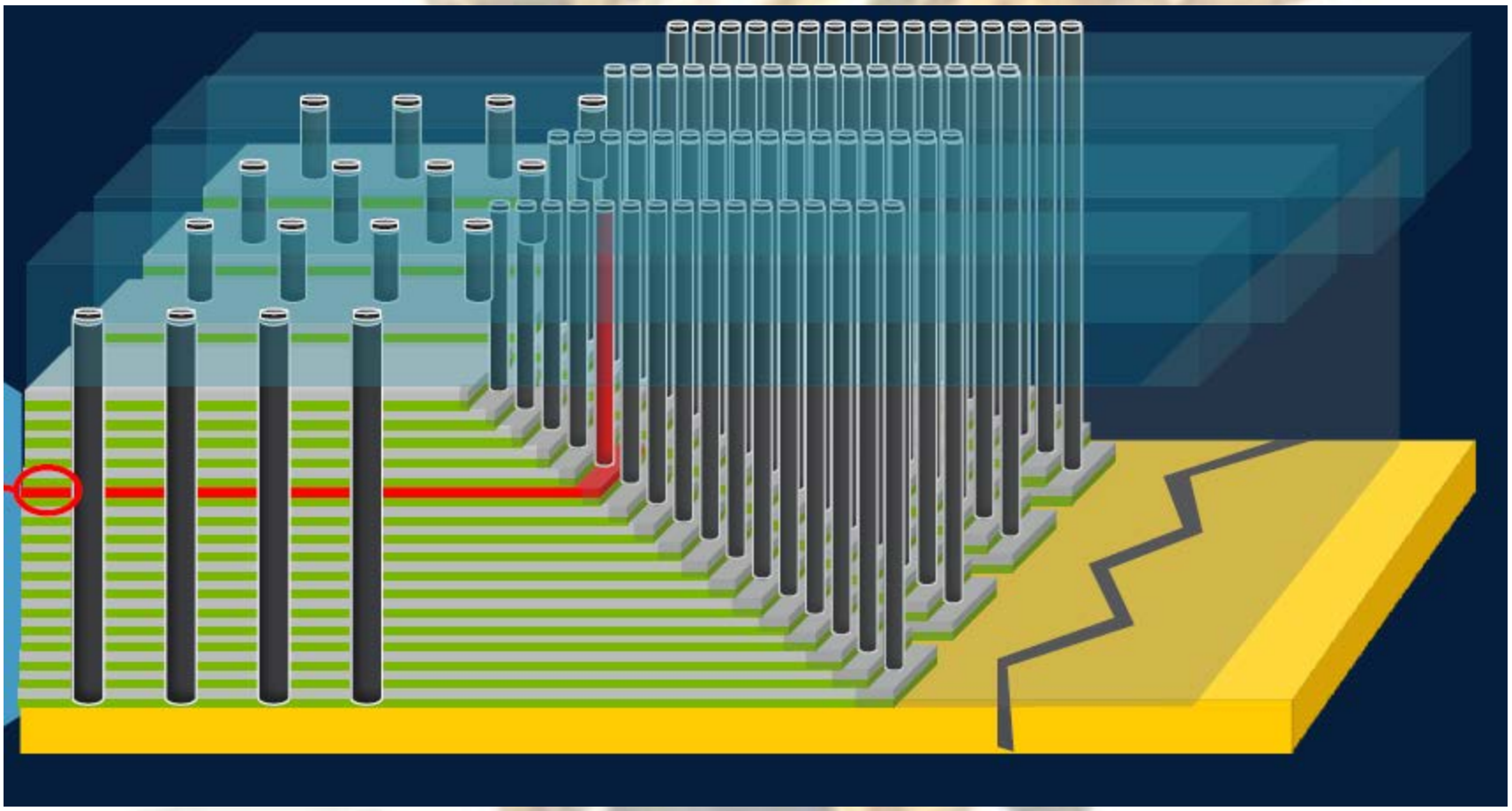


So Now You Have NAND Strings



How do you connect to the control gates???

Enter The Stairstep Process



Source: Eteris

Cutting The Stairstep

Like I Said Before:

"3D is a very complicated process!"

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A Timeline For Flash Obsolescence

- 2013: 1Ynm planar cell
  - Requires Hi-k gate dielectric
- 2015: 1Znm planar cell
  - May be the last planar cell
- 2017: 3D NAND in volume
- 2019: 3D – “The Next Generation”
- 2021: Final (?) 3D generation
- 2023: NAND yields to new technology

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Impact of New Memories

Summary

- Scaling planar NAND is hard
  - Making 3D NAND is even harder
- NAND will be here for a long time
  - No replacement before 2020
- When it's replaced our lives will change
  - Our customers, though, won't perceive that anything is any different!

Thank You!

Jim Handy

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