Non Volatile Memory Invades the Memory Bus: Performance and Versatility is the Result

A discussion on why and how Non Volatile Memory is moving onto the DDR bus and what it means for the industry, as well as the performance gains and versatility it brings with it.

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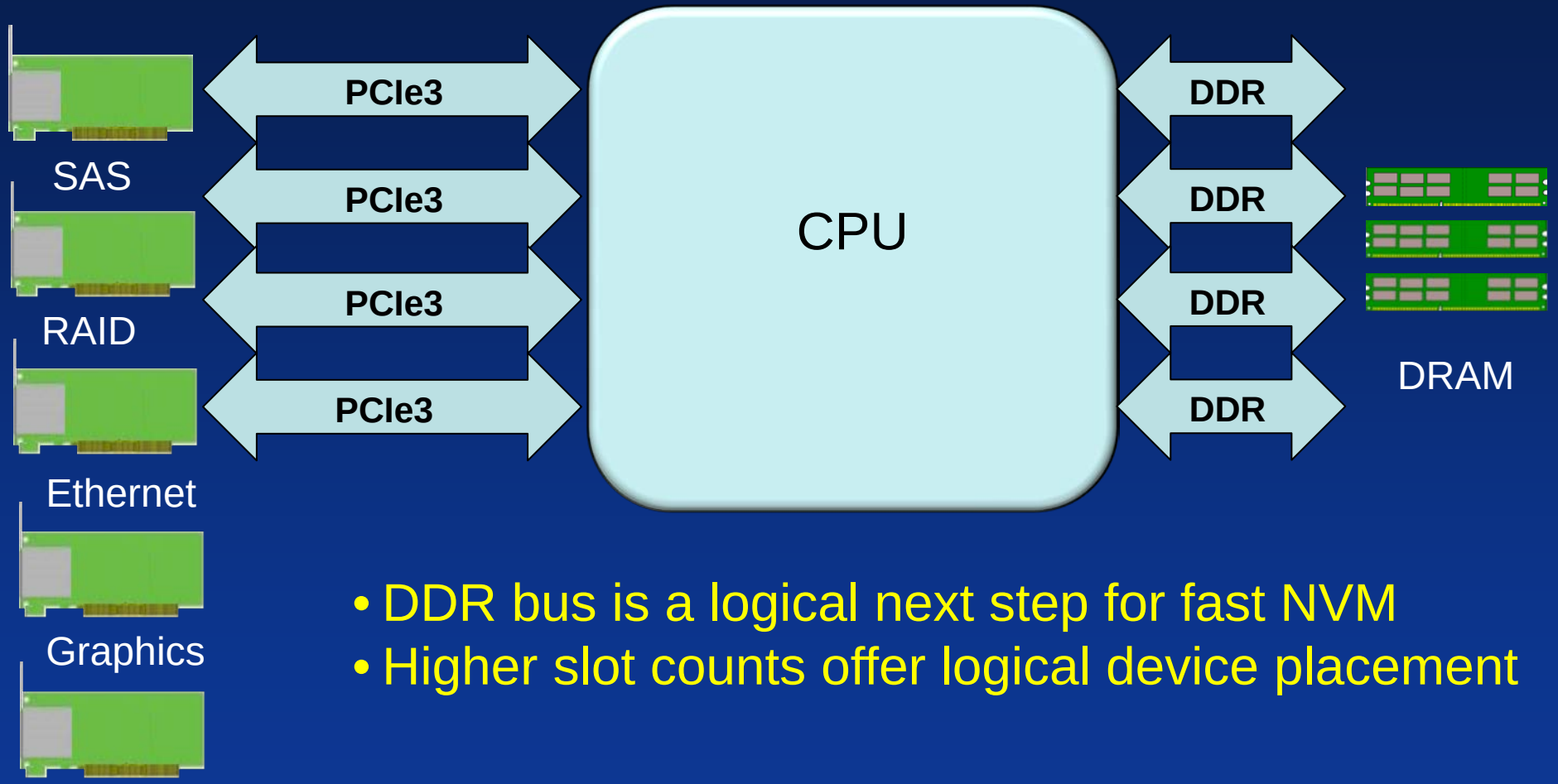
New Trend Seen in Flash Discussions

- Non Volatile memory on the DDR bus is a big topic of conversation these days
  - Why is this happening?
  - Methods?
  - What is the benefit to customers?

Before we start…..
How do we get data to the CPU?



- DDR bus is a logical next step for fast NVM
- Higher slot counts offer logical device placement

Why is This Happening?

- There are a limited number of data pathways to the CPU
  - PCIe
  - DDR
  - PCIe slots are limited in most cases at 2 to 10 slots
    - Most everything in one form or another will attempt to utilize them
    - RAID, SAS, Graphics cards and Ethernet contend for the same limited set of PCIe slots

- DIMM slots number from 24 to around 200
    - Dram is the only contention point for the slots
    - Large slot count allows for granular device approach
    - Aggregate solution possible comprised of small capacity devices with more controllers per GB of media

More Reasons……

- Aggregate storage targets gaining traction (fast small capacity devices)
  - provide granular approach to capacity needs and performance
  - Allow high ratio of controller versus flash while still allowing large capacity points
    - More then 700 IOPS per GB versus less then 100 for some shared storage enclosures
  - DDR3 aggregate solutions don’t require custom HW changes

- Recovery times for servers are large, driving a need for protection of data held in DRAM in event of power loss

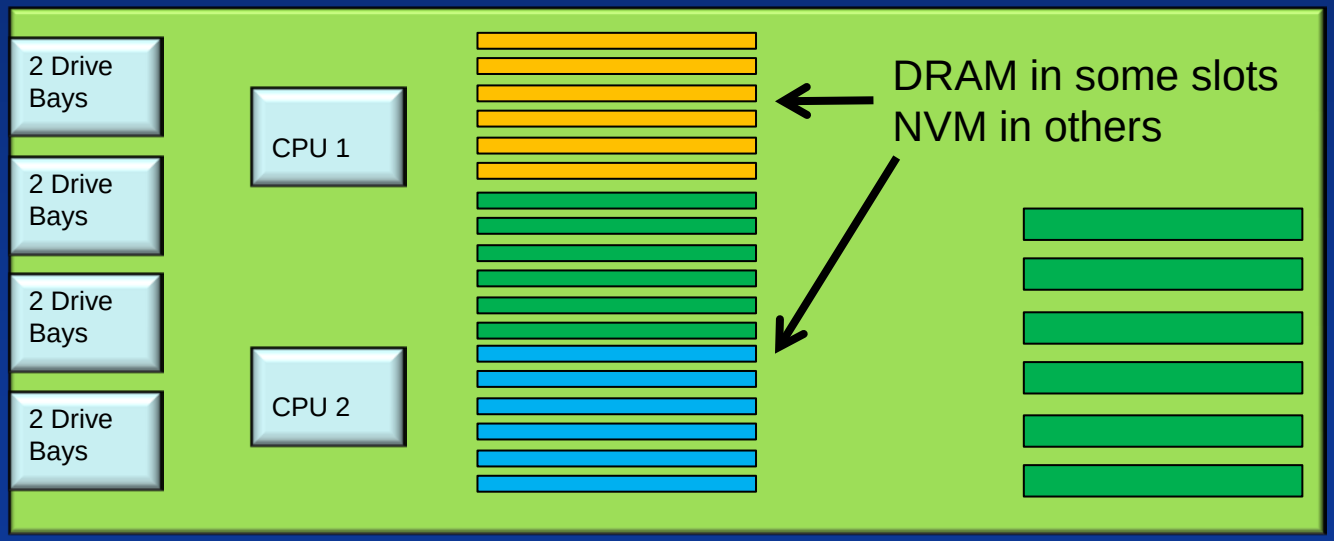
Methods

- Non volatile memory utilizing DDR slot and data path
  - Slower tier of main memory
  - Fast storage block device
- DRAM backed up with non volatile memory
  - DIMM has DRAM and non volatile memory on board
  - The DIMM has some power source to allow for backup at the point of failure
  - Device behaves like a normal DRAM
- Nonvolatile media in a flash slot but using alternate data path
  - DDR slot usage and power draw
  - SATA data path

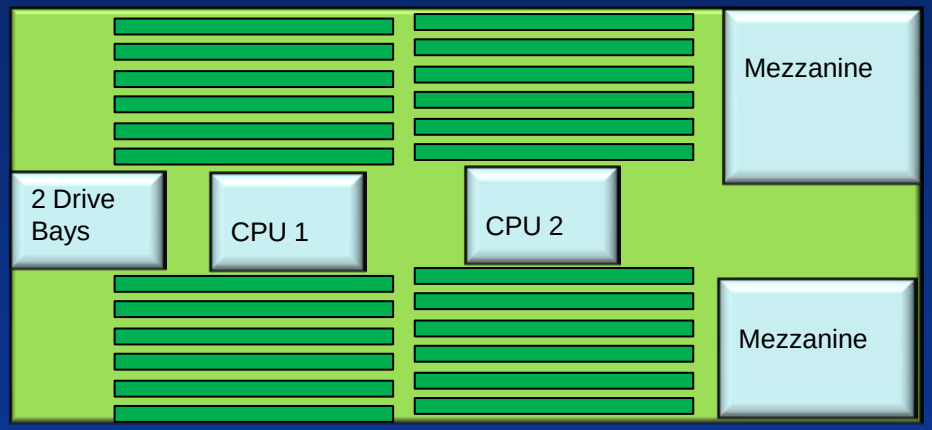
What is the Customer Benefit?

- NVM backed DRAM allows for quick recovery of unexpected power fails and could save UPS cost
  - Applications can be up and running quickly after system post with no need for DRAM to be reloaded or work lost to the last checkpoint

- Aggregated small capacity storage solutions provide granular approach to performance and capacity (Use what you need with small capacity increments with more efficiency)



What is the Customer Benefit?

- Blade form factors can now do more
  - Mezzanine slots can be used for ethernet and fibre channel
  - Front drive bays can be used for boot devices
  - Caching can utilize unused DIMMS slots
  - Databases can utilize unused DIMM slots
- 

- Capacity needs can now use cumulative PCIe and DDR3 based solutions
- Write latency on NVM block devices can now be lower without the need for DRAM and battery protection schemes

What is the Customer Benefit?

- Performance can scale linearly as each DDR slot is a separate data pipe
- Capacity needs can now use cumulative PCIe and DDR3 based solutions
- Write latency on NVM block devices can now be lower without the need for DRAM and battery protection schemes
- Fast but small capacity devices brought together in large numbers can bring very dense capacity and performance points.
  - Ex… (40) 400 GB Flash DIMM devices with a modest 150k IOPS each provide 6 million IOPs at a 16 TB capacity point
    - An 8 socket system with 192 DIMM slots would still have over 150 DIMM slots open for DRAM (or more NVM)

THANK YOU

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