



Carbon₂: Diablo Second Generation Architecture

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HISTORICALLY: *DYNAMIC MEMORY ISOLATED FROM PERSISTENT MEMORY*



Memory Segregation

- DRAM Closely Coupled With CPU
- Flash Accessed Via I/O Subsystem





MCS Coupled with Processor, Apps, System Memory Distance and Contention Issues Eliminated Data Stays Within Memory Subsystem for Local Access

- Achieves ultra-low latency
- Terabytes of local persistent memory

Enabled by a Unique Architectural Approach

- Provides highest I/O's at lowest latency
- As low as 3.3 microsecond writes





First Generation MCS Reference Design Kit

• Enables NAND Flash to directly interface with Memory Channel

Presents as a Block I/O Device

Managed just like other storage devices

DDR3 Interface, Standard RDIMM Form Factor

- Plugs into standard DIMM slots, no external connections
- IBM, Supermicro offering solutions





Second Generation MCS Goal

• Fast time-to-market & performance, functionality improvements

Enhancements

- DDR4 memory interface
 - Modular design allows low risk move to new interfaces
- NanoCommit[™] Technology
 - Allow DRAM persistence on nanosecond timescale to terabytes of flash memory
- MCS Processing Engine enhancements
 - Optimized processing capabilities with increased performance
 - Firmware changes for increased functionality, performance
 - NanoCommit[™] is first example, several others planned
 - Reduced latency even further (even lower than 3.3 microseconds!)



MEMORY CHANNEL STORAGE™: REFERENCE DESIGN KIT STRATEGY

Phase 1: MDK2 Development Kit

- FPGA based development kit
- Validate ASIC design
- Early prototyping
- UEFI, firmware, driver development

Phase 2: Carbon₂ Reference Design Kit

- ASIC reference design
- Full reference storage subsystem
- Linux, VMware, MS Windows drivers

Ecosystem Enablement

- OEM pre-qualifications
- ISV testing/optimizations, proof points
- Media architectural reviews







THANK YOU!

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