Understanding the Impact of Threshold Voltage on Flash Reliability and Performance

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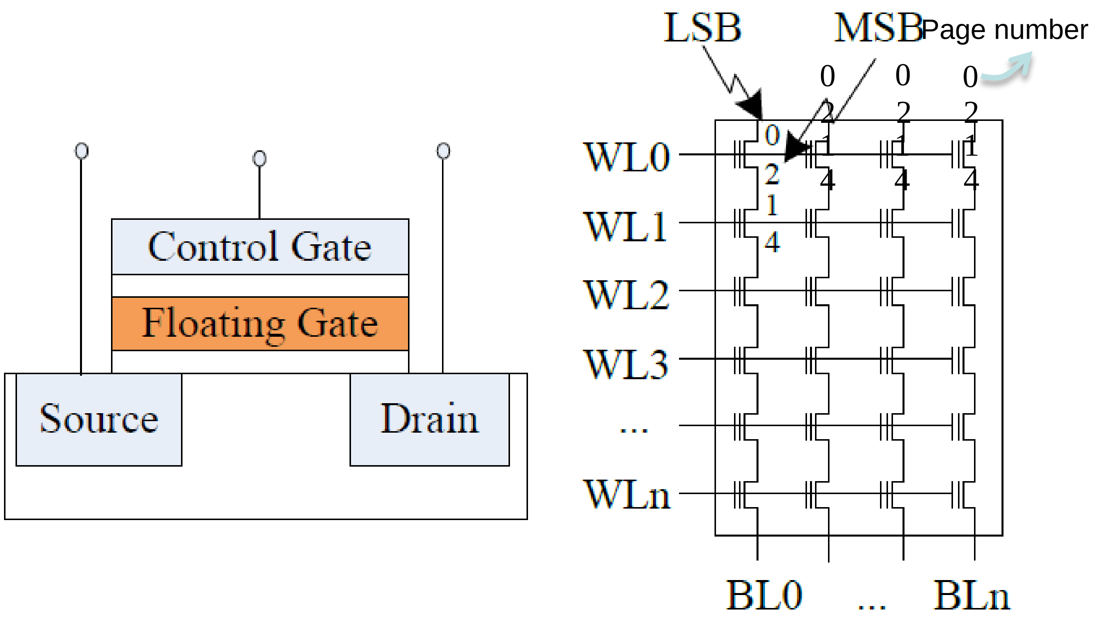
Outline

- Background and model analysis
- Threshold voltage reliability model
  - Testing methodology
  - Experimental results
  - Model establishment
- A case study: threshold voltage reduction

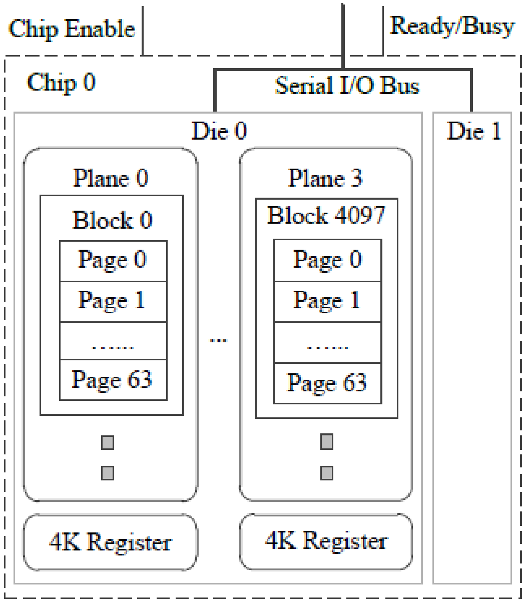
Summary

NAND Flash

- NAND flash based solid state drives (SSDs) have been largely adopted in supercomputing centers.



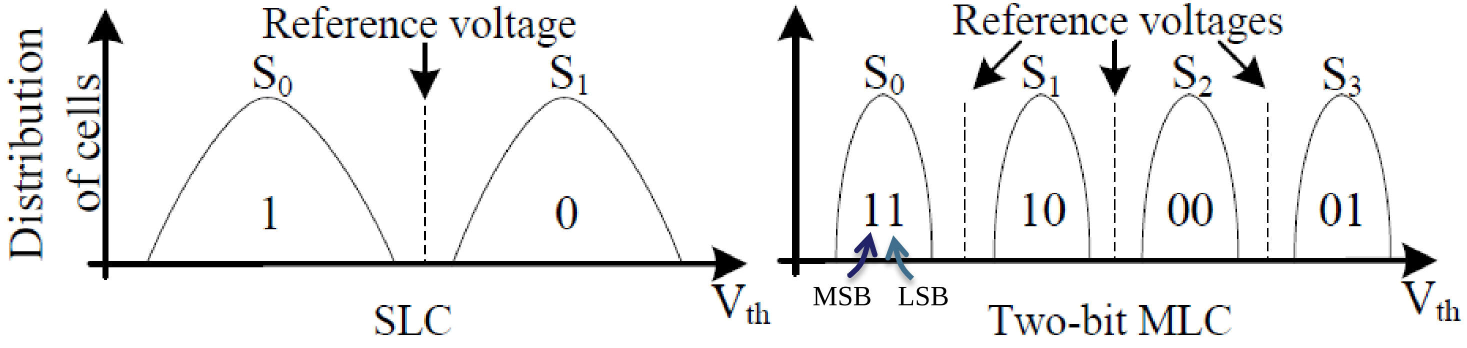
(a) Flash memory cell and block structure



(b) Flash memory

MLC Flash

- Flash memory uses threshold voltages to represent data information



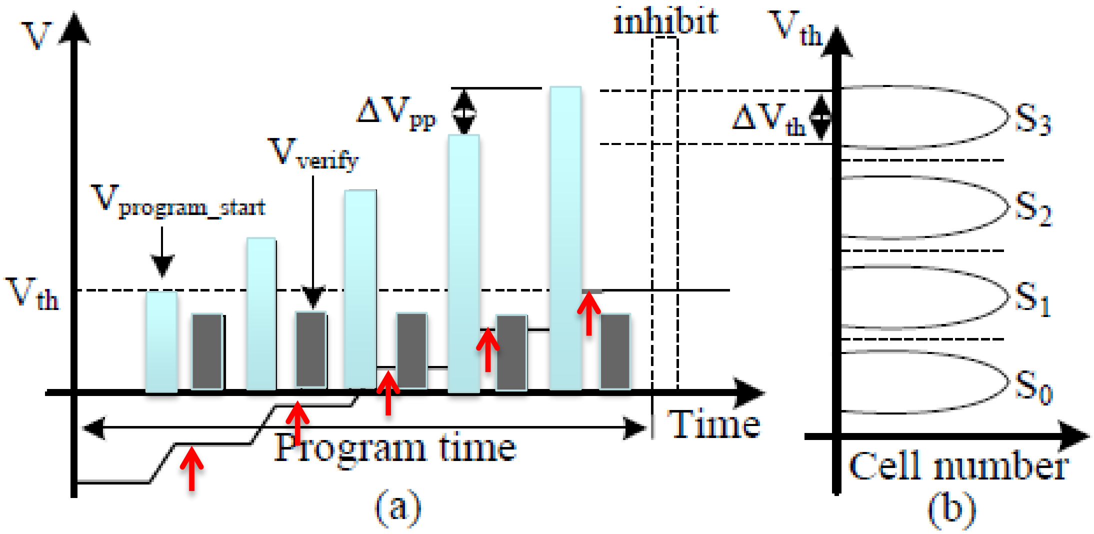
  - Each memory cell can store 2 bits data
  - A narrowed threshold voltage range
  - A shrunk memory cell size

Threshold Voltages

What is the impact of threshold voltages on flash performance and reliability?

ISPP(incremental step pulse programming)

- ISPP is a standard cell programming process



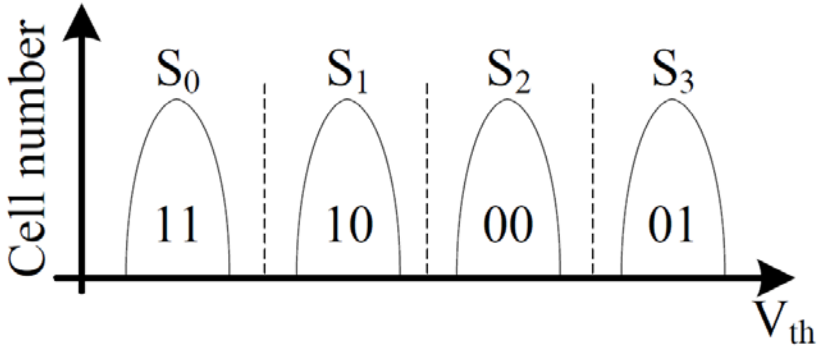
$$V_{th} = V_{start} + \beta \Delta V_{pp} N_s$$

N_s represent the number of programming steps;

β is a material related coefficient.

Threshold Voltage Distribution

- Cells are not identical
- Threshold voltages of cells programmed to the same state are different among cells

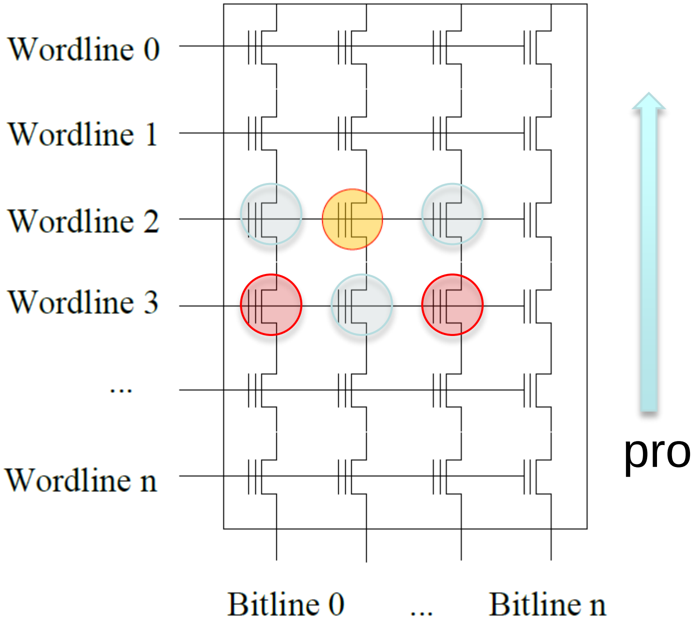


- Probability density function (Gaussian)

$$f(x) = \sum_{s=0}^{2^M-1} P(S_s)\frac{1}{\sqrt{2\pi}\delta_s}\exp\{\frac{-(x-\mu_s)^2}{2\delta_s^2}\}$$

  - $P(S_s)$ is the probability of being state S_s. In a 2-bit MLC $P(S_s) = 1/4$.

Cell-to-cell Interference



program

$$\Delta V_{th}^{(p,q)} = \gamma_{fg1}\Delta V_{th}^{(p,q+1)} + \gamma_{fg2}(\Delta V_{th}^{(p-1,q)} + \Delta V_{th}^{(p+1,q)})$$

Y_{fg1} and Y_{fg2} are the floating gate coupling ratios.

$$\Delta V_{th}^{(p,q)} = (\gamma_{fg1} + 2\gamma_{fg2})\Delta V_{th}^{\max}$$

If the maximum threshold voltage difference is reduced, the floating gate coupling effect is reduced.

Threshold Voltage Reliability Model

Testing Methodology

- Threshold voltage ←→ Reliability

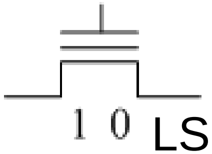
★ The threshold voltage of each state in a flash memory is fixed by its internal logic.

★ Each state (i.e., data pattern) represents a particular threshold voltage level.

○ We can control threshold voltage of a memory cell by programming different data patterns to it.

★ The number of bit errors per page

★



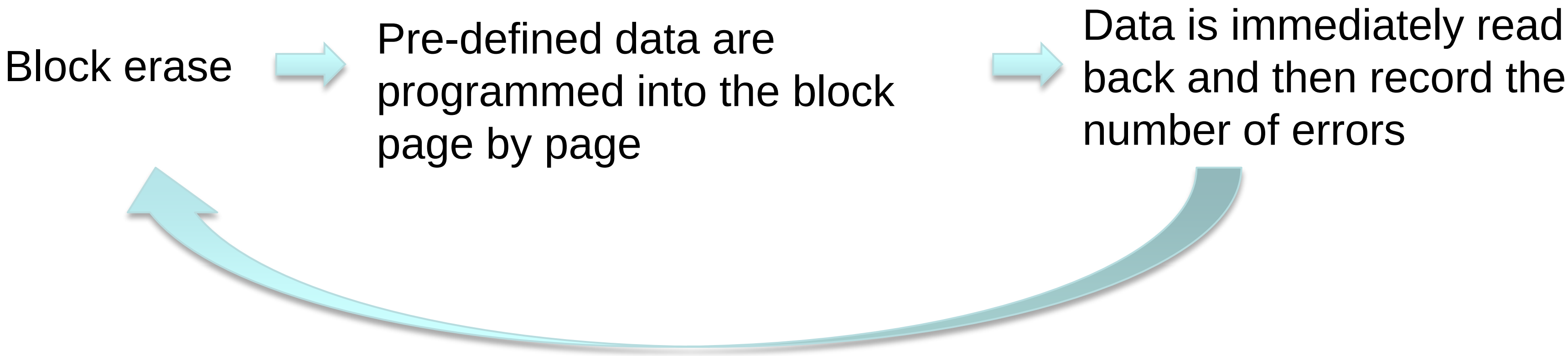
MSB page

LSB page

○ The number of errors per cell:
Any bit flip in a 2-bit cell is recorded as a cell error.

Erase/Programming Scheme (1/2)

- Cell errors are collected during every P/E (program/erase) cycle



Block erase

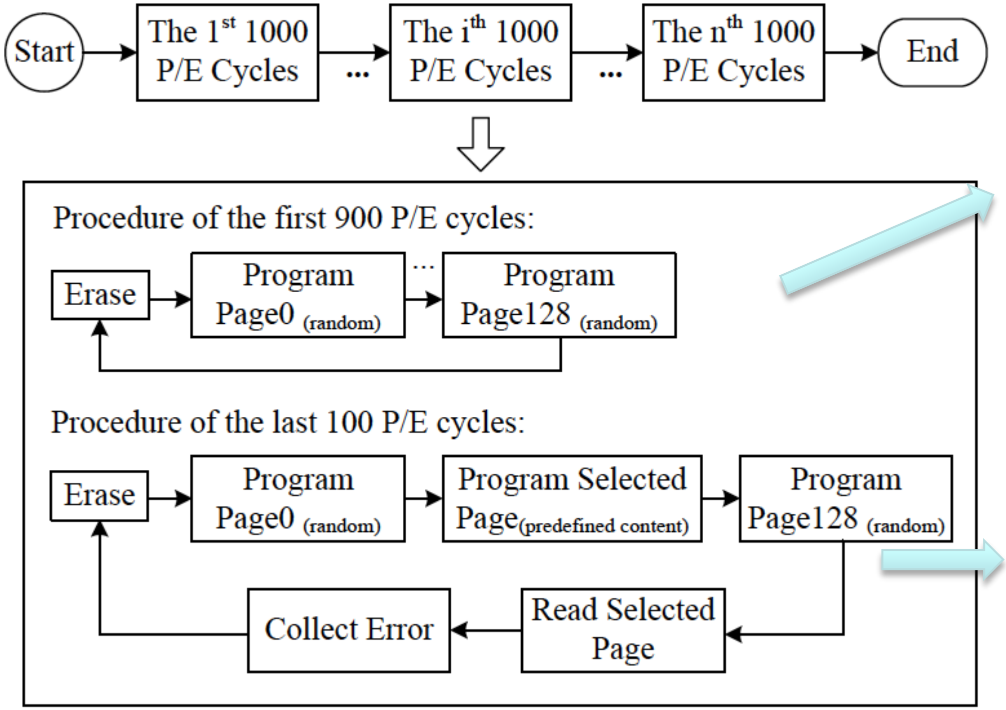
Pre-defined data are programmed into the block page by page

Data is immediately read back and then record the number of errors

Pre-defined data eliminate the cell-to-cell interference that exists in real applications

Erase/Programming Scheme (2/2)

- A revised P/E scheme



Start

The 1st 1000 P/E Cycles …

The ith 1000 P/E Cycles …

The nth 1000 P/E Cycles

End

Procedure of the first 900 P/E cycles:

Erase

Program Page0 (random) …

Program Page128 (random)

Procedure of the last 100 P/E cycles:

Erase

Program Page0 (random)

Program Selected Page(predefined content)

Program Page128 (random)

Read Selected Page

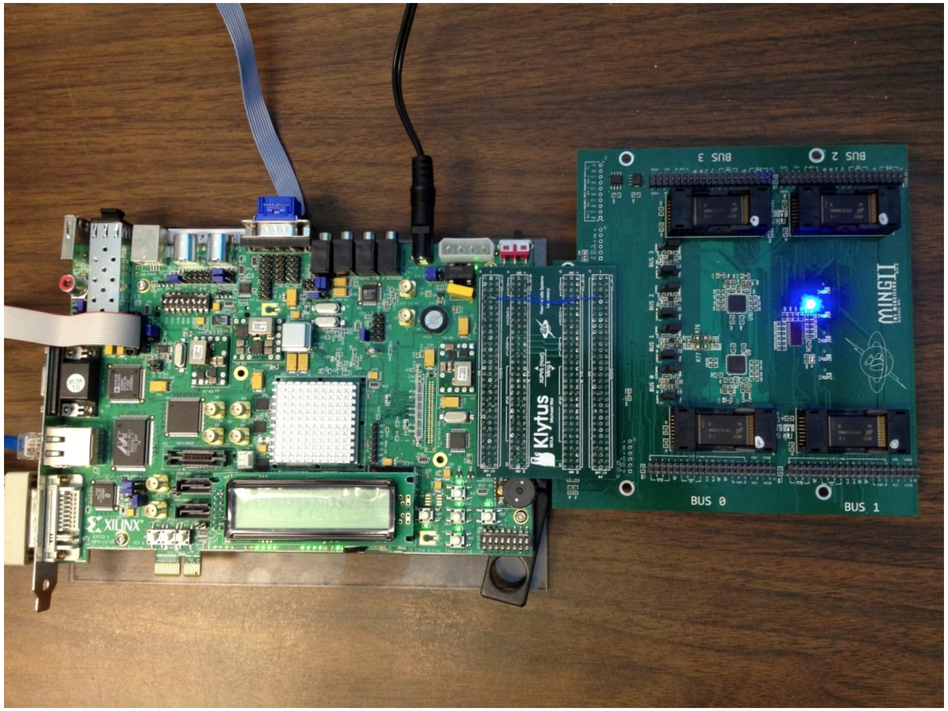
Collect Error

Only increase the accumulated threshold voltage for each page

Record cell errors

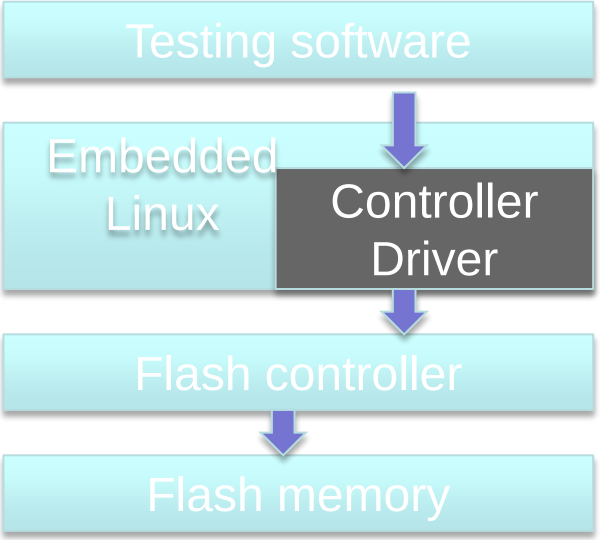
Hardware Platform

- Xilinx Xupv5-Lx110t evaluation board
- Ming II flash daughter board



Software Stack

- Flash controller on FPGA, no ECC;
- Embedded Linux, 3.0 kernel version;
- A driver for controller;
- Testing software preforms the P/E scheme and count errors.



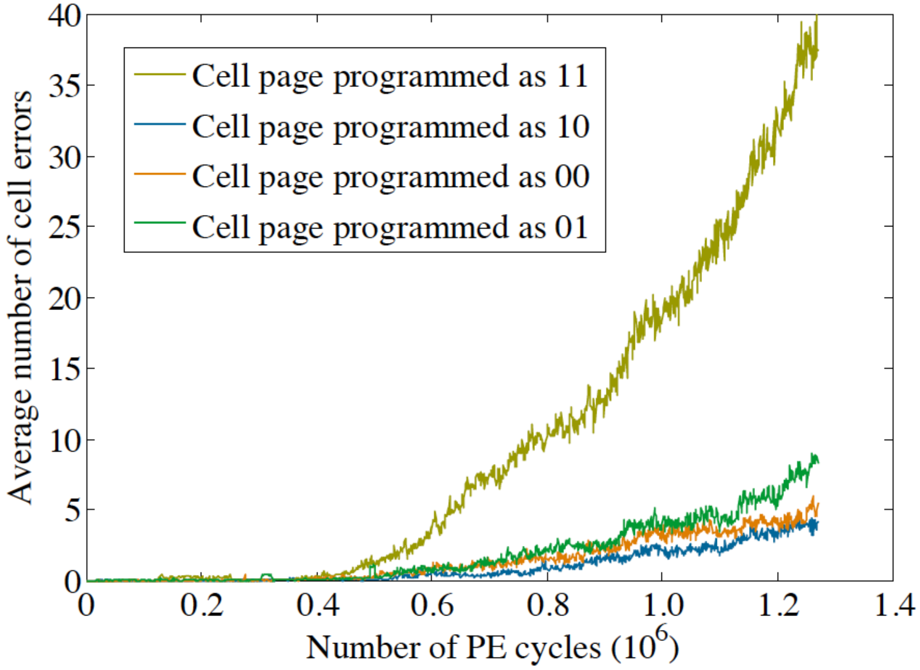
Experimental Results (1/2)

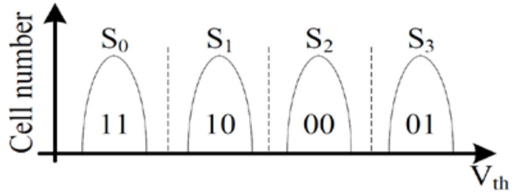
- Average number of cell errors in four cell pages

(1) The number of cell errors increases as the P/E cycles enlarge;

(2) The cell page programmed as ‘11’ exhibits the most unreliable characteristic;

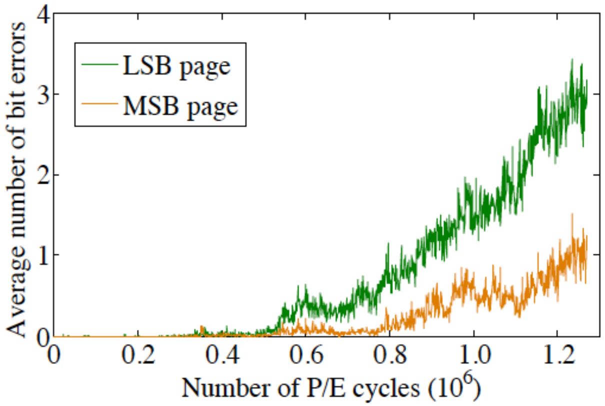
(3) Cell pages programmed to a higher voltage incur more errors as the P/E cycles enlarge;



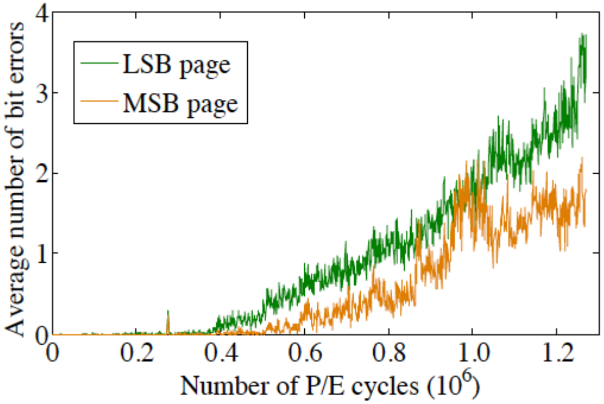


Experimental Results (2/2)

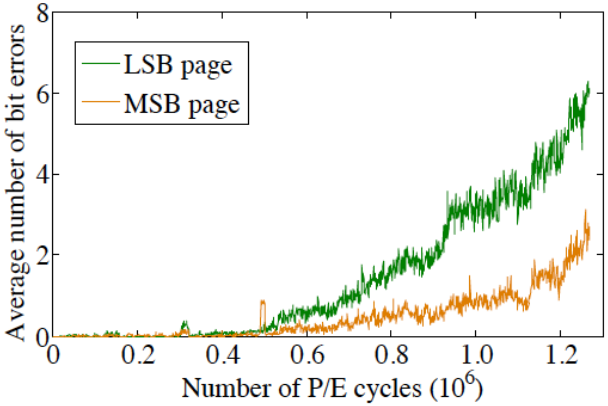
- Number of errors in LSB and MSB pages



(a) Cell page programmed as 10

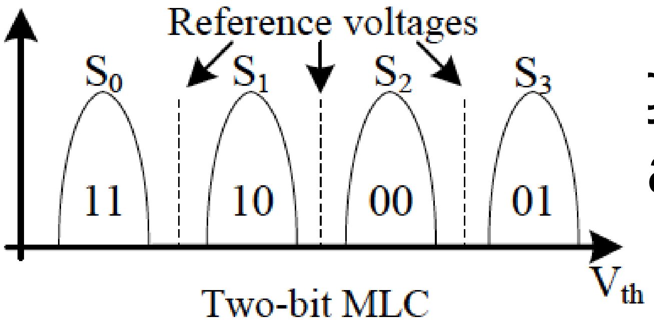


(b) Cell page programmed as 00



(c) Cell page programmed as 01

- LSB pages jer number of bit errors thar ages under all programmir



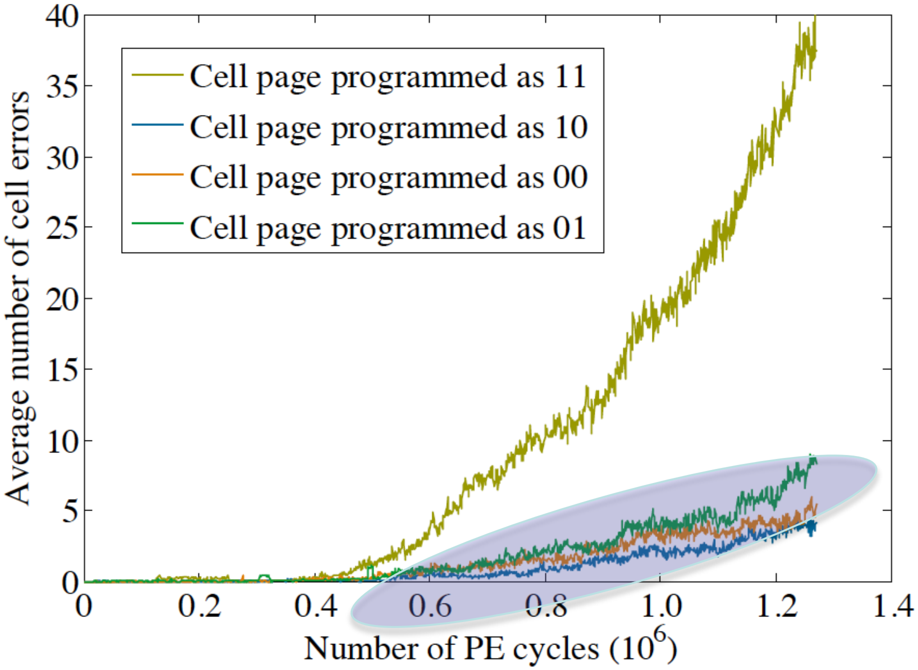
Two-bit MLC

Model Establishment (1/4)

- Consider the three programming states

- Use the nonlinear least square fitting method

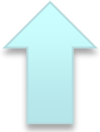
- Compared the exponential-law model, degree 2, 3, and 4 polynomial model



Model Establishment (2/4)

- Model errors (mean square deviation) comparison

Cell page	Exponential-law	Degree 2 polynomial	Degree 3 polynomial	Degree 4 polynomial
’10’	14.619	16.784	20.276	215.551
’00’	9.628	14.482	16.646	74.392
’01’	8.442	7.934	13.436	15.571



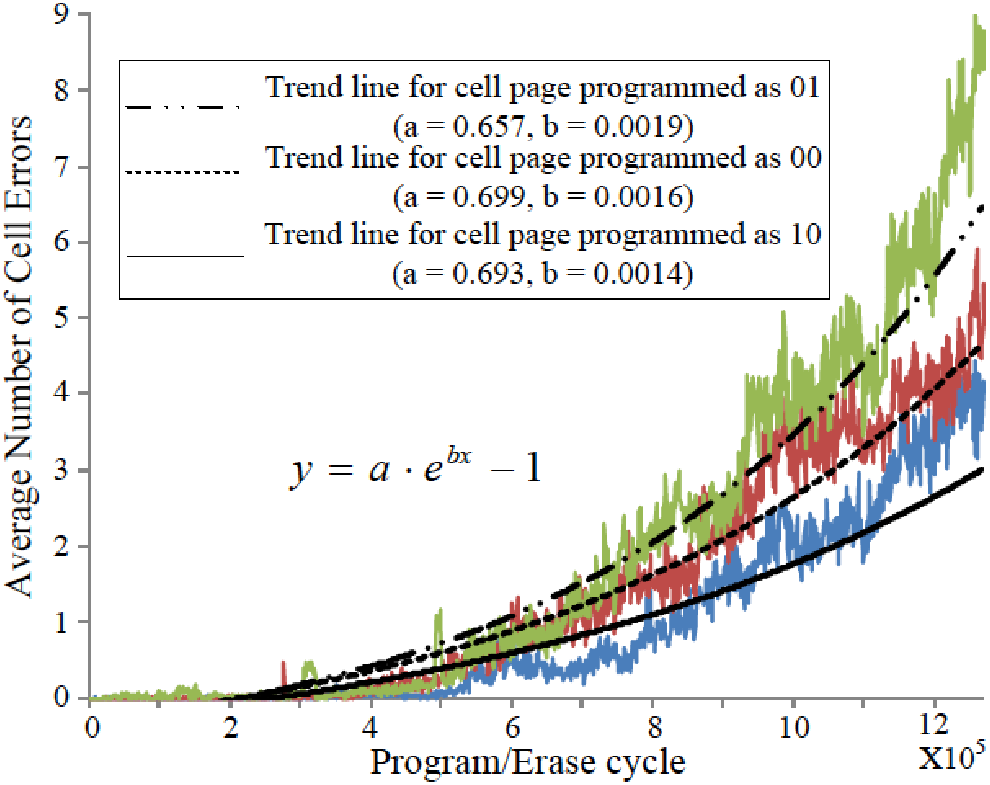
Best choice

Model Establishment (3/4)

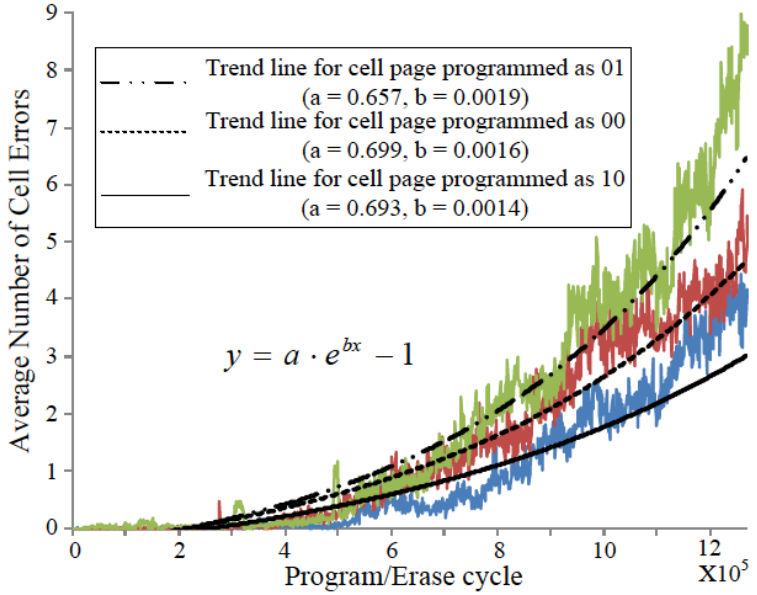
- Parameter fitting
  - Find a set of *a* and *b*
- As each pair of *a* and *b* represent a state (i.e., V_{th})

$$a = -5E^{-4}\ln(V_{th}) + 0.0019$$

$$b = 0.036\ln(V_{th}) + 0.6616$$



Model Establishment (4/4)



$$Err = (-5E^{-4}\ln(V_{th}) + 0.0019)e^{(0.036\ln(V_{th}) + 0.6616)N} - 1$$

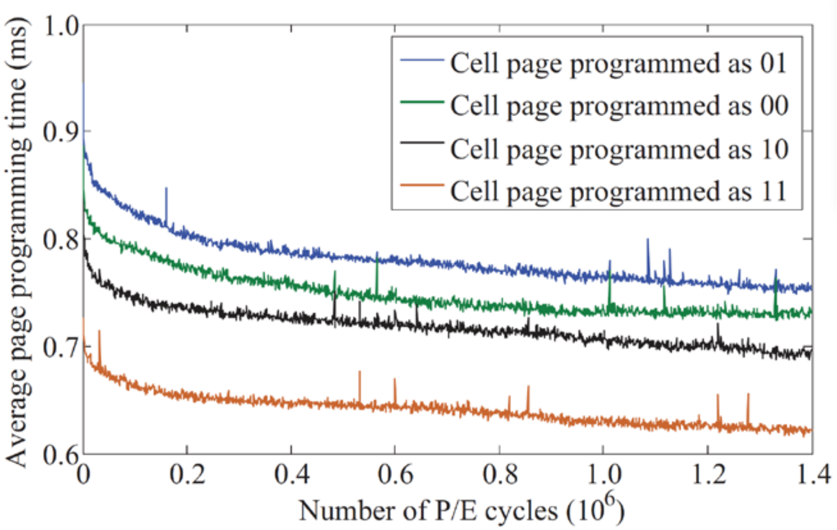
General Form:

$$Err = (\alpha_1 \ln(V_{th}) + \beta_1)e^{(\alpha_2 \ln(V_{th}) + \beta_2)N} - 1$$

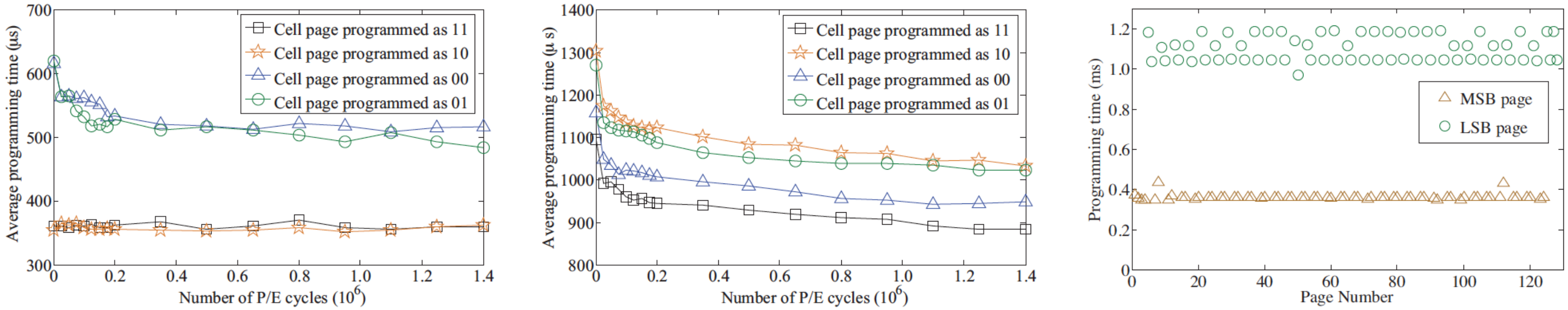
The α_1, β_1, α_2, and β_2 are determined by the characteristics of a flash memory

Page Programming (1/2)

- Pages programmed to a lower threshold voltage have a better programming performance.
- The programming time decreases as the number of P/E cycles increases.



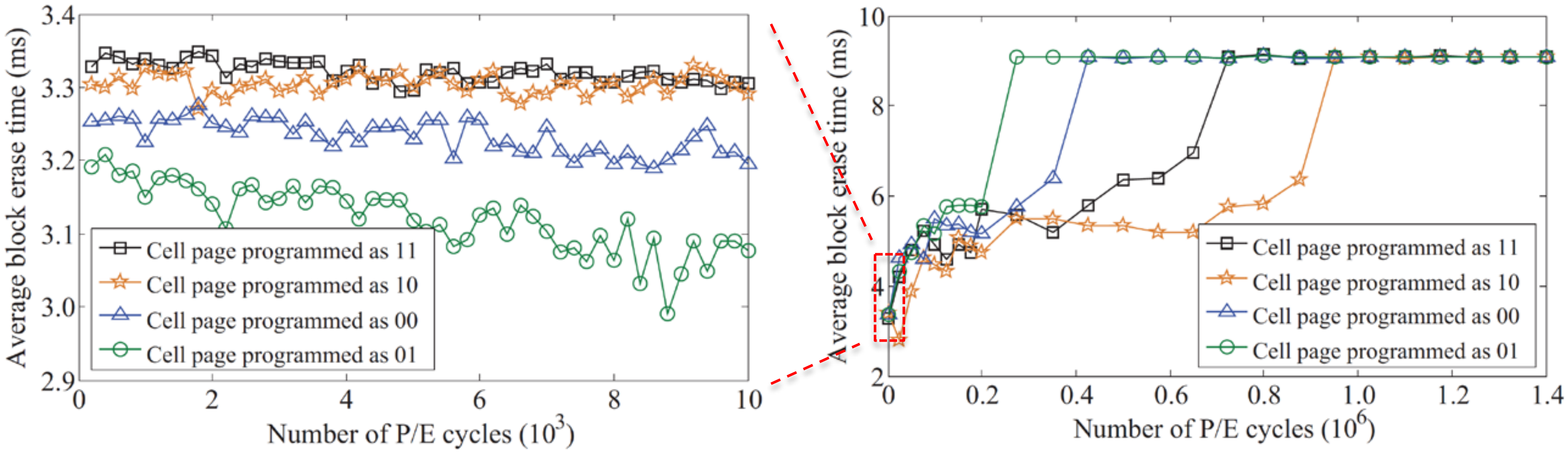
Page Programming (2/2)



(a) MSB page programming time (b) LSB page programming time (c) Page programming time in a block

- Programming speed of an MSB page is much faster than that of an LSB page.
- Programming time of MSB pages that are programmed as ’00’ and ‘01’ is 1.42 times longer than that of MSB pages programmed as ’11’ and ’10’.
- MSB pages have almost the same programming time, whereas the programming time of LSB pages varies substantially.

Block Erase



- In flash’s early lifetime, blocks programmed to a higher threshold voltage have a shorter erase time.
- The erase time increases to 9 *ms* when flash comes to the end of its lifetime.

A Case Study:
Threshold Voltage Reduction

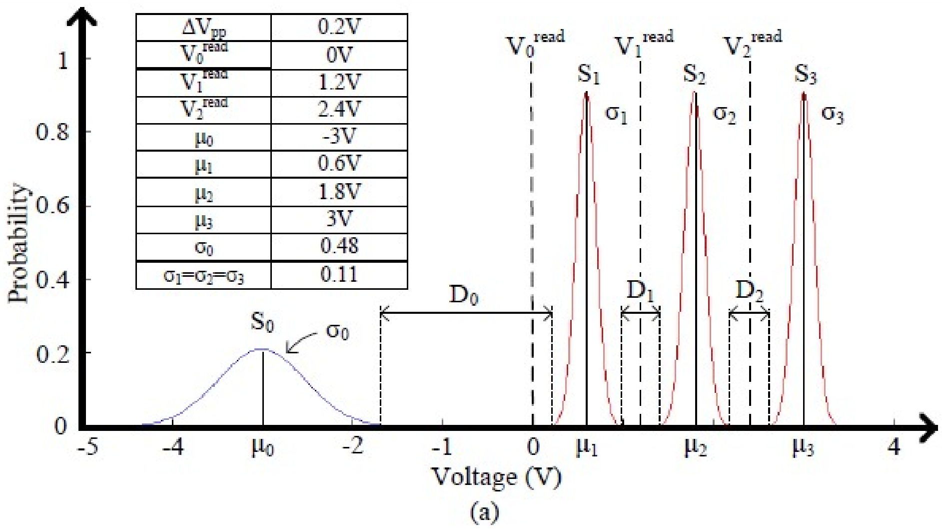
A Case Study

- The value of threshold voltage influences flash reliability and performance.

- Why not reducing the threshold voltages of each state in an MLC flash memory?

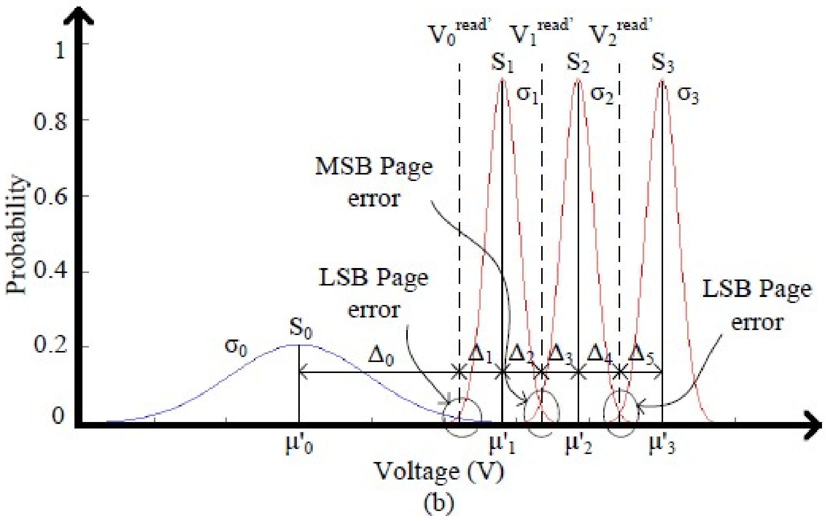
- We propose the Threshold Voltage Reduction (TVR) approach by reducing the margin between two adjacent states.
  - Performance and reliability ⇧

Threshold Voltage Reduction



ΔV_{pp}	0.2V
V_0^{read}	0V
V_1^{read}	1.2V
V_2^{read}	2.4V
μ_0	-3V
μ_1	0.6V
μ_2	1.8V
μ_3	3V
σ_0	0.48
$\sigma_1=\sigma_2=\sigma_3$	0.11

(a) A normal V_{th} distribution.



(b) A TVR applied V_{th} distribution.

(b) Shows an extreme case that the width of all the three margins are shrunk to zero. (retention free)

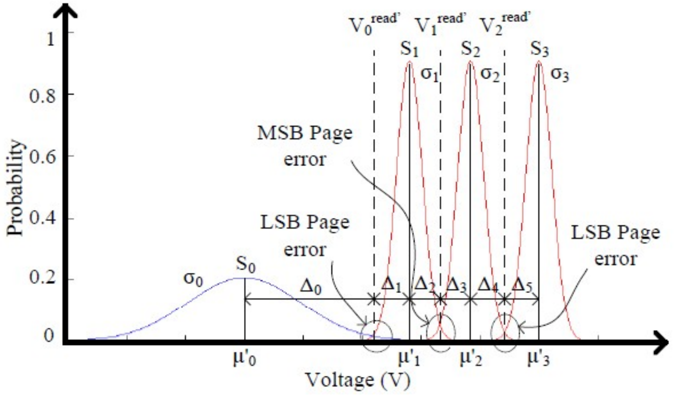
TVR Analysis(1/3)

- The probability that the voltages of cells cross the read reference voltage can be calculated by the tail probability function.

$$RBER_{MSBpage} = \frac{1}{4} Q_1\left(\frac{|\Delta_2|}{\delta_1}\right) + \frac{1}{4} Q_2\left(\frac{|\Delta_3|}{\delta_2}\right)$$

$$RBER_{LSBpage} = \frac{1}{4} Q_0\left(\frac{|\Delta_0|}{\delta_0}\right) + \frac{1}{4} Q_1\left(\frac{|\Delta_1|}{\delta_1}\right) + \frac{1}{4} Q_2\left(\frac{|\Delta_4|}{\delta_2}\right) + \frac{1}{4} Q_3\left(\frac{|\Delta_5|}{\delta_3}\right)$$

$Q_s(x)$ is the tail probability function of each state.

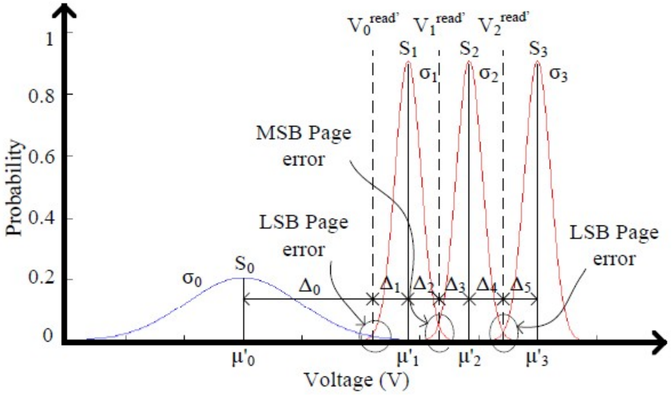


TVR Analysis(2/3)

- To simplify the computation, we assume that a forward state change and a backward state change have the same probability.

$$Q_1\left(\frac{|\Delta_2|}{\delta_1}\right) = Q_2\left(\frac{|\Delta_3|}{\delta_2}\right)$$

$$Q_0\left(\frac{|\Delta_0|}{\delta_0}\right) = Q_1\left(\frac{|\Delta_1|}{\delta_1}\right) = Q_2\left(\frac{|\Delta_4|}{\delta_2}\right) = Q_3\left(\frac{|\Delta_5|}{\delta_3}\right)$$

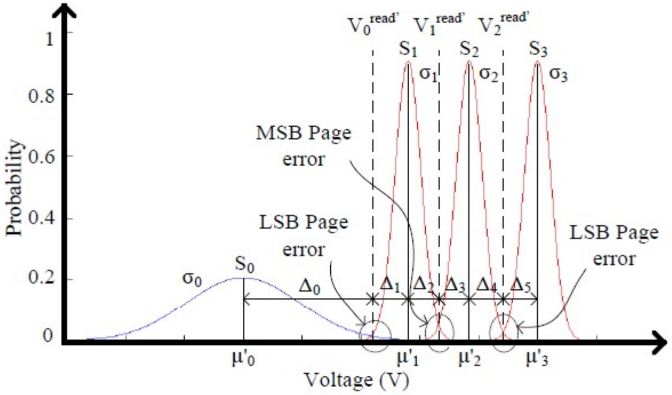


TVR Analysis(3/3)

- For modern flash memory, RBER must be lower than 4.5E-4 (industry standard).

$$\Delta_0 \approx 1.40; \Delta_1 = \Delta_4 = \Delta_5 \approx 0.36; \Delta_2 = \Delta_3 \approx 0.34$$

- The maximum threshold voltage that can be reduced is determined.



Programming Speed Improvement

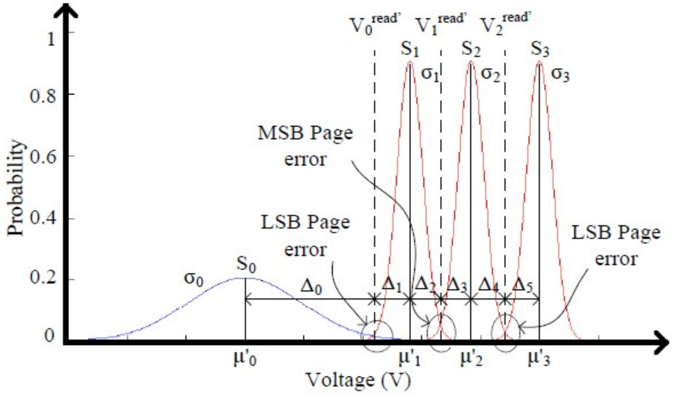
- Programming speed is determined by ISPP

$$V_{th} = V_{start} + \beta \Delta V_{pp} N_s$$

$$\lceil N_s \rceil = \frac{\Delta V_{th}}{\beta \Delta V_{pp}}$$

19 steps → 9.5 steps

Programming speed is improved by 50% on average.



Reliability Improvement

- Threshold voltage reliability model

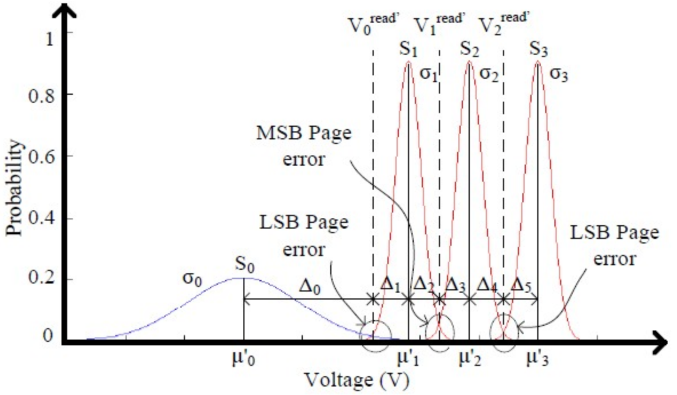
$$Err = (-5E^{-4}\ln(V_{th}) + 0.0019)e^{(0.036\ln(V_{th})+0.6616)N} - 1$$

RBER is lower than 4.5E-4

12.46E5 → 13.35E5 P/E cycles

Reliability is

improved by 7.1%.



Impact on SSDs (1/2)

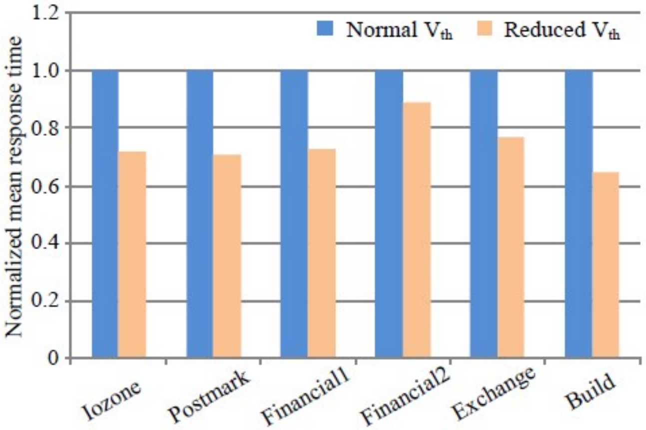
- DiskSim 4.0 and Microsoft SSD module
- Real-world traces (Financial 1, Financial 2, Iozone, and postmark)

Page size	Pages per Block	Blocks per Plane	Planes per Die	Dies per package	Package number
4 KB	64	2,048	4	2	4 – (4, 8)

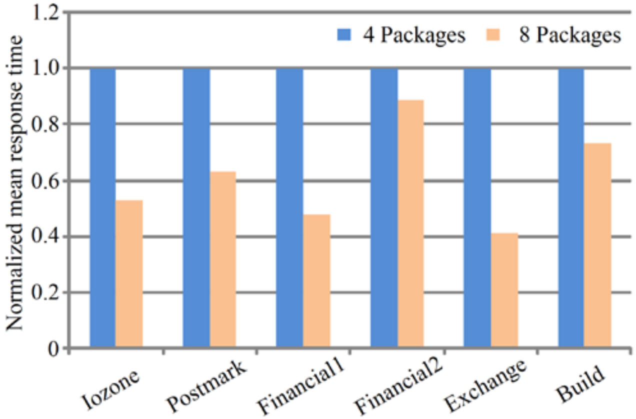
Block erase (µs)	Program (µs)	Read (µs)
2,000	200 – (100, 200)	20

Impact on SSDs (2/2)

- TVR can reduce SSD's overall mean response time by 11% to 35% (in a 4-channel example).



- When we increase the package parallelism from 4 to 8, the overall mean response time consistently decreases (in exchange the improvement is 59%).



Summary

- The threshold voltage in MLC plays a very important role in both flash performance and reliability.

- An empirical threshold voltage reliability model is established based on experimental results.

- A TVR approach that can improve flash performance and reliability is proposed.

Future Work

- Consider the data retention requirement and improve the TVR approach.

- Reducing the average programming voltage level by transforming high threshold voltage data patterns into low threshold voltage date patterns.

Acknowledgements

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Questions?