Noise Modeling and Capacity Analysis for NAND Flash Memories

Qing Li, Anxiao (Andrew) Jiang and Erich F. Haratsch

July 24, 2014

THE TEXAS A&M UNIVERSITY SYSTEM 1876

LSI

Outline

1 Motivation

2 Fundemantal concepts on flash memories

3 Channel Modeling for Errors in Flash Memories

4 Capacity analysis of flash memory

5 Conclusion and future work

1 Motivation

Flash memory is a significant nonvolatile memory technology

Flash memories are not reliable

- Noise/disturbs: retention error, cell-to-cell interference, program disturb, etc.

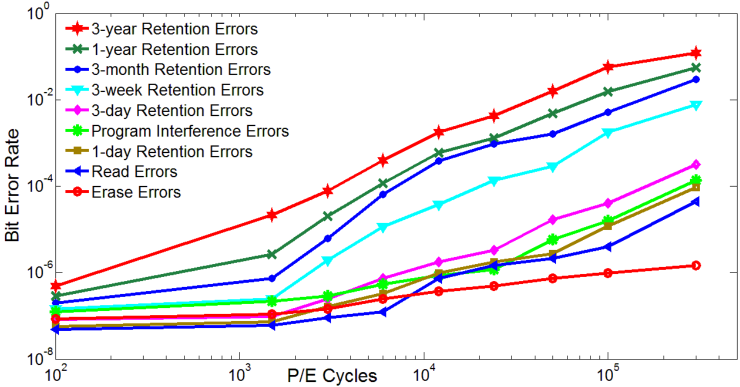


Figure 1: From Yu Cai et al, Carnegie Mellon University

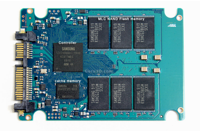
Contributions of this paper

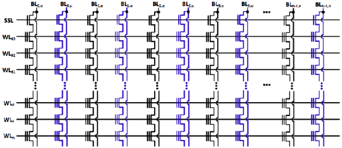
- Suvery noise and construct channel models.
- Analyse flash capacity under those models.
- Explore some useful schemes against noise.

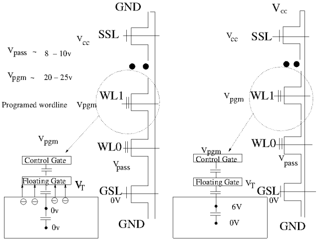
2 Fundemantal concepts on flash memories

The structure of flash memories

- Flash chip → · · · → flash block → flash page → flash cell.





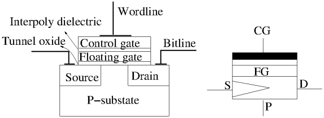


(a) Programming

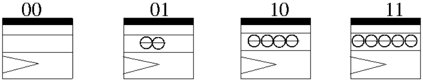
(b) Programming inhibit

Structure and operations of flash memory cell

- Flash memory cell and its representation used.

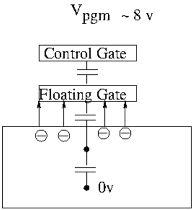


- Use electrons to represent data.

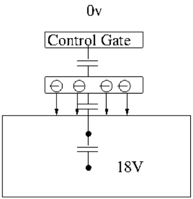


Flash memory cell operations

- Program/write: inject electrons to floating gate.
- Erase: remove electrons from floating gate.
- Read: measure the number of electrons in floating gate.



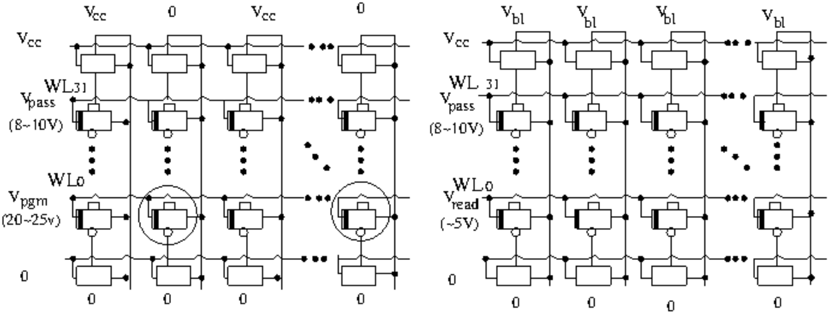
(a) Programming



(b) Erase

Structure and operations of flash memory array

- Program/read unit is a page.
- Erasure unit is a block.

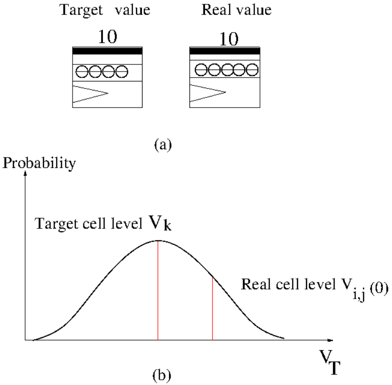


(a) Program

(b) Read

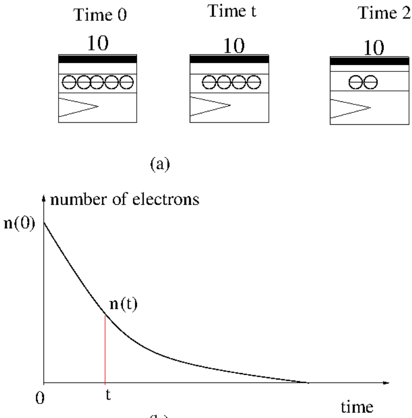
3 Channel Modeling for Errors in Flash Memories

Inaccurate programming



- $Z_k = V_{i,j}(0) - V_k$, $Z_k \sim \mathcal{N}(0, \sigma_k)$.

Retention Error

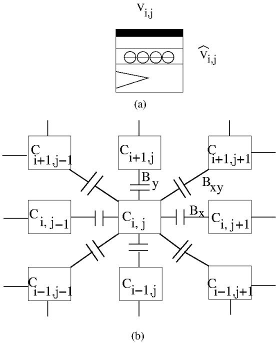


(a)

(b)

- $V_{i,j}(t) = V_{i,j}(0)e^{-v_{i,j}t} + Z_{re}$.
  - $V_{i,j}(t)$ – cell level for cell $c_{i,j}$ at time t

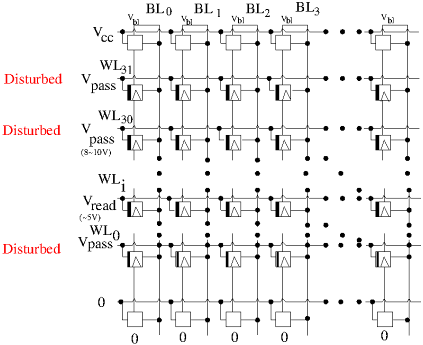
Cell-to-cell interference



-

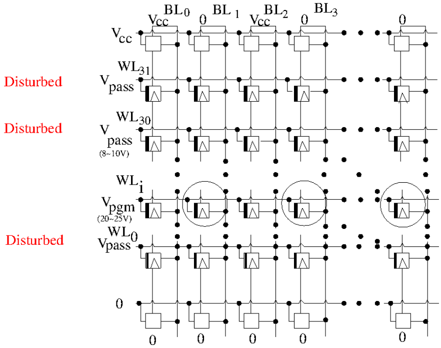
$$\begin{aligned} V_{i,j} &= \hat{V}_{i,j} + B_x(\hat{V}_{i,j-1} + \hat{V}_{i,j+1}) + B_y(\hat{V}_{i-1,j} \\ &+ \hat{V}_{i+1,j}) + B_{xy}(\hat{V}_{i-1,j+1} + \hat{V}_{i-1,j-1} \\ &+ \hat{V}_{i+1,j+1} + \hat{V}_{i+1,j-1}) + Z_{inter}, \end{aligned}$$

Read disturb



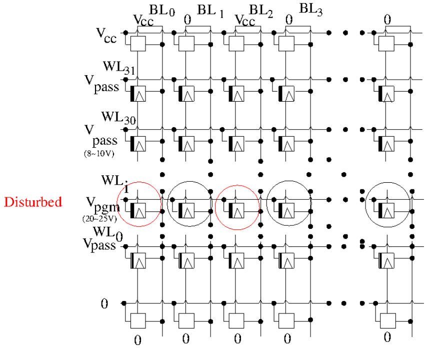
- $V'_{i,j} = V_{i,j} + \gamma^{rd}_{i,j} + Z_{rd}$.
- $V_{i,j}$ – cell level before read disturb; $V'_{i,j}$– cell level after read disturb; γ^{rd}– average cell level increase due to read disturb; Z_{rd} — possible deviation.

Pass disturb



- $V'_{i,j} = V_{i,j} + \gamma^{pasd}_{i,j} + Z_{pasd}$.
- $V_{i,j}$ – cell level before pass disturb; $V'_{i,j}$– cell level after pass disturb; γ^{pd}– average cell level increase due to pass disturb; Z_{pd} — possible deviation.

Program disturb



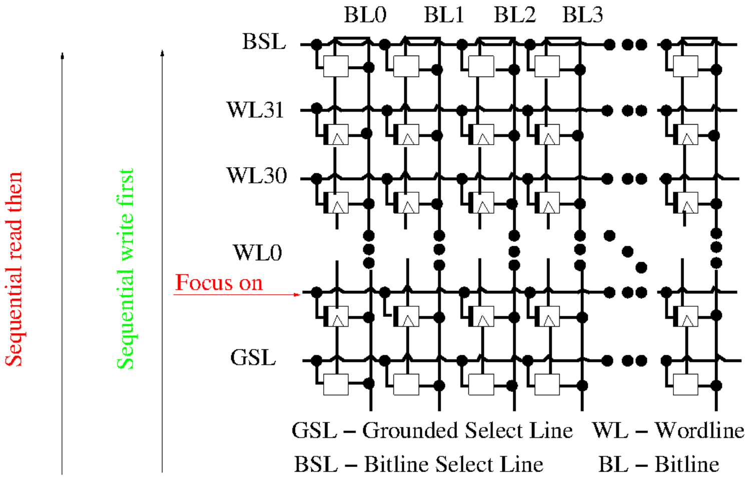
- $V'_{i,j} = V_{i,j} + \gamma^{prod}_{i,j} + Z_{prod}$.
- $V_{i,j}$ – cell level before program disturb; $V'_{i,j}$– cell level after program disturb; γ^{pd}– average cell level increase due to program disturb; Z_{prod} — possible deviation.

4 Capacity analysis of flash memory

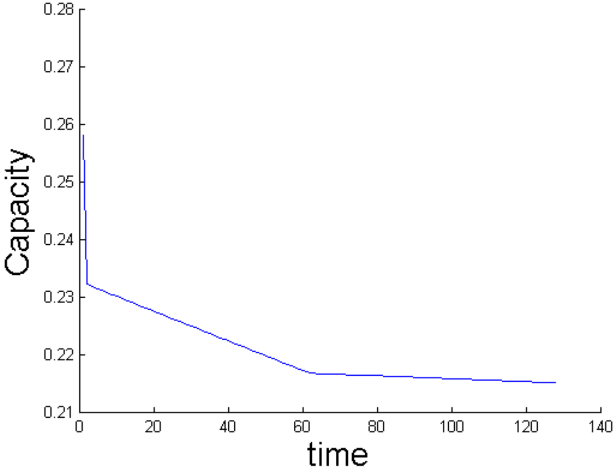
In this section, we analyze the impact of noise on channel capacity with our model

- Capacity degrades with flash operations.
- Impact of sub-threshold for flash capacity.
- Benefit of dynamic thresholds.

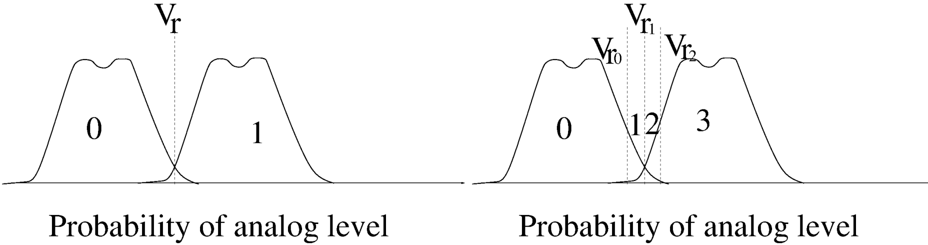
Capacity degrades with flash operations (1/2)



Capacity degrades with flash operations (2/2)



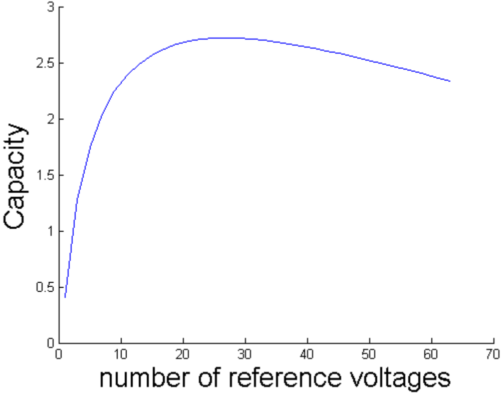
The impact of sub-thresholds for flash capacity (1/2)



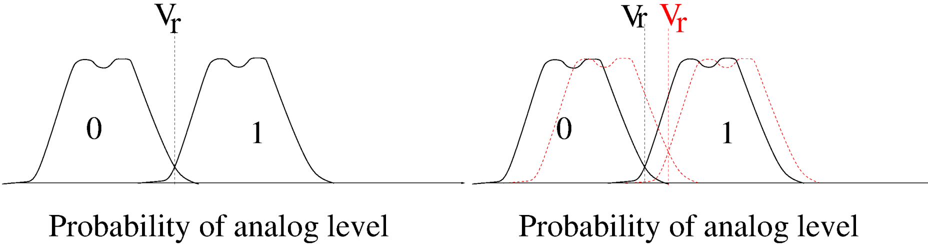
- More sub-thresholds, more read disturb.

The impact of sub-thresholds for flash capacity (2/2)

- There is a complex trade-off between the number of sub-thresholds and flash capacity.

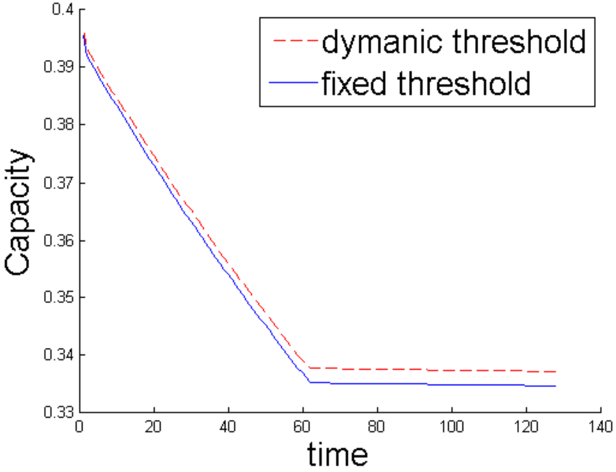


Dynamically adjust reference threshold voltages (1/2)



- Dynamically adjust references to minimize error probability.

Dynamically adjust reference threshold voltages (2/2)



5 Conclusion and future work

- We have explored noisy in NAND flash memories and their impacts on capacity.

- Future work: precisely characterize the mathematical formulas of noise.

Thank you!