Enterprise NAND Flash Memory with 1x-nm Technology

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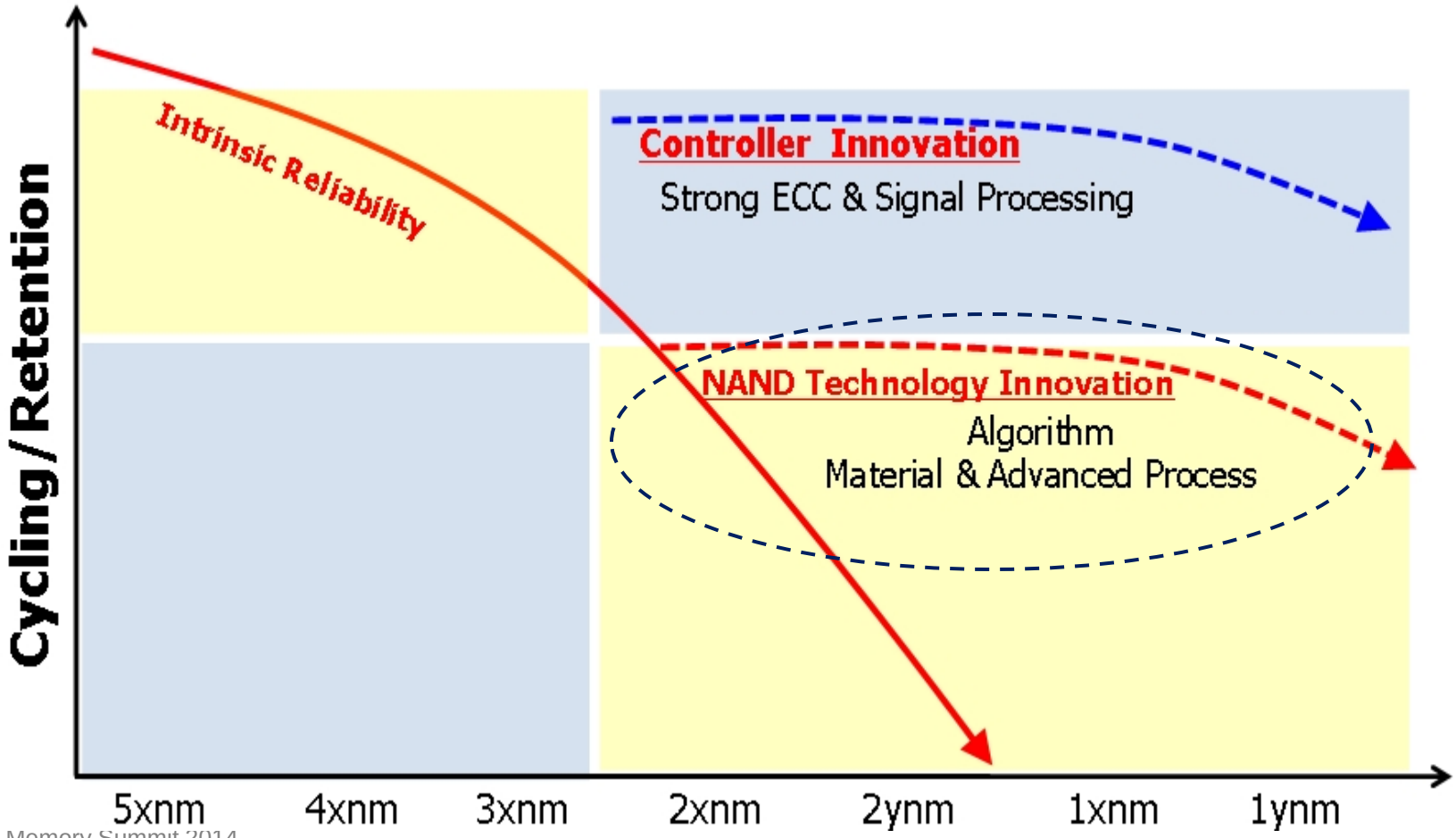
Introduction

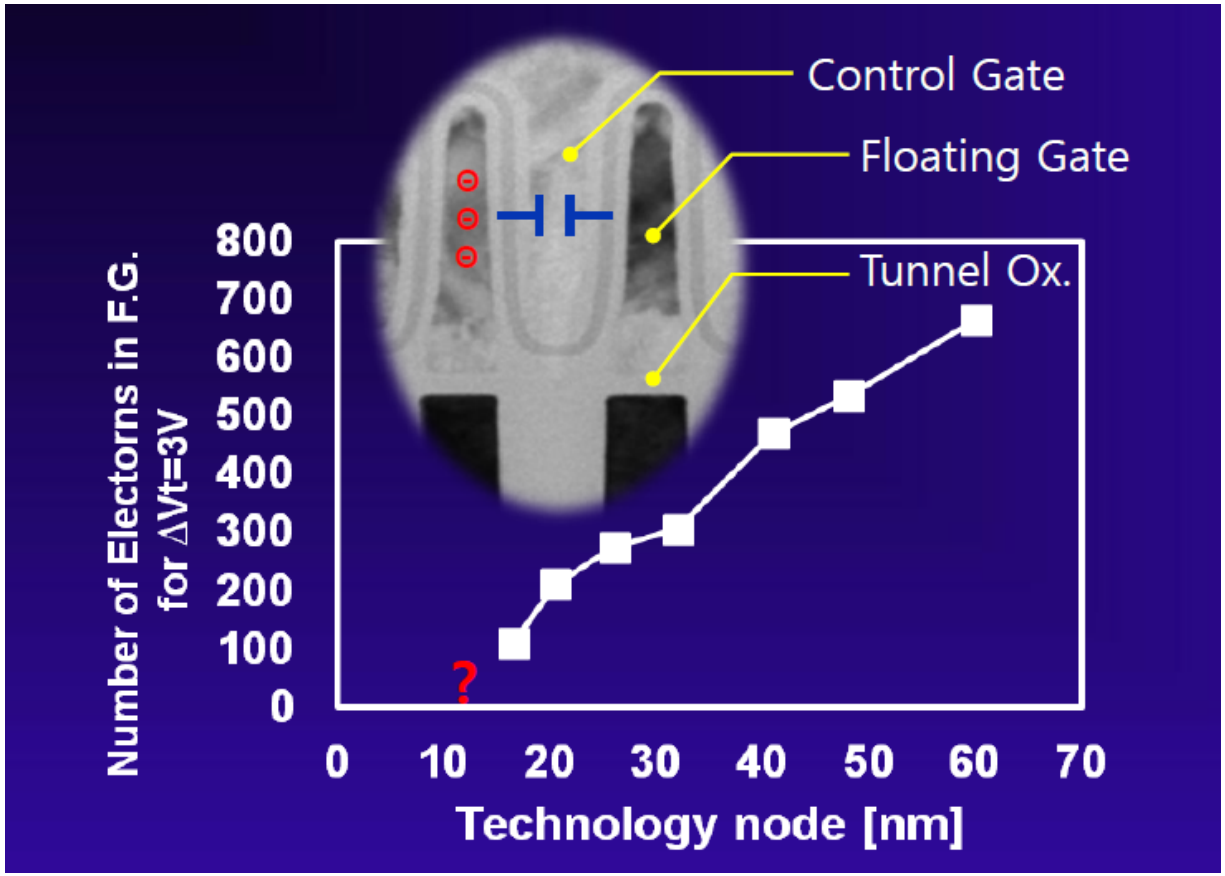
Technology Innovation for Scaling Challenges

- Process technology innovation compensates intrinsic reliability degradation.
- NAND Reliability is also boosted by strong ECC engine of controller and algorithms from below 2X nm technology



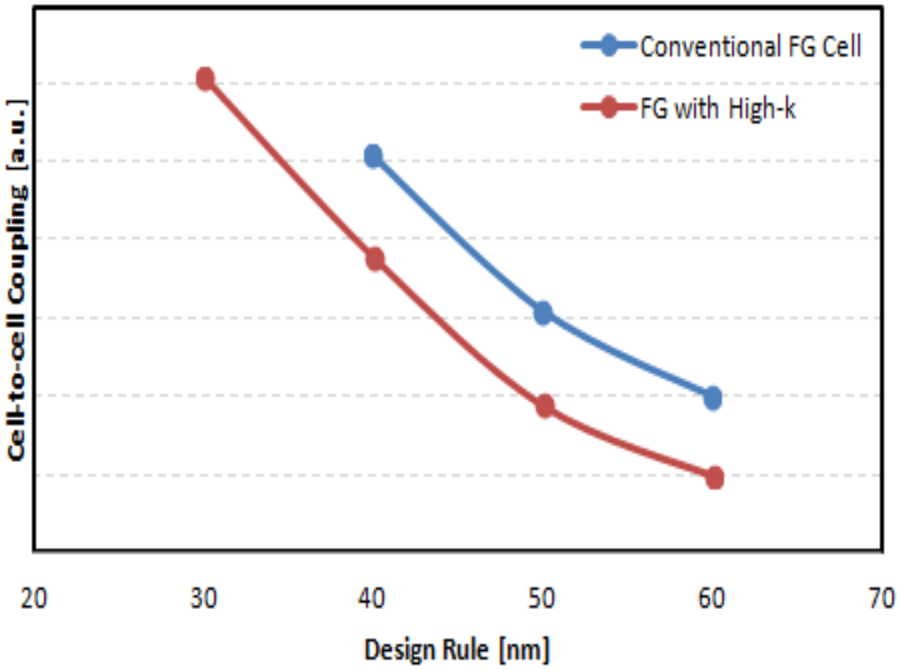
Scaling Issues : Reduced Number of Stored Electrons

- Number of stored electrons in floating gate is about 100 electrons/3V in 1X nm tech.
- It causes small charge loss tolerance.

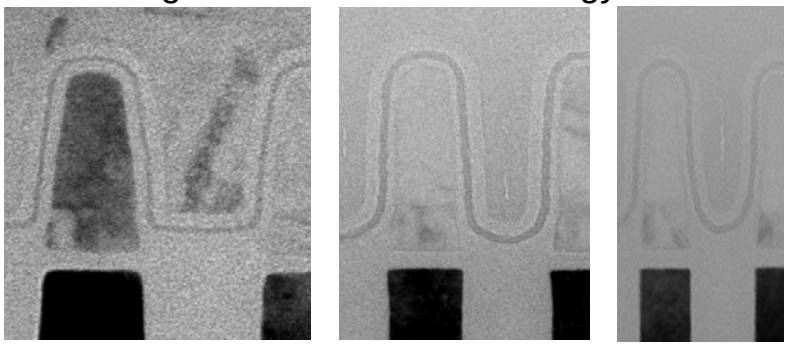


Scaling Issues : Interference by Coupling

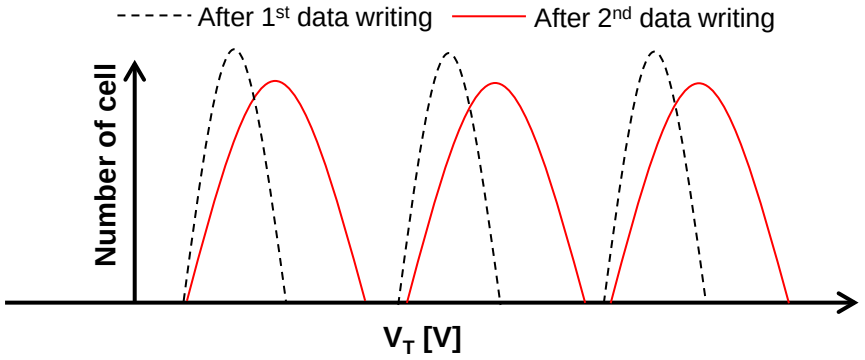
- As tech. shrinks, cell to cell interference by coupling is increased.
- It is more difficult to maintain state separation.



TEM images with various technology nodes.

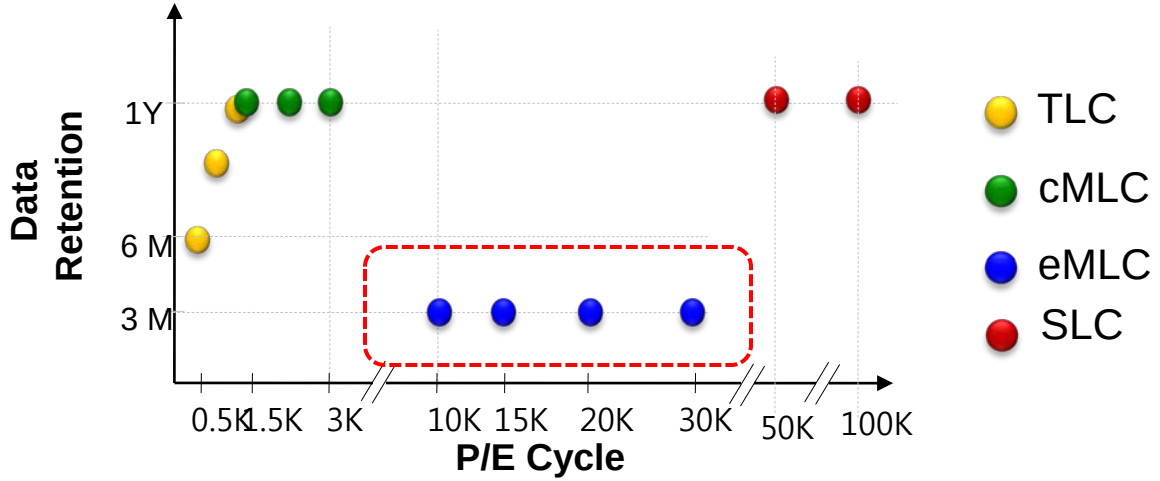


(a) 4x-nm (b) 3x-nm (c) 2y-nm



Reliability Targets in 1X nm devices – cMLC, eMLC

- Different reliability targets as application and usage modes in the same technology.
- eMLC products require higher P/E cycle and less retention characteristics than those of cMLC.

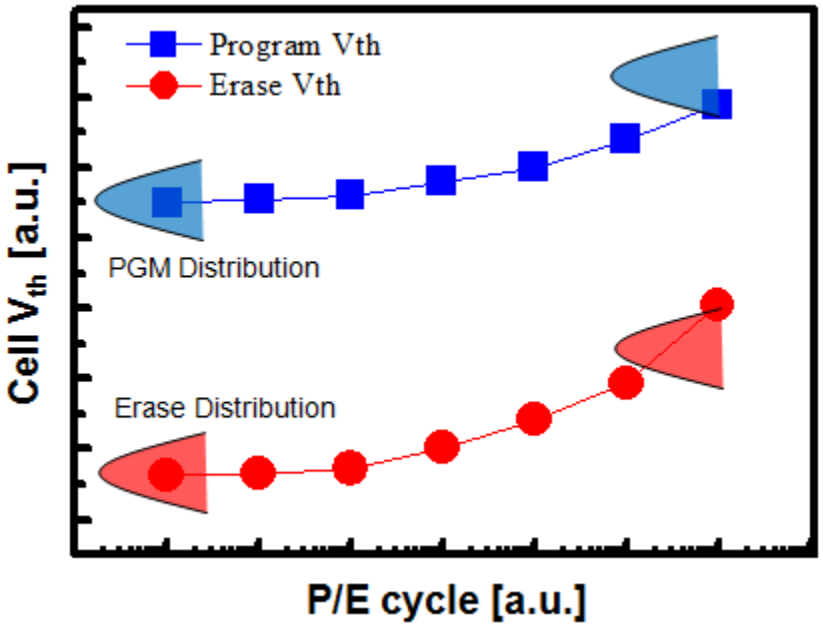


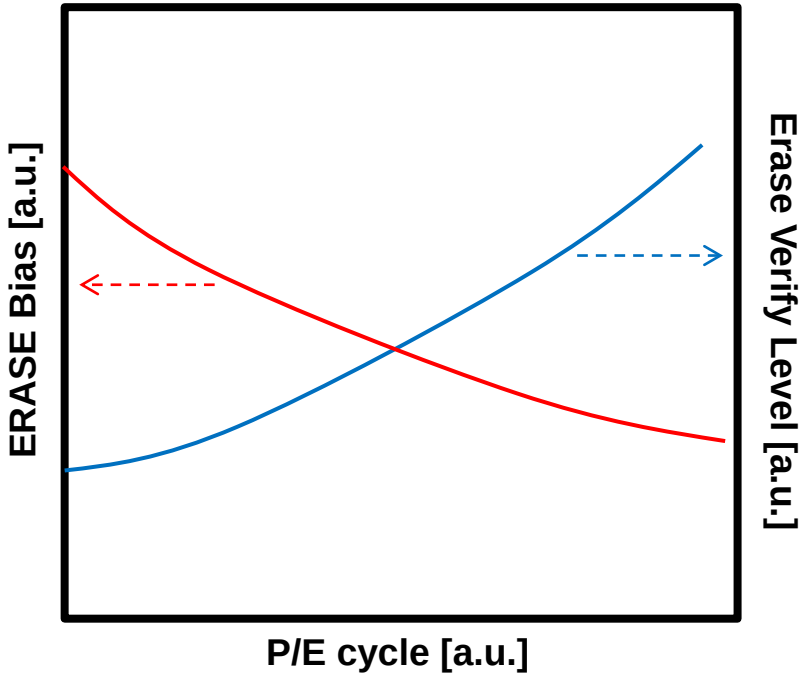
	SLC	eMLC	cMLC	TLC
Endurance	50K~100K	5K~30K	1.0K~3K	0.5K~1.5K
Retention	1Y	1~3Months	1Y	0.5Y~1Y
Read Disturbance	100K	3K	10K	3K~5K
ECC Engine	BCH	BCH & LDPC	BCH&LDPC	BCH & LDPC

Algorithms for eMLC with 1x-nm Tech.

Erase Verify Level Control

- Since erase stress is the major factor for cell degradation as P/E cycles, controlling erase verify level is important for eMLC.
- We can apply reduced erase bias by increasing erase verify level which results in less stress to tunnel oxide.

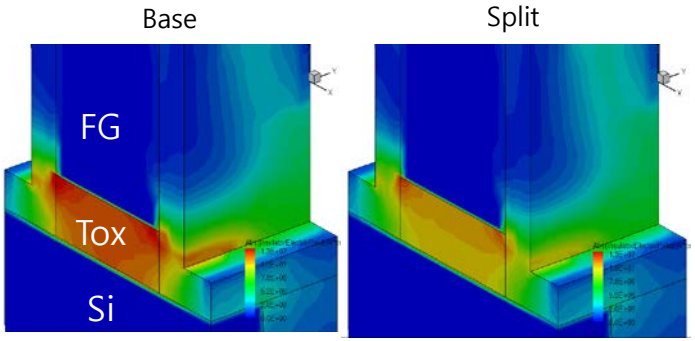




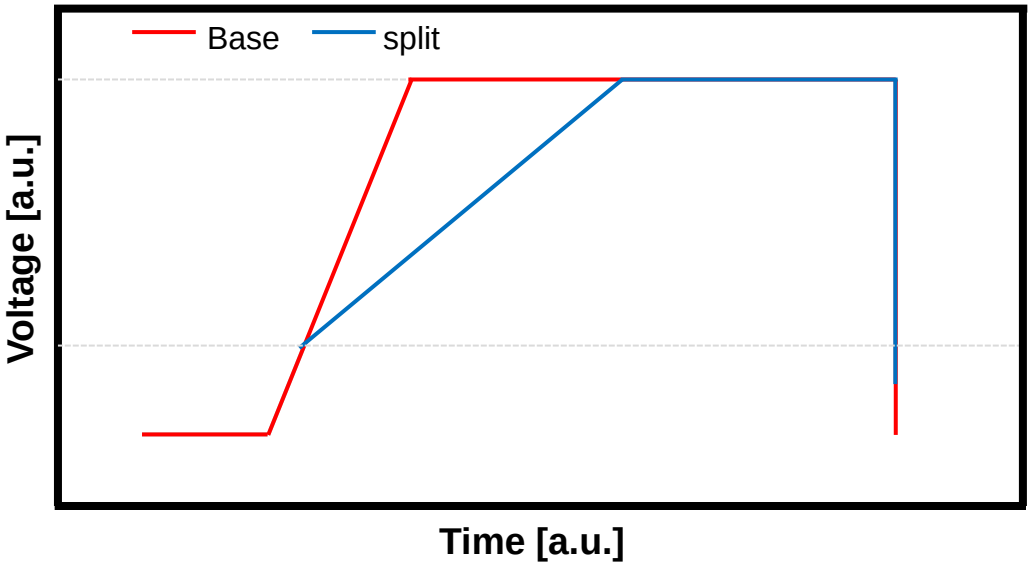
Erase pulse control

- Electric field at tunnel oxide is higher when steep erase slope scheme is used.
- Erase stress is reduced by erase rising slope control for higher P/E cycles.

• Electric field simulation

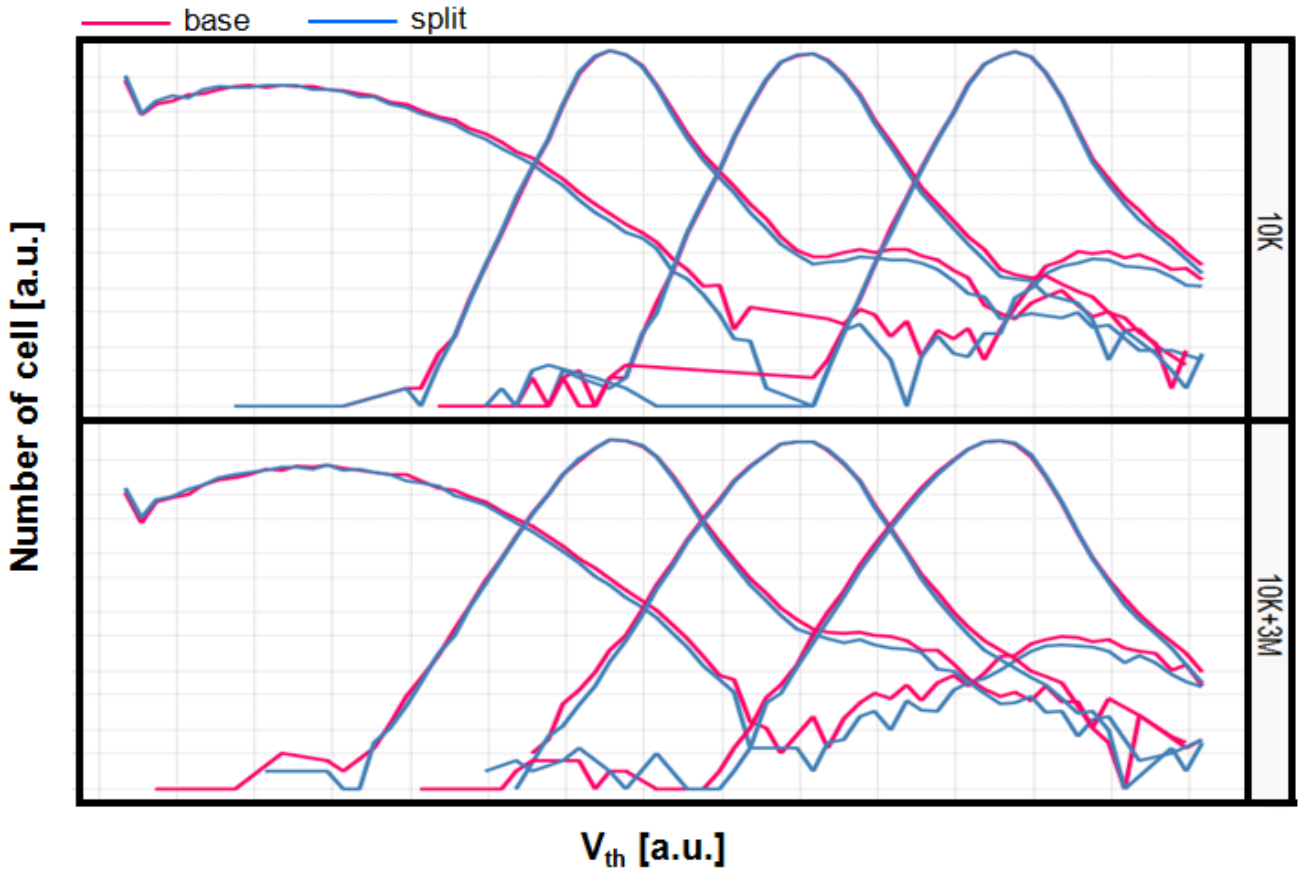


• Erase Pulse



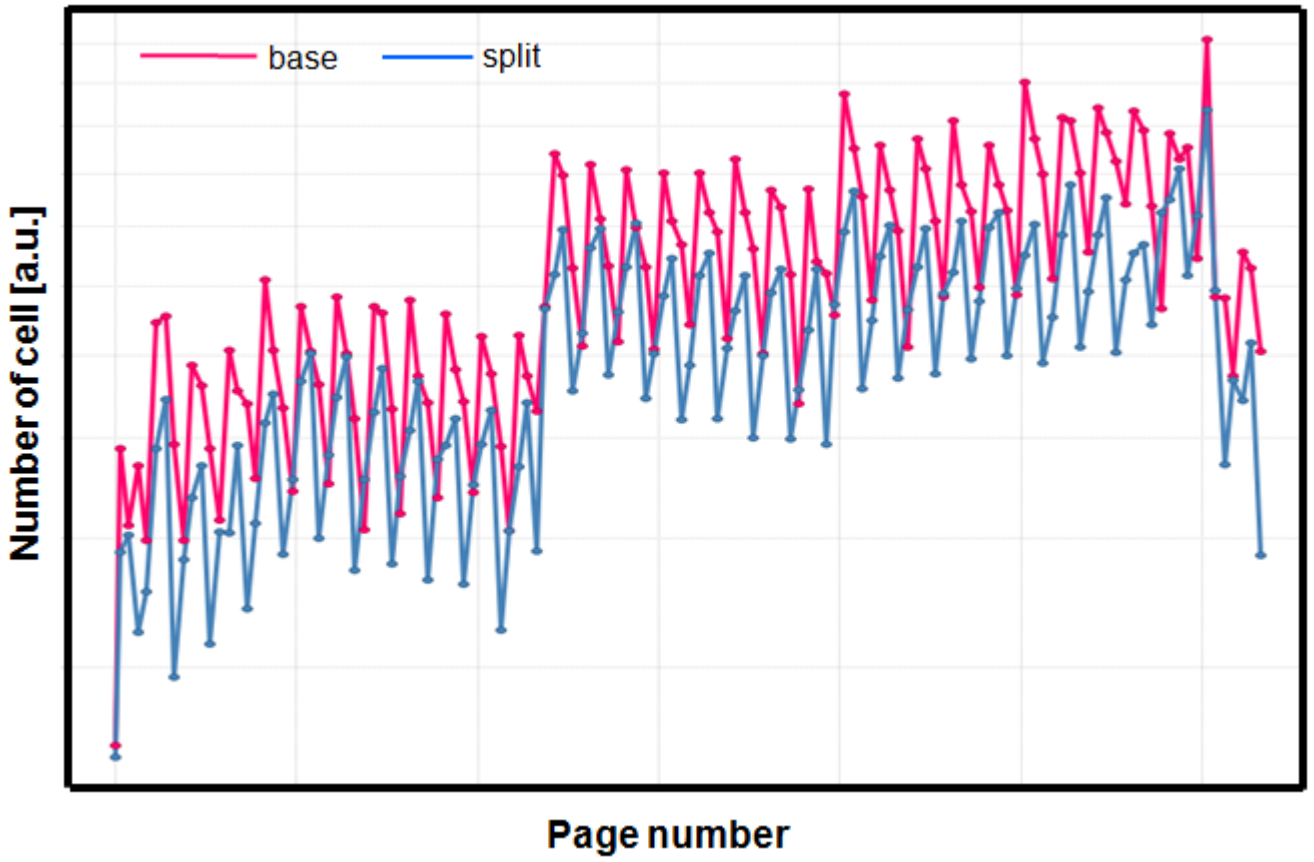
Erase pulse control : Distribution

- After P/E cycles, split condition shows improved distribution.
- After P/E + Retention, split condition also shows better results.



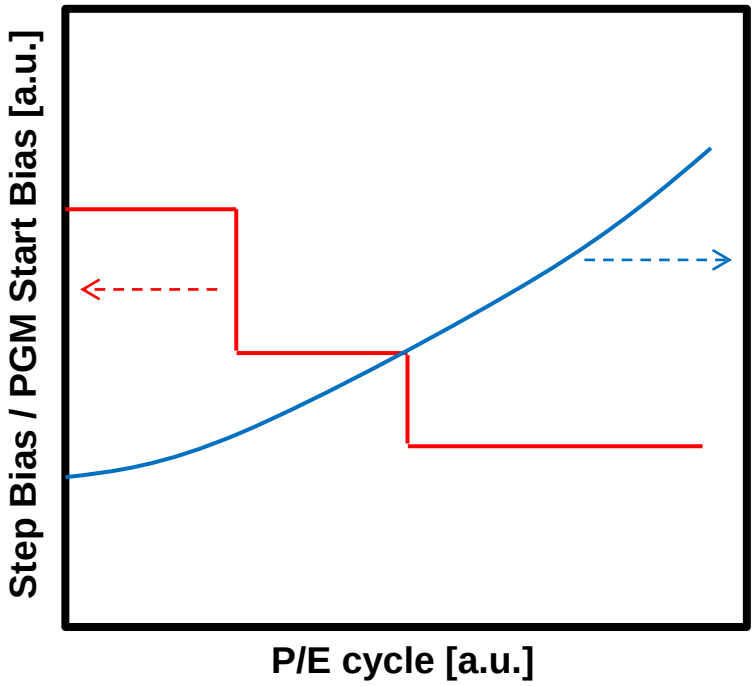
Erase pulse control : Disturbance

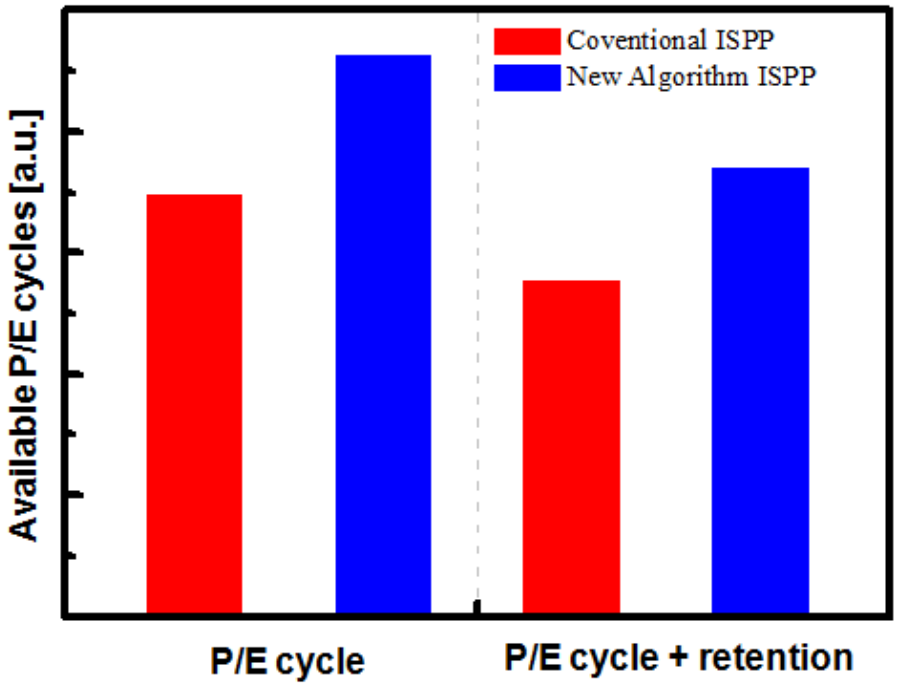
- Applying split condition results in better disturb characteristics.



Controller assisted ISPP algorithms

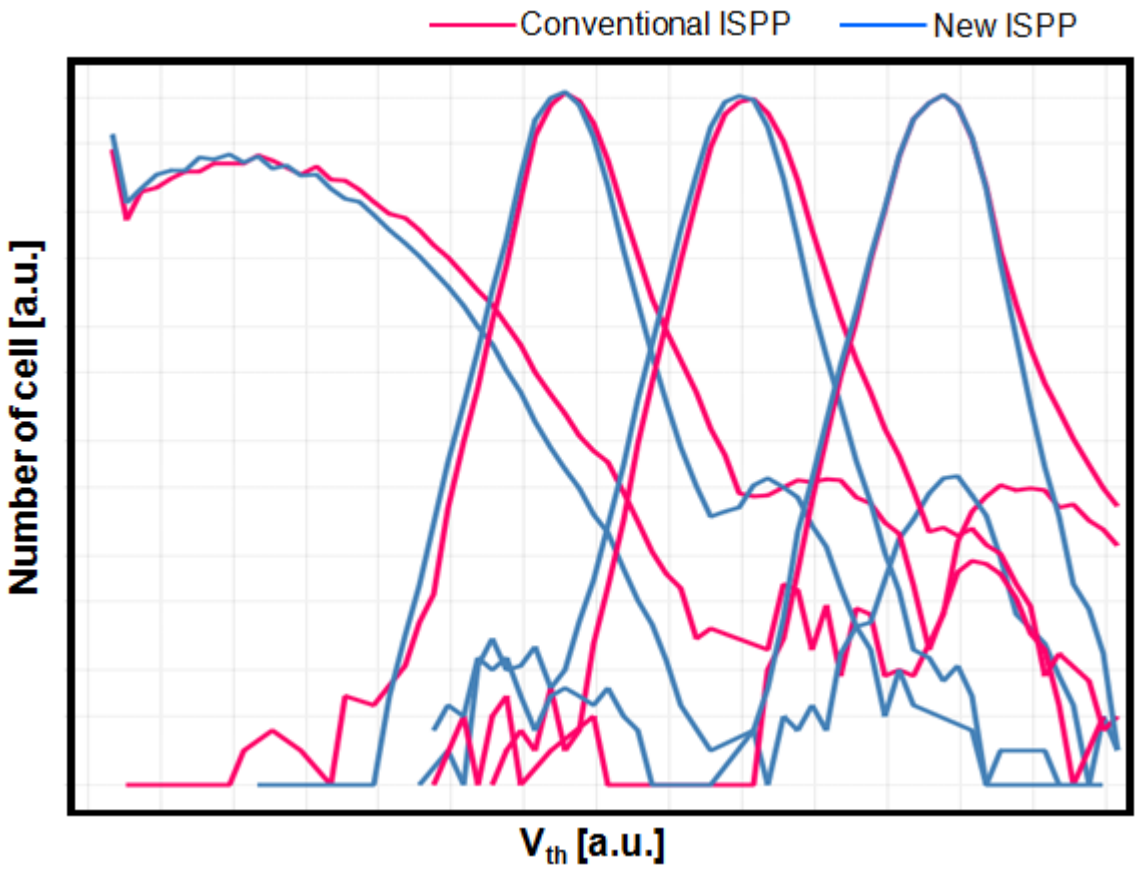
➢ Using the controller assisted new ISPP algorithm which modify the program condition with tracking cell speed results in improved cycle and retention characteristics.





Controller assisted ISPP algorithms

- Applying new ISPP algorithm shows improved distribution after 10K P/E cycles.



Conclusions

- As technology shrinks, it is difficult to get high reliability because of increasing cell-to-cell coupling and reduced number of stored electrons in floating gate.

- We made eMLC NAND flash memory with 1x-nm by using several algorithms.

- As P/E cycles, cell speed is increased so that controlling erase verify level delicately results in less stress to tunnel oxide.

- By controlling erase pulse scheme, we can reduce erase stress which results in improved distribution and disturbance characteristics with high P/E cycles.

- Using controller assisted ISPP algorithms make it possible to get better distribution characteristics after high P/E cycles.

Thank you for your attention

Q & A