



NVDIMM CONTROLLER ARCHITECTURE

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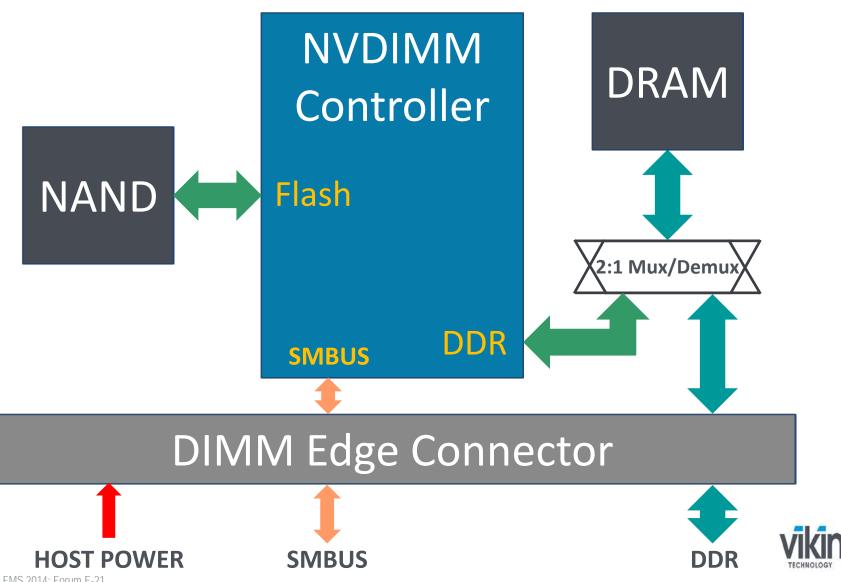


NVDIMM

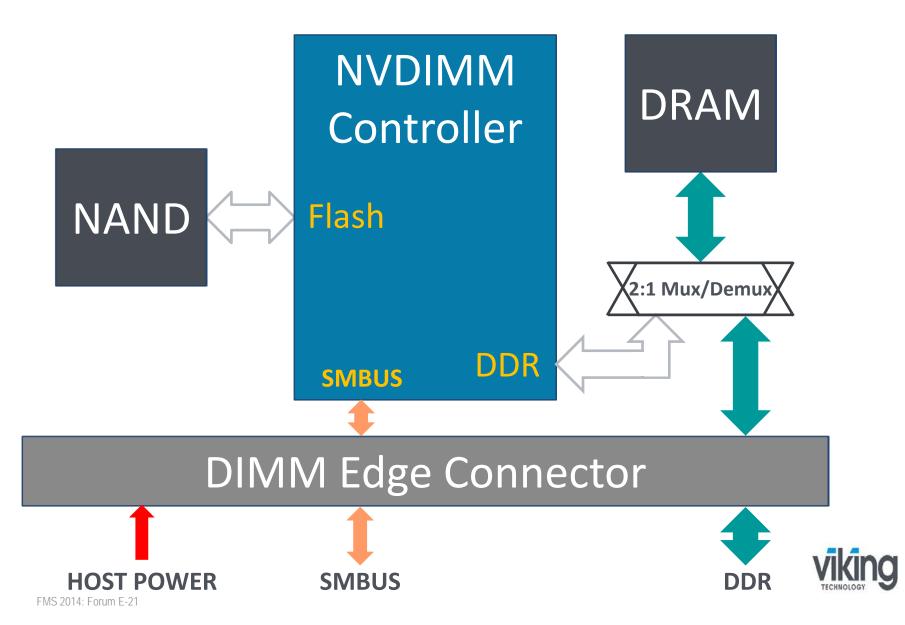
- "Hybrid" Memory Module Combining DRAM and NAND
 - Plugs Into JEDEC Standard DDR DIMM Socket
- Leverages Beneficial Characteristics Of Each Memory Technology
 - Speed, endurance, and random byte addressability of DRAM
 - Non-volatility of NAND Flash
- Enables Main Memory Persistence
 - Data in DRAM is preserved through system power cycles



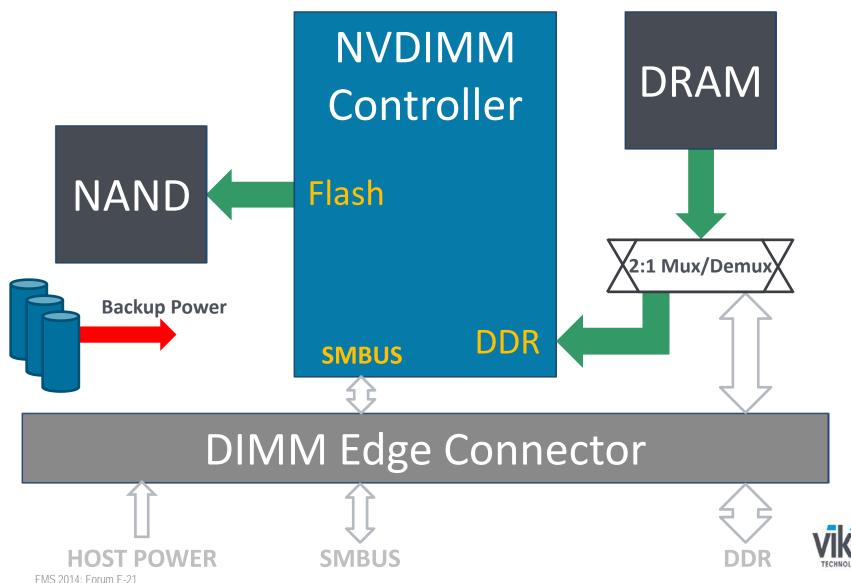
NVDIMM Block Diagram



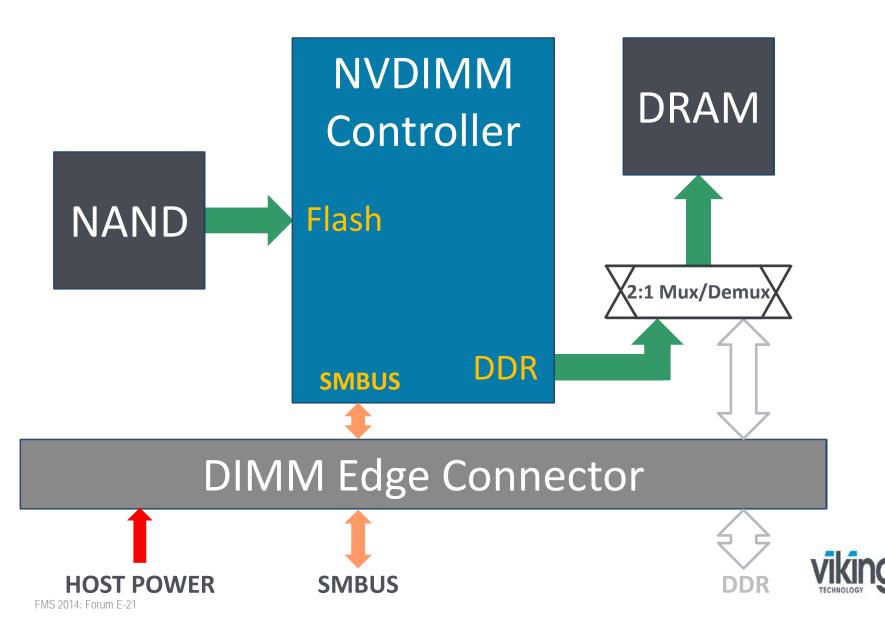
Standard DIMM Operation



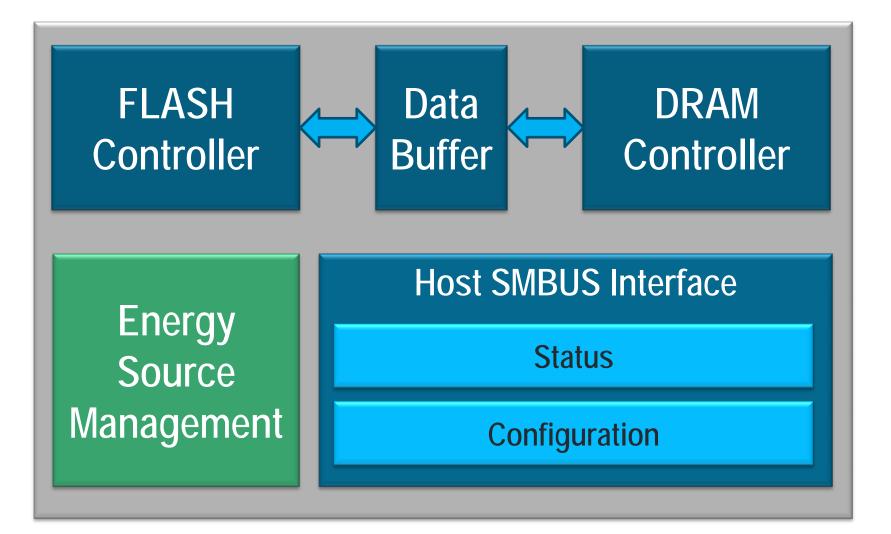
SAVE Operation



RESTORE Operation



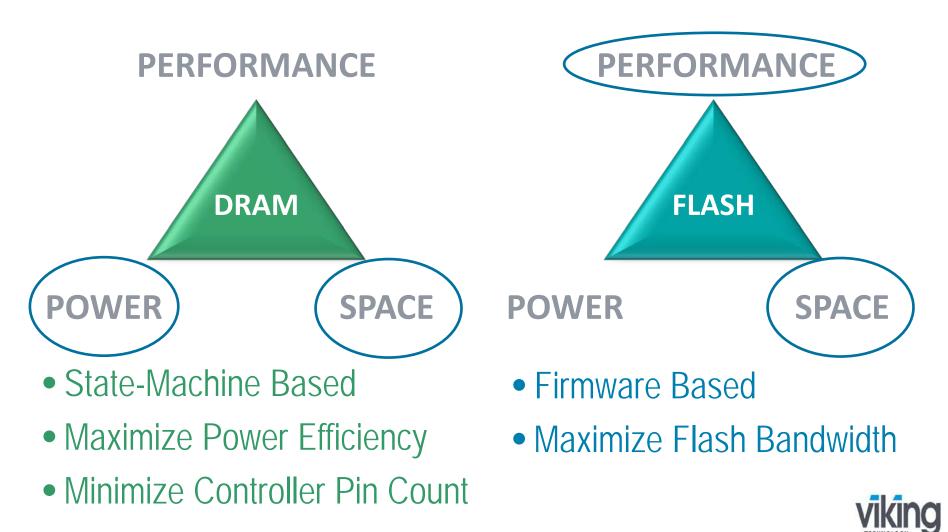
NVDIMM Controller





Memory Controller Design Tradeoffs

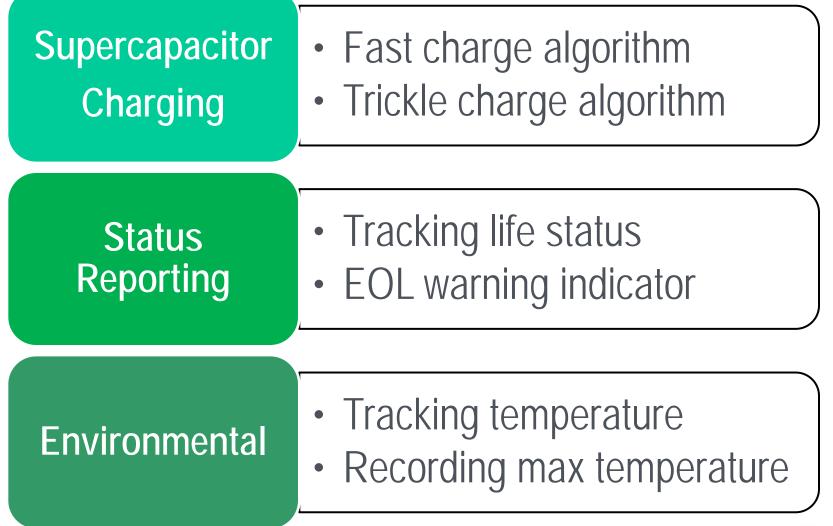
• Key Goals: Minimize SAVE energy, board space, and cost



Flash Controller Comparison

	General Purpose SSD Controller	NVDIMM Controller
Workload	Heavy read to heavy write %, random, sequential, small or large block	During SAVE, 100% large block sequential writes, During RESTORE, 100% large block sequential reads
Endurance	1-10 DWPD	<1 DWPD
Static Data Retention	Years	Not required to preserve SAVE'd images once they've been restored.
Performance Consistency	Tolerant to some variation in latency, bandwidth	Strict requirement to complete SAVE within maximum time limit. Write B/W needs to be consistent.
ECC, Wear Leveling, Bad Block Mgmt	Required. ECC strength appropriate to flash technology being deployed.	Required. ECC strength appropriate to flash technology being deployed
Garbage Collection	Complex	Straightforward
Read Disturb, Read Scrub	Required	Not Required

Energy Source Management





Host Control / Status Interface

Configuration

- ARM / DISARM NVDIMM
- Automatic SAVE Trigger Types

Control

- Commands: SAVE, RESTORE, ERASE
- Reset

Status

- NVDIMM Operating Mode
- Energy Source Health
- Flash Statistics





Questions?





Thank You

