Iterative, Layered and Latticed ECC
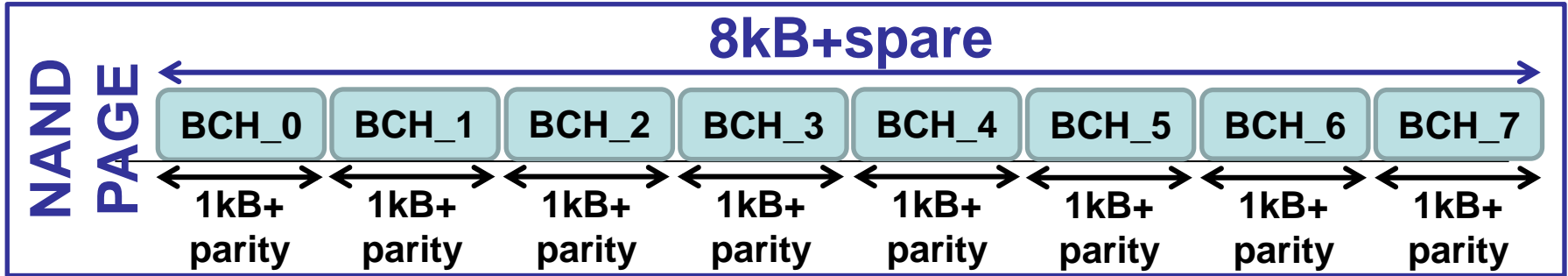
Oliver Hambrey

Siglead Europe

www.siglead.com

Hamming Code

↓

BCH

↓ ↓

iterative BCH "turbo"

- hard

LDPC

- hard
- soft
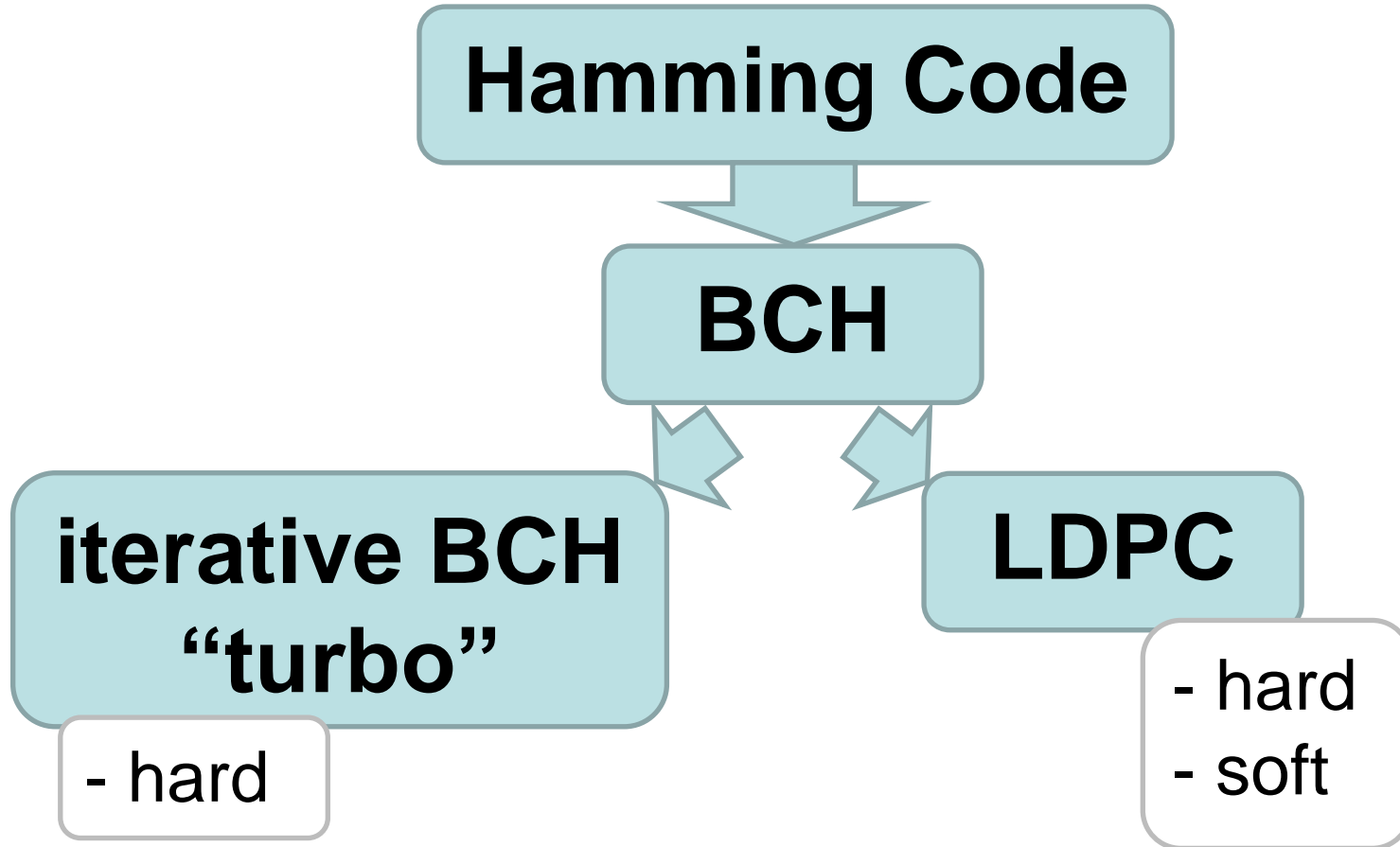
Iterative

- **standard** approach (several standalone ECCs per page)

8kB+spare

NAND PAGE

| BCH_0 | BCH_1 | BCH_2 | BCH_3 | BCH_4 | BCH_5 | BCH_6 | BCH_7 |

1kB+parity | 1kB+parity | 1kB+parity | 1kB+parity | 1kB+parity | 1kB+parity | 1kB+parity | 1kB+parity

- **iterative** approach (ECCs exchange information)

8kB+spare

NAND PAGE

| BCH_0 | BCH_1 | BCH_2 | BCH_3 | BCH_4 | BCH_5 | BCH_6 | BCH_7 |

1kB+parity | 1kB+parity | 1kB+parity | 1kB+parity | 1kB+parity | 1kB+parity | 1kB+parity | 1kB+parity
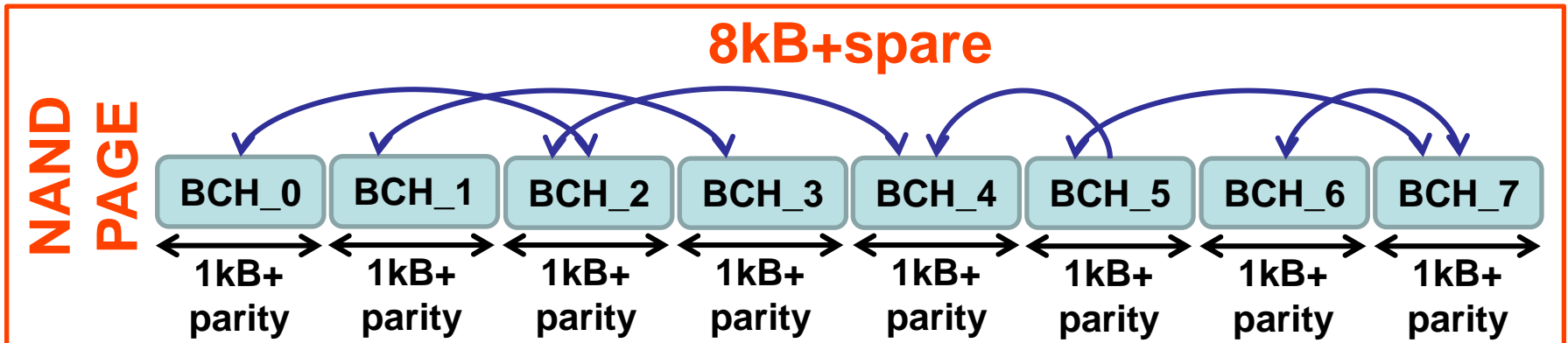
- **CLAIM:** same code rate, lower UPER

Layered

Stronger Error Correction → (left arrow, downward)

Higher Latency → (right arrow, downward)

MAIN ECC (BCH)

↓

INTRA PAGE ITERATIONS

↓

READ RETRY

↓

NEIGHBOUR PAGE ITERATIONS
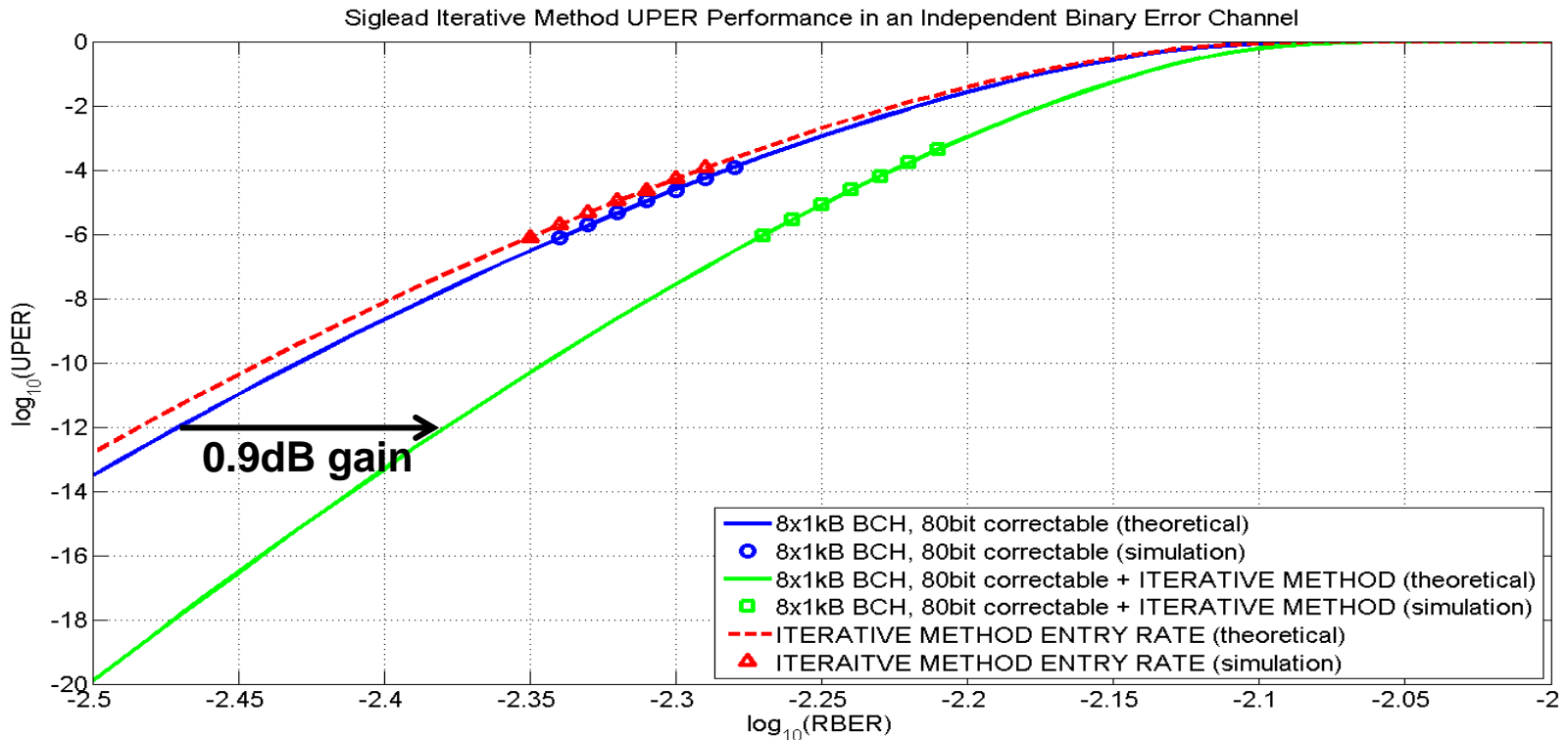
↓

LATTICE ECC

↓

HIGHER LEVEL RECOVERY
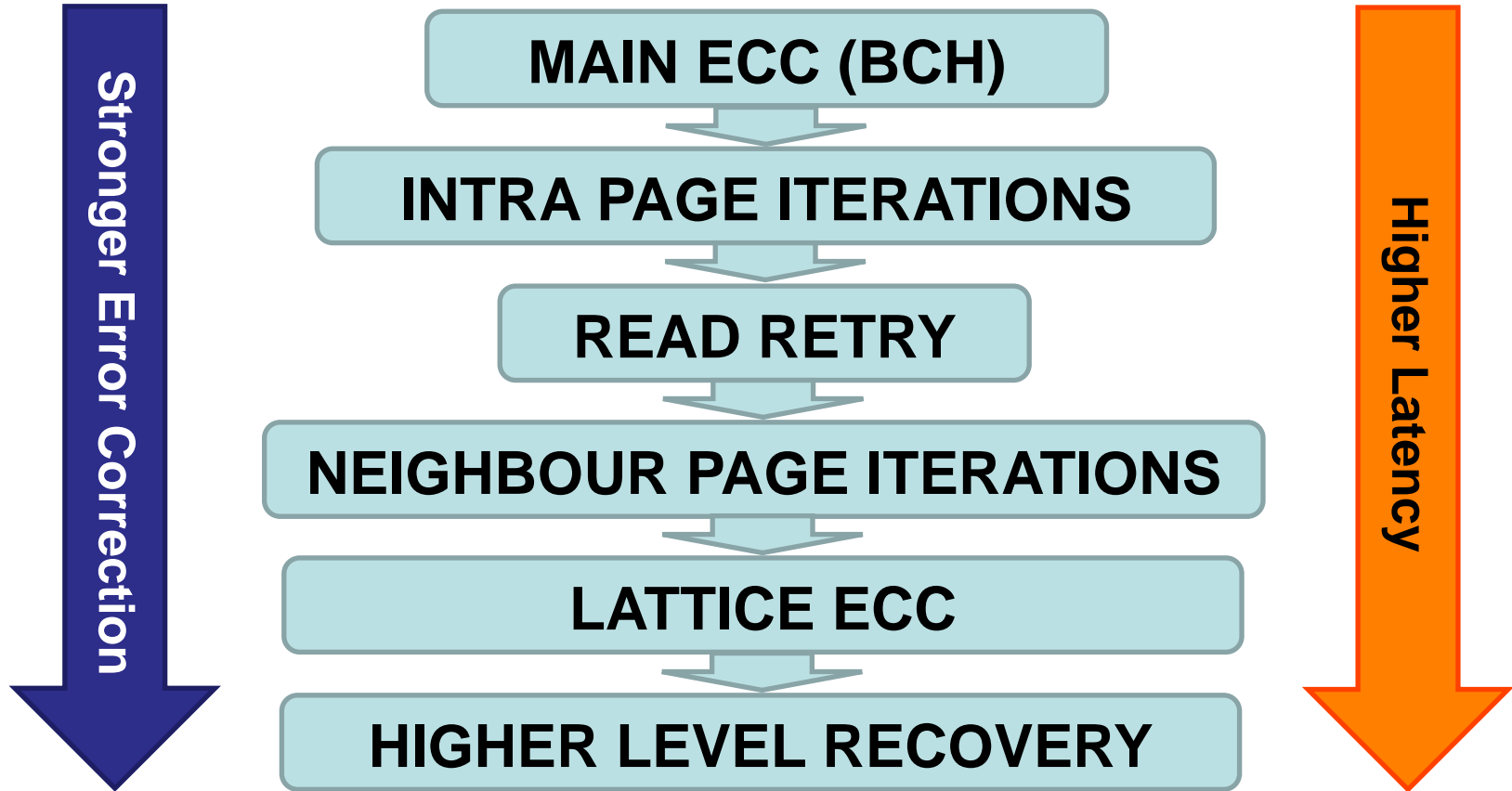
- **Rule of thumb:** **Enter next layer with frequency at most 0.1/x**
  x is the increase in latency between current and next layer
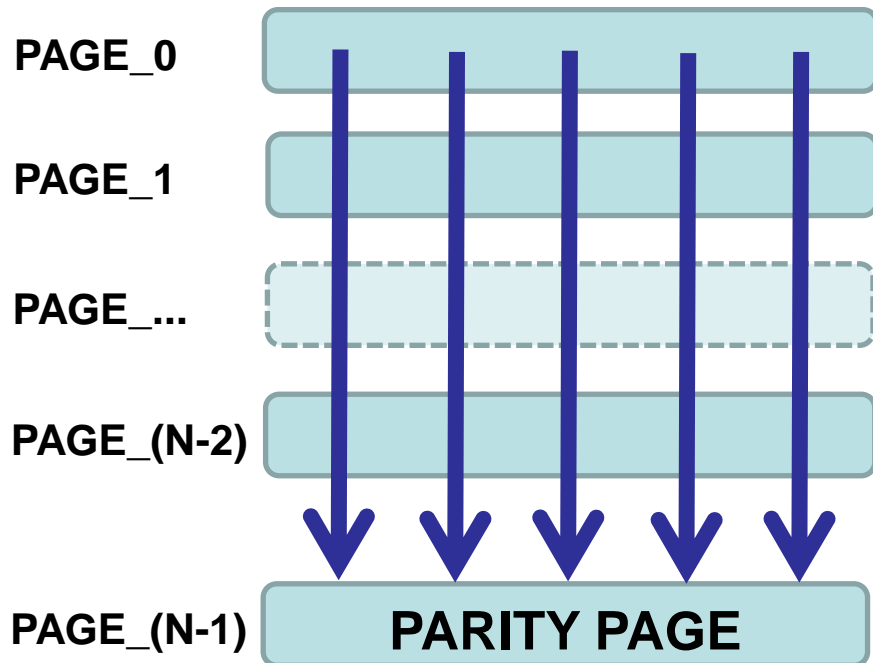
Iterative Performance Evaluation

Sigiead Iterative Method UPER Performance in an Independent Binary Error Channel

$\log_{10}(\text{UPER})$ vs $\log_{10}(\text{RBER})$

0.9dB gain

Legend:
- 8x1kB BCH, 80bit correctable (theoretical)
- 8x1kB BCH, 80bit correctable (simulation)
- 8x1kB BCH, 80bit correctable + ITERATIVE METHOD (theoretical)
- 8x1kB BCH, 80bit correctable + ITERATIVE METHOD (simulation)
- ITERATIVE METHOD ENTRY RATE (theoretical)
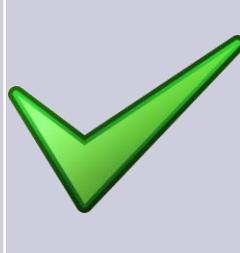- ITERAITVE METHOD ENTRY RATE (simulation)

Iterative Method:

- ☑ 0.9dB gain in RBER @ UPER$=10^{-12}$
- ☑ No reduction in code rate
- ☑ No noticeable increase in mean latency

Latticed

BLOCK RAID-LIKE LATTICE

PAGE_0

PAGE_1

PAGE_...

PAGE_(N-2)

PAGE_(N-1) **PARITY PAGE**

	RAID-LIKE	LATTICE ECC
# parity pages	**r**	**r**
always correct up to **r** bad pages?	✅	✅
sometimes correct more than **r** bad pages?	❌	✅

Lattice ECC Correctability

1x TLC NAND - Page Correctability of Lattice ECC

(Y-axis: Percentage of Lattices Correctable by Lattice ECC; X-axis: Number of Uncorrectable Pages Before Lattice ECC)
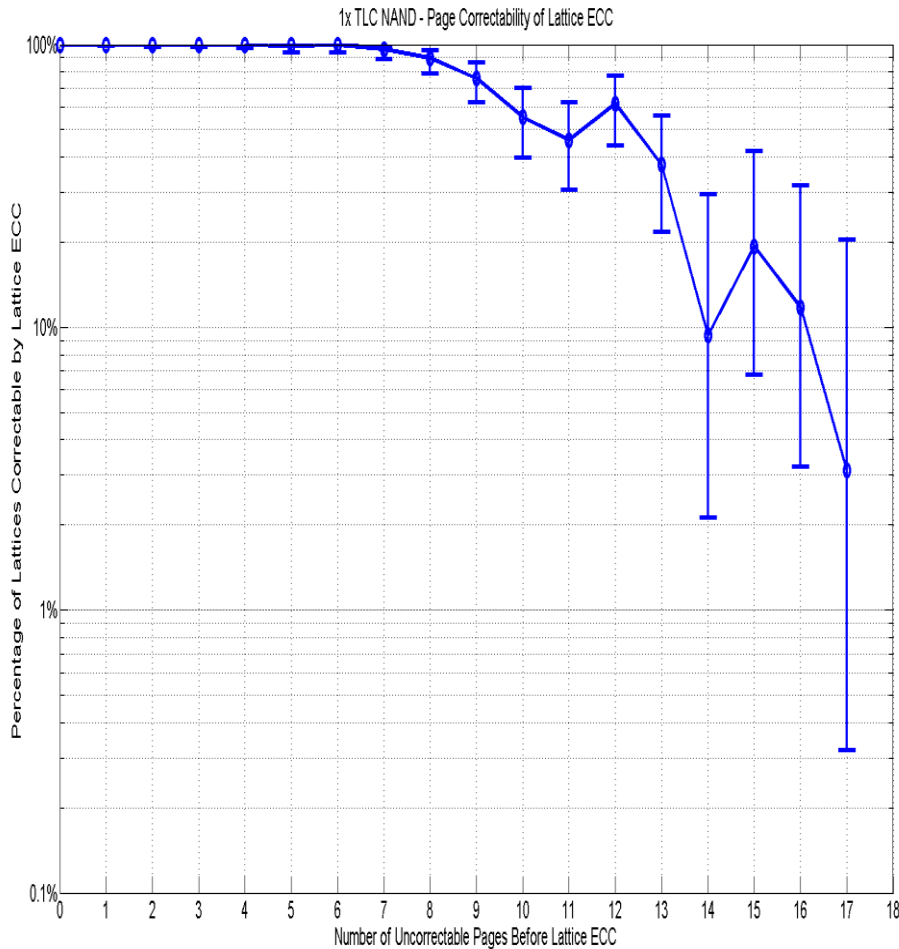
- ➢ **1x TLC NAND**
  - ▪ over 2 million pages analysed
- ➢ lattice size: 129 pages
  - ▪ 128 info pages
  - ▪ 1 parity page
- ➢ 1 page correctable guaranteed
- ➢ **up to 8 pages correctable more than 90% of the time!**

ECC ENGINE	P/E CYCLE ENDURANCE (5 P/E cycles per day per block@40ºC)			LIFESPAN@800P/E CYCLES (years@30ºC)		
	300	400	900	0	1	7
8x1kB BCH 60bit correctable per 1kB	✔	✘	✘	✘	✘	✘
8x1kB BCH 60bit correctable per 1kB + SIGLEAD ITERATIVE METHODS	✔	✔	✔	✔	✔	✔

➢ **Siglead's iterative BCH engine:**
  ✓ **increases P/E cycle endurance**
  ✓ **improves data retention lifespan**

Summary

1. **Iterative methods based on hard BCH decoding:**
   - powerful error correction
   - no change in code rate
   - low silicon cost
   - negligible impact on average latency

2. **Powerful Lattice ECC:**
   - guaranteed correctability of r bad pages with r parity pages
   - more than guaranteed correctability in many cases

3. **Siglead's iterative BCH engine:**
   - powerful, low latency, iterative hard ECC
   - significant endurance and lifetime gains for sub 20nm NAND

www.siglead.com/eng

- ➢ **SSD controller SL2007(8):**
  - ▪ SATAIII
  - ▪ 8(16) CE/channel
  - ▪ Siglead's iterative BCH engine
- ➢ **SigNASII/III:**
  - ▪ NAND Flash Memory evaluation
- ➢ **ADC/DAC evaluation board Sp9907:**
  - ▪ AD converter 12bit 550Msps 2channel
  - ▪ DA converter 16bit 1Gsps 2channel

SL2007 — High quality SSD Controller IC

SigNASIII — NAND Flash Memory tester

Sp9907 — FPGA with high speed ADC/DAC

SigNASII — NAND Flash Memory analyzer