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LDPC Code Concepts and Performance on High-Density Flash Memory

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Conventional SSD Controllers use BCH Codes

- BCH codes are algebraic codes
  - Defined by code length and error correction capability: for example 40 bit error correction over 1KB code words
  - Straight-forward ECC design based on these parameters
- BCH codes are decoded with hard-decision algorithms
- Error recovery by read retry
  - Individual hard decision decoding attempts for different read voltages

Low-Density Parity Check Codes

- Defined by a sparse (low density) parity check matrix H
- Are represented with a bi-partite graph
- Approach channel capacity
- Support hard and soft decision decoding
- Past Applications:
  - Standard-based: Wifi (802.11n), 10G Ethernet (802.3an), DVB 2nd Gen.
  - Non-standard based: Hard Disk Drives

LDPC Code Illustration

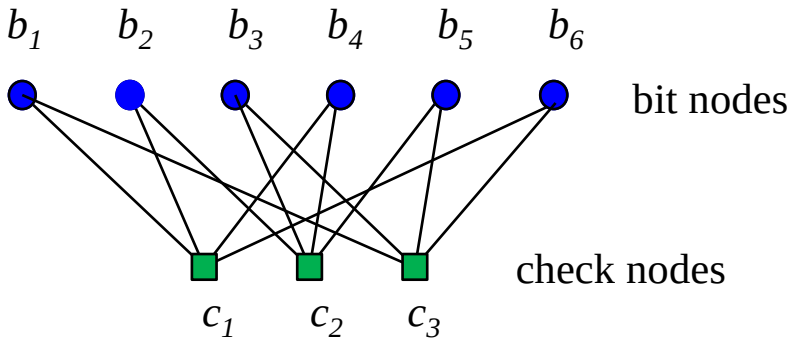
Parity Check Matrix:

$$H = \begin{array}{c} \begin{matrix} b_1 & b_2 & b_3 & b_4 & b_5 & b_6 \end{matrix} \\ \begin{bmatrix} 1 & 1 & 0 & 1 & 0 & 1 \\ 0 & 1 & 1 & 1 & 1 & 0 \\ 1 & 0 & 1 & 0 & 1 & 1 \end{bmatrix} \end{array} \begin{matrix} \\ c_1 \\ c_2 \\ c_3 \end{matrix}$$

Parity Check Equations:

$$c_1: \quad b_1 + b_2 + b_4 + b_6 = 0$$
$$c_2: \quad b_2 + b_3 + b_4 + b_5 = 0$$
$$c_3: \quad b_1 + b_3 + b_5 + b_6 = 0$$

Bi-Partite Graph:



LDPC Design Parameters

- Code rate
- Code length
- Parity check matrix and graph topology
  - Column weight = number of edges of bit node
  - Regular/irregular code = constant/non-constant column weight
- Decoding by an iterative message-passing algorithm
  - Min-sum
  - Sum-product

LDPC Error Correction Capability

- LDPC error correction capability depends on:
  - Quality of soft decisions
  - Number of decoding iterations
  - Error location
- LDPC error correction capability is best specified by:
  - Supported raw bit error rate (RBER) at target user bit error rate (UBER) after decoding
  - UBER = codeword failure rate / user bits per code word

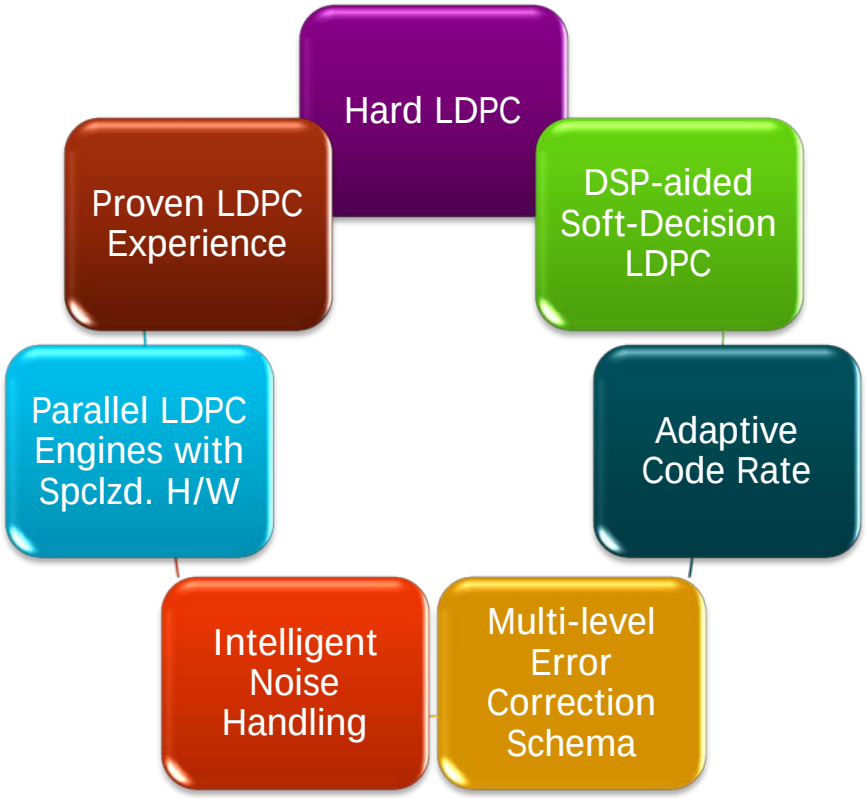
LDPC Codes Applied to Flash

- Flash devices typically provide hard decisions for a single read voltage
- Soft decision can be obtained by
  - reading with multiple read voltages
  - combining these read results to compute log-likelihood ratios (LLRs):

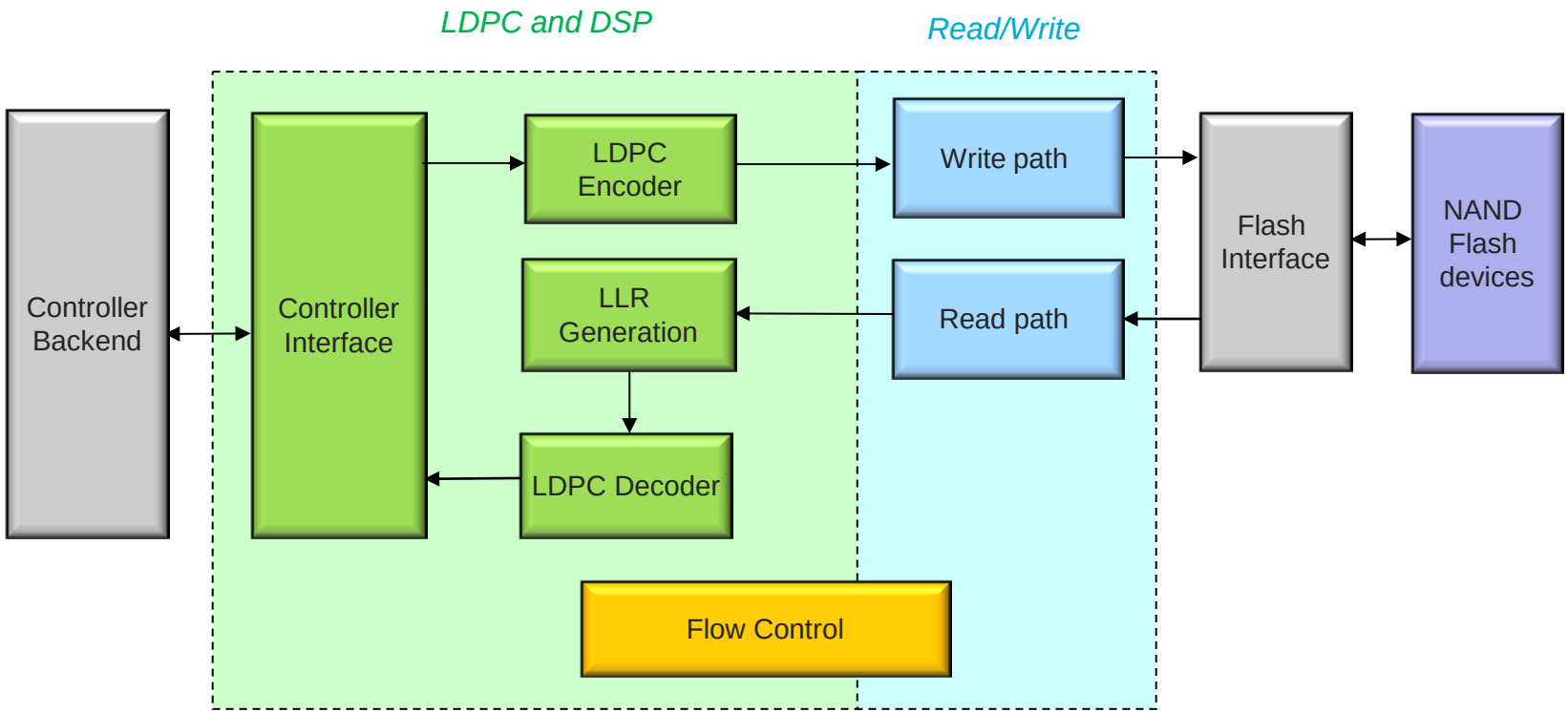
$$LLR = \frac{P(c = 0|r)}{P(c = 1|r)}$$

LSI SandForce® SHIELD™: Advanced LDPC for Flash Storage

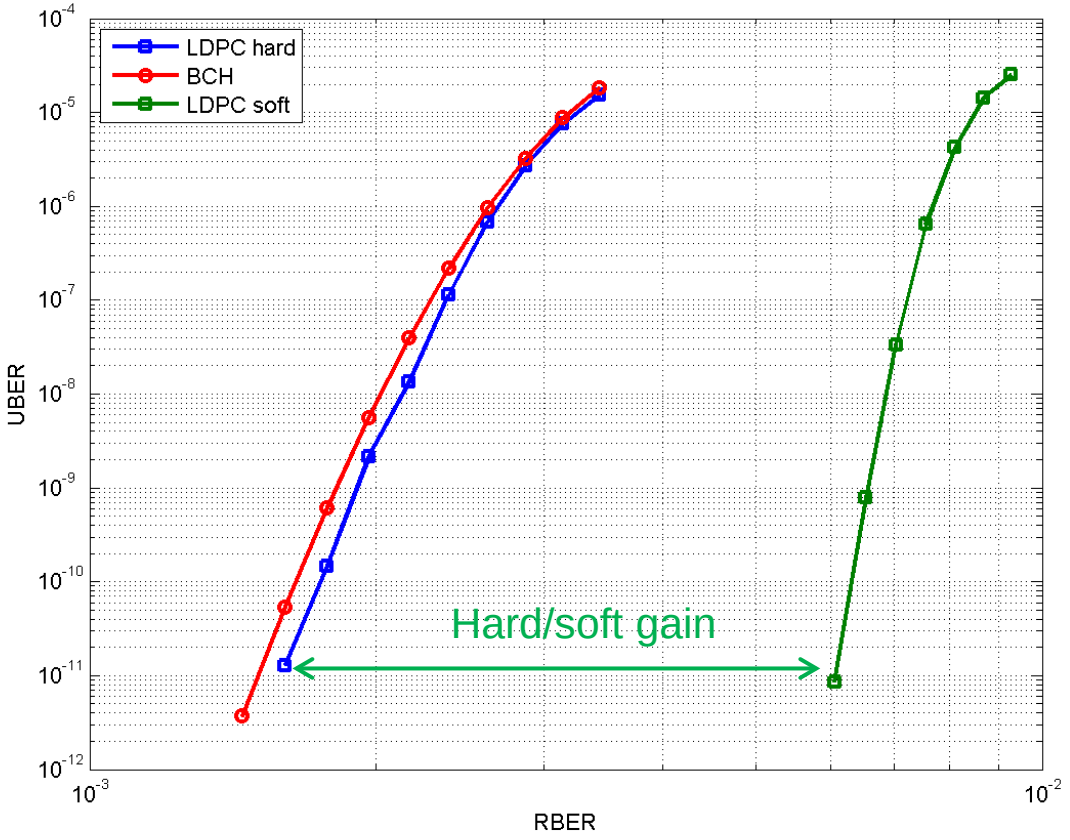
SHIELD™ uniquely combines a number of features and correction techniques for optimum time-to-data



LDPC Controller Block Diagram

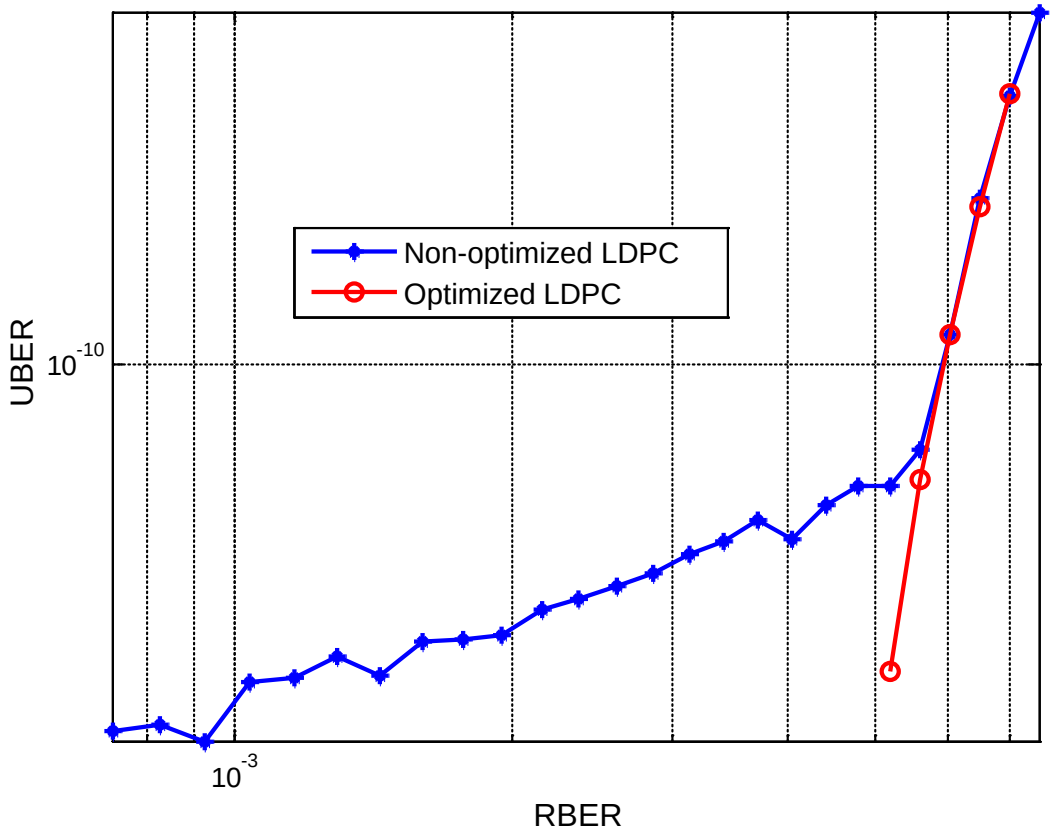


Hard/Soft LDPC vs. BCH Coding



Soft-decision LDPC coding has significant gain over BCH coding

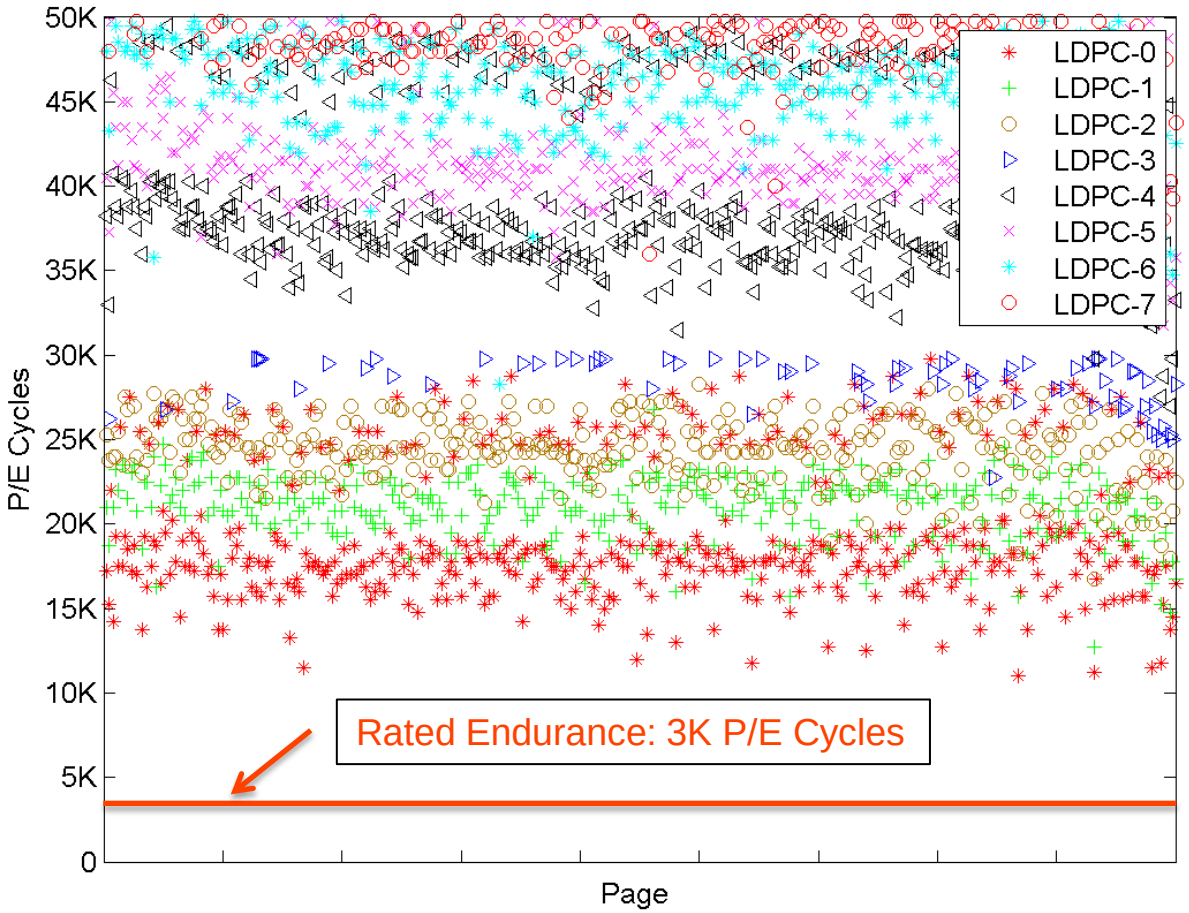
Optimized LDPC Error Correction Performance



Don't be fooled by unproven LDPC solutions

LDPC Correction Performance with Latest 15/16-nm Class MLC Flash

Stronger LDPC Correction



Conclusion

- LDPC codes are best characterized in terms of supported RBER at the target UBER.
- Significant expertise and knowledge are required to design an optimized LDPC solution that meets the target UBER.
- LDPC codes outperform BCH codes by a significant margin.
- LDPC codes extend the lifetime of the latest high-density flash memories.