Hardware/Software Co-Simulation for Error-Floor Detection in LDPC

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LDPC & NAND

- LDPC codes are becoming popular for ultra-scaled NAND technologies
- Error floor phenomenon is due to the iterative nature of decoding algorithm
- Error floor can’t simply be predicted by using equations
- UBER target $<10^{-16}$
- UBER needs to be verified

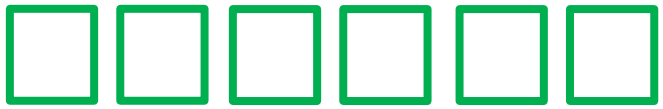
LDPC Validation

Solution A

small simulation effort - few HW/SW resources –> long simulation time

ASIC with LDPC engine Development Time

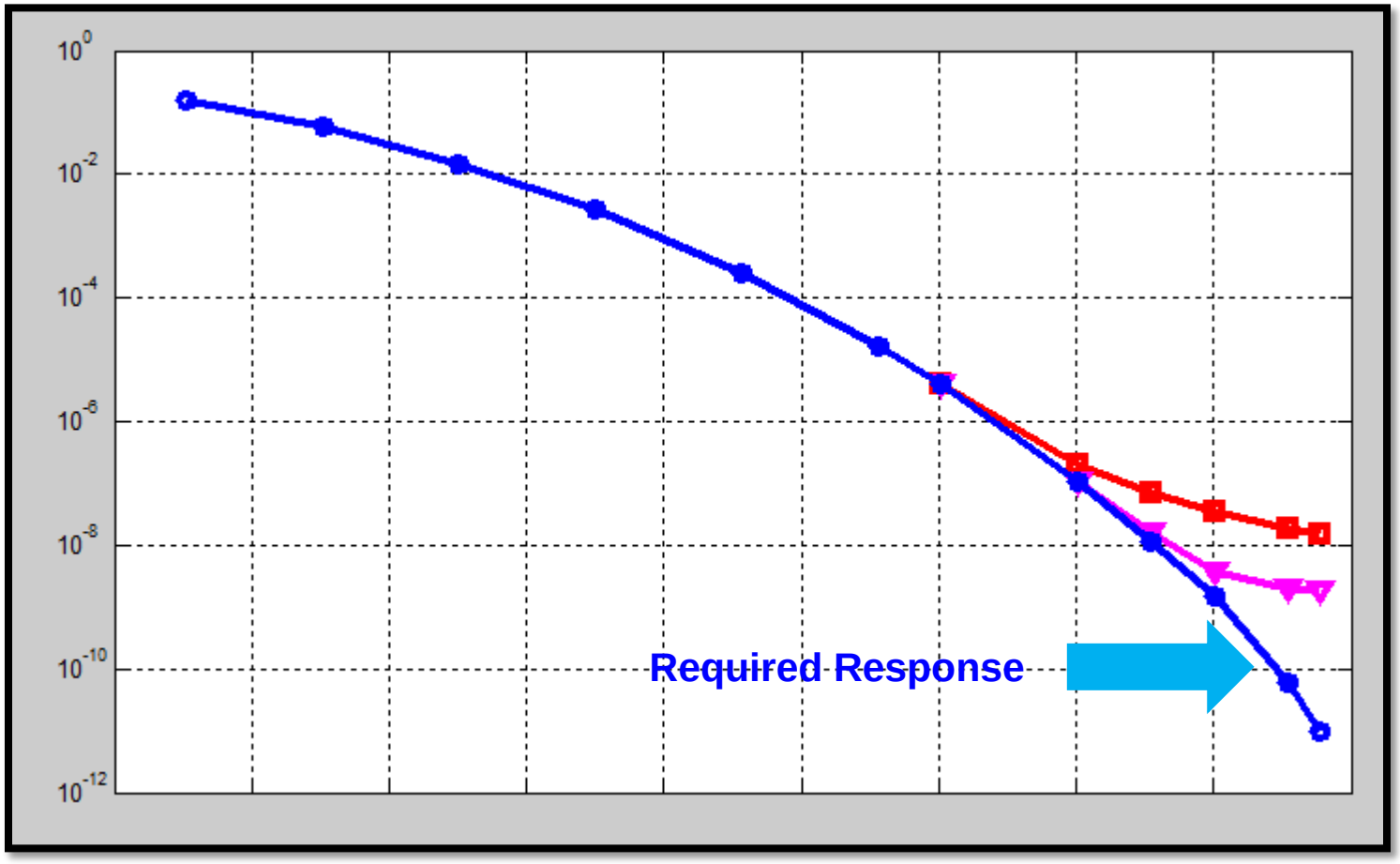
Solution B



BIG simulation effort
A lot of HW/SW resources
–> very short simulation time
–> multiple simulation rounds

- We may have to support multiple Code Rates
- Multiple revisions of any given code will have to be completed
- Software to find good candidate solutions is a must! (Must minimize the number of deep dive revisions)

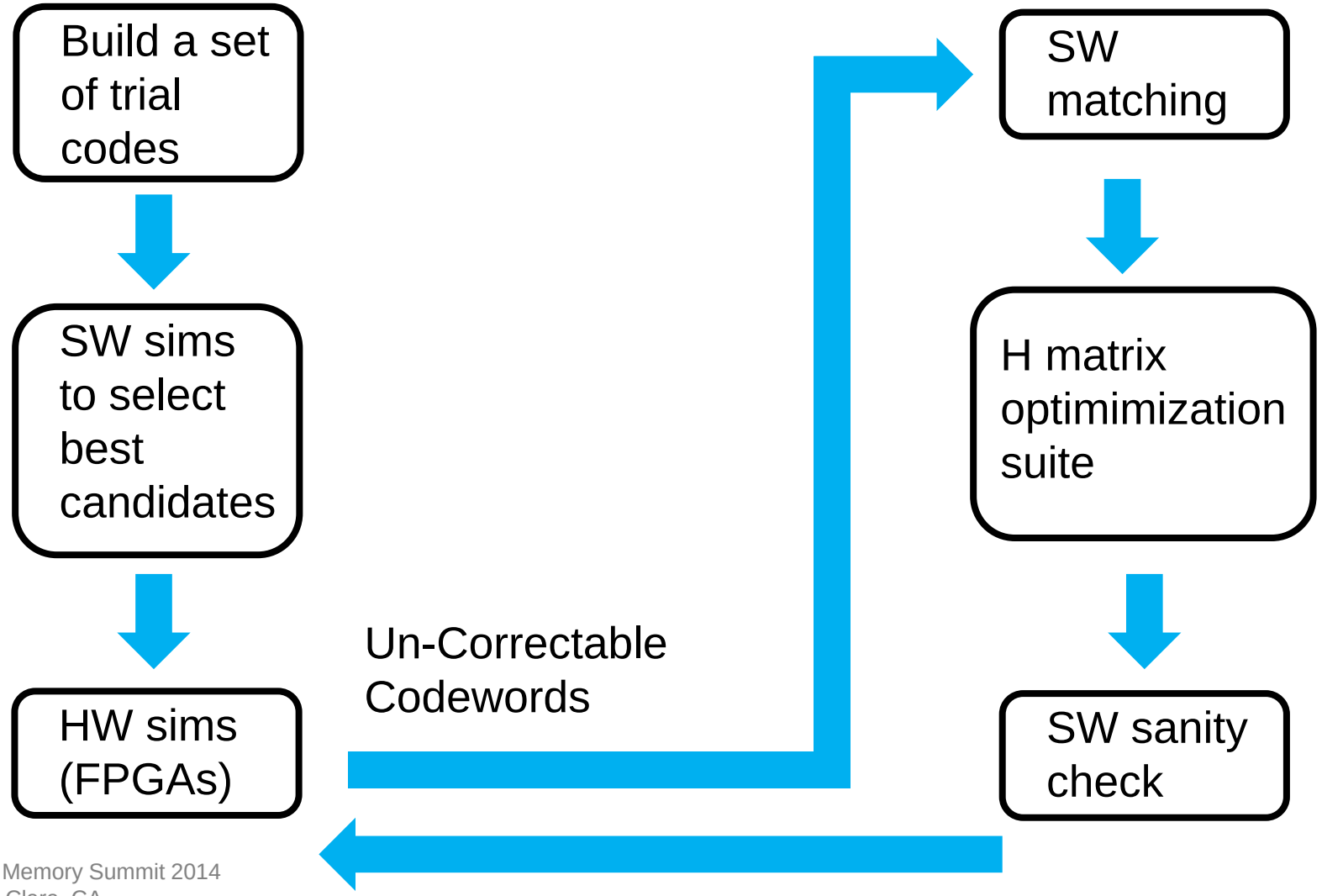
Error Floor



H Matrix Development

- How to build a quality H matrix in as short a time as possible?
- May have to consider waterfall and floor performances
- Deep floor area (FER < 10^{-10}) very difficult to determine, hard to calculate and very difficult to simulate as the required FER is reduced
- Must be certain that actual hardware component itself also meets the FER requirements

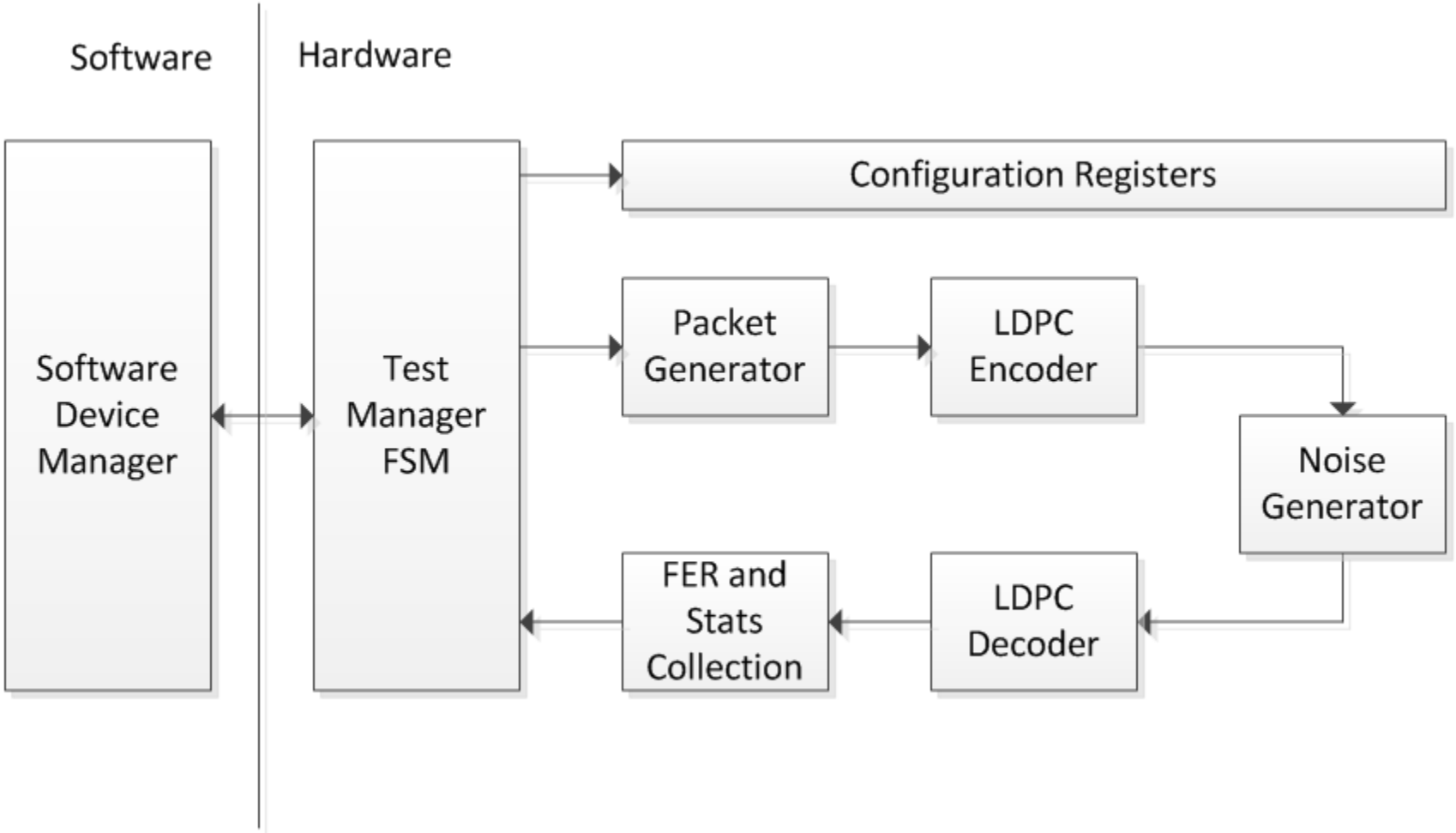
HW/SW Co-Simulation Flow



Building a Trial Code

- Use a Software process
- Select H matrix parameters (rate, rows, columns, parity style, degree of columns and rows,…)
- Choose the construction method amongst all possibilities
- Density evolution, cycle breaking, etc.

HW Co-Simulator



Code Updating Procedure

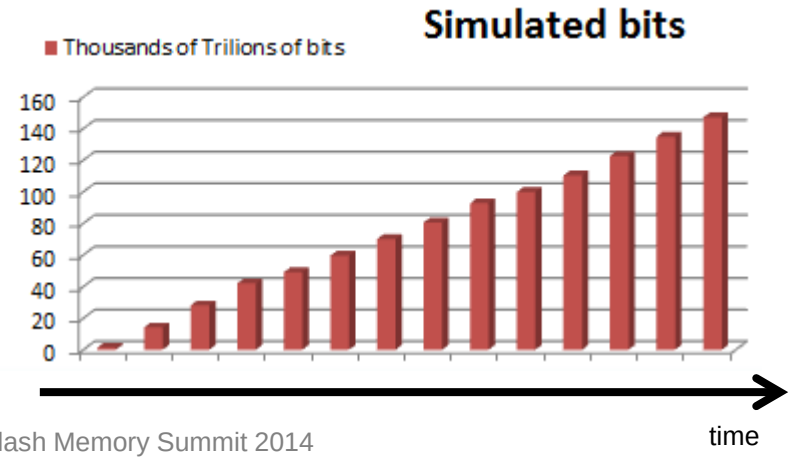
- Recover and reproduce all uncorrectable packets in software
- Categorize failure conditions
  - Standard frame error (large number of bit errors)
  - Hardware fault (un-reproducable)
  - Trap condition
  - etc.
- Analyze Trap Conditions to root-cause
- Modify the current candidate to avoid as many traps as possible

Hardware Platforms / Throughput

- As much throughput as possible! Multiple Engines per FPGA & multiple FPGAs
- Silicon accurate implementations on FGPA for Encoder and particularly the Decoder
- We must also verify real ASIC implementation: subtle faults can create a false floor
- Minimize cost for re-creating error conditions
- Potentially dealing with 1e3 or 1e4 interesting FEC blocks

Simulation Speed

- FPGAs are the answer
- Hundreds of thousand of trillions of bits can be simulated



Highlights

- LDPC are very effective but suffer from error floor
- SW is great to find good H matrices
- FPGAs are the only viable way to prove that error floor is below the FER target
- By SW-HW Co-Simulation H matrix can be improved
- Hundreds of thousand of trillions of bits can be simulated in a reasonable timeframe

Thank You!

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