Low-Power Error Correction for Mobile Storage

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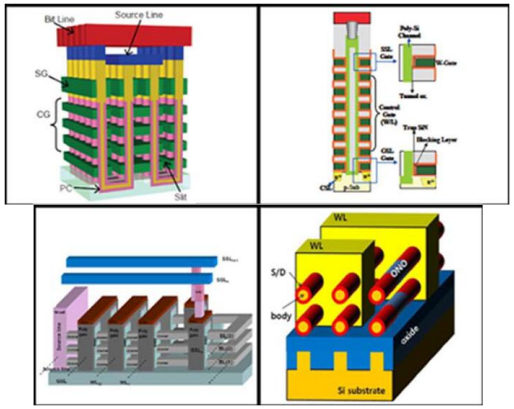
Power Consumption

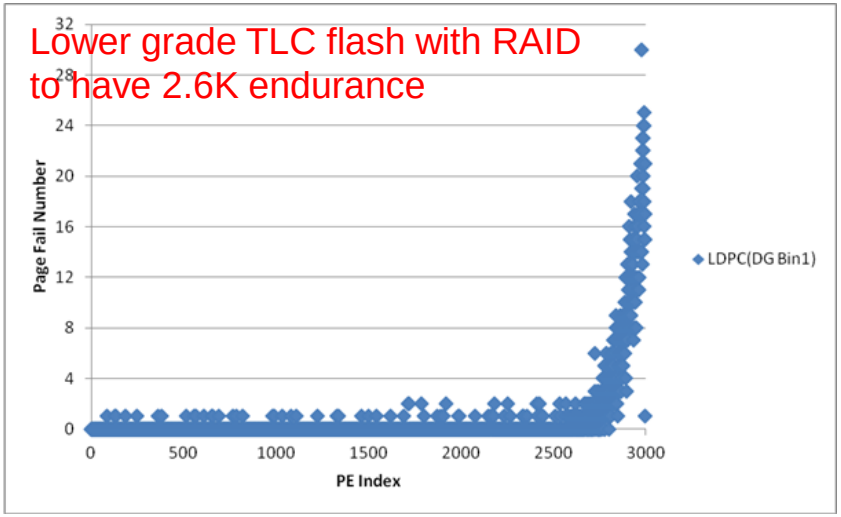
- The ECC engine will consume a great percentage of power in the controller
- Both RAID and LDPC become crucial to high reliable flash controller, which is employed in embedded applications.
- Stronger correction capability
  - Longer ECC chunk (e.g., 2KB BCH is stronger than 1KB, and 2KB LDPC is much stronger than 1KB)
  - Higher decoder resolution and parallelism architecture will reduce the decoding latency.
  - Higher power consumption.
- Wider range corrupt data recovery
  - Larger RAID recovery range will provide wider range data recovery.
  - Consume more memory size and calculation logic.
  - Higher power consumption.
- In normal operation…
  - For RAID engine, only the encoder part is active all the time.
  - LDPC uses the hard-decoding only, but the encoder is always active in each flash write action.
- Power consumption reduction in hot region
  - RAID encoding
  - LDPC decoding

RAID Engine

- The SSD module failure rate will be the Key for TLC adoption on SSD.
- Latest Planar NAND might be 1znm.
  - Bit column, sense-Amp, address decoder, or charge pump corrupted
  - WL lining or WL to WL short.
- First popular 3D structure on BiCs.
  - Inherit most of failure cases from 2D.
  - High aspect ratio etching and larger number of layers control will contribute more failure cases.
- No Erase/Program failure, but with reading ECC failure.
  - Need RAID engine to do the error recovery.
  - In 3D TLC, three WL lining may cause data loss over 9 pages.
- High efficiency RAID with erasure decoding.
  - Encoding with high efficiency memory access.
  - Memory access dominates the encoding power.
  - Low RAID recovery trigger rate.

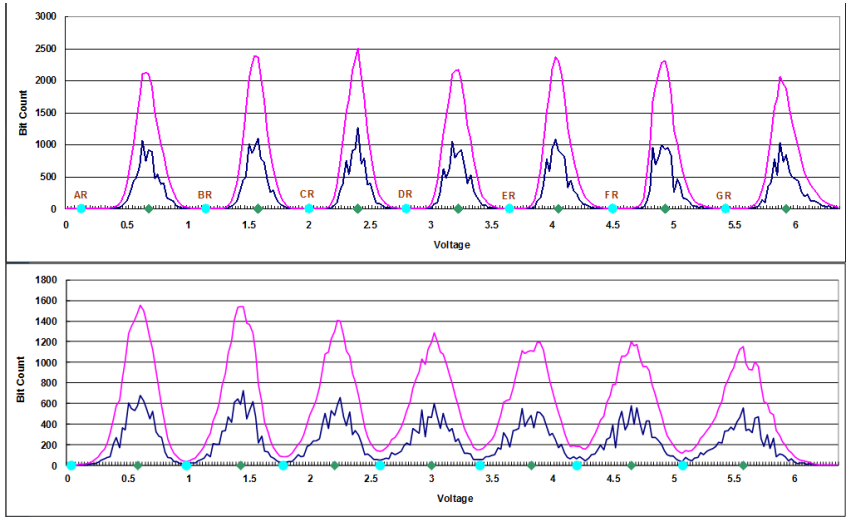


[Ref]: VLSI symp. 2009, pp.136-137, VLSI symp. 2008, pp. 192-193
VLSI symp. 2010, pp. 131-132,
IEEE Trans. Electron Devices, vol.58, no.5, pp. 1006-1014, Apr.2011

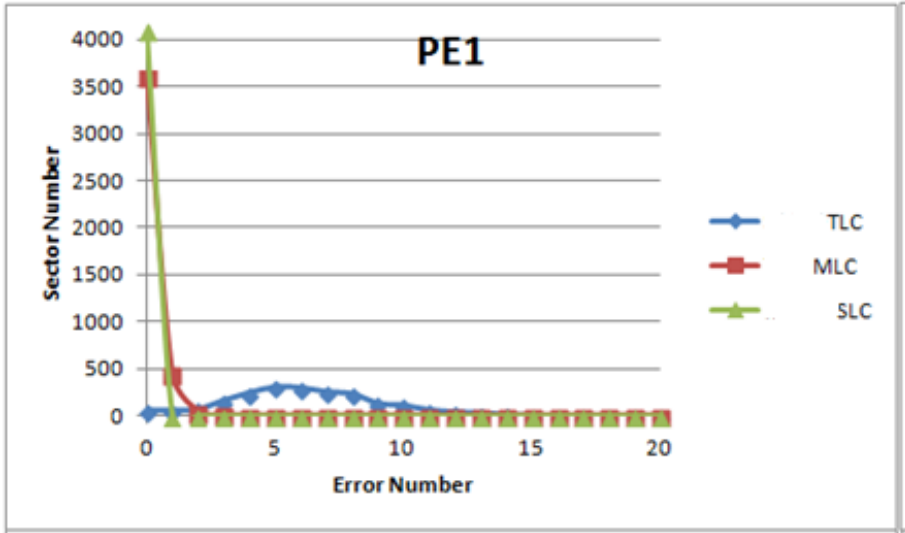


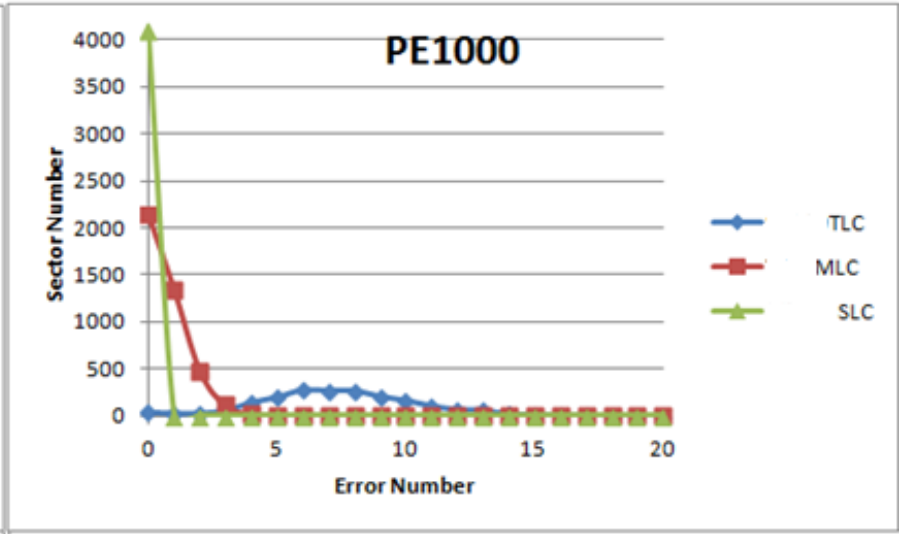
DSP Engine Power Consumption

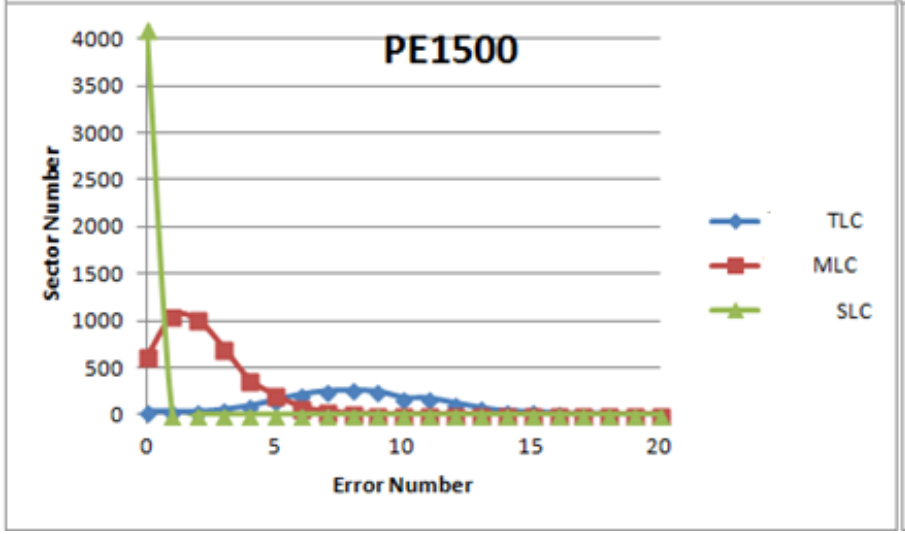
- NAND Flash characteristics on Endurance and Retention.
- Retention capability on TLC degrades rapidly as P/E cycle increases.
- Reduce the power with Retention-aware algorithm:
  - Predict the sensing point in the first read.
  - Joint the soft-decoding and the Vt-tracking.
  - Minimize the number of read operation
- The error bit number is the key factor of power consumption.
  - Sensing the data which has lowest bit error rate
  - Predict error types and select the decoding strategy.

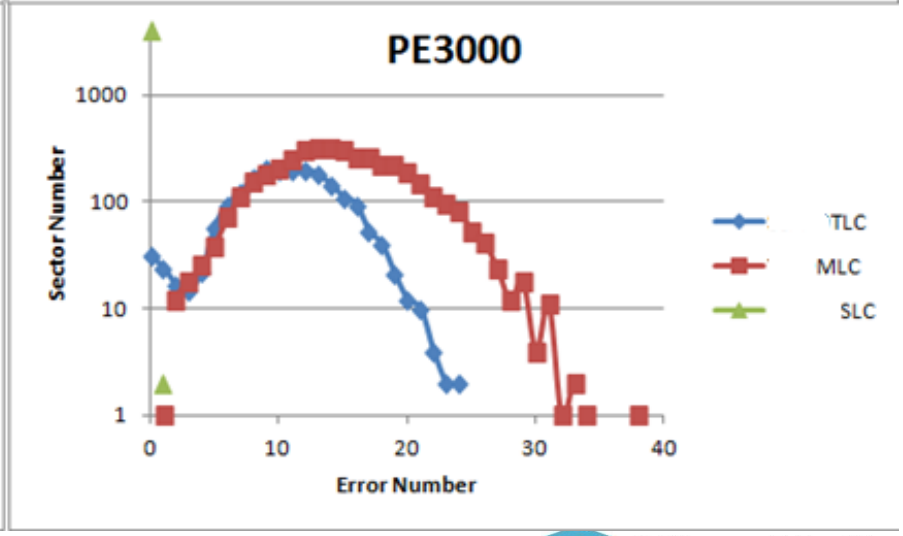


NAND characteristic. SLC/MLC/TLC

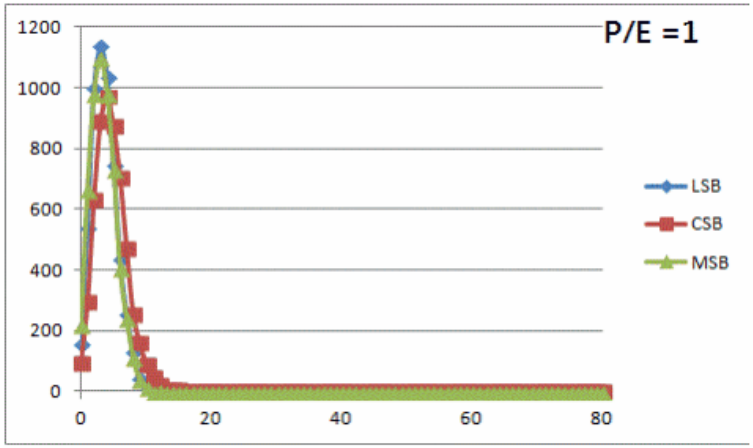




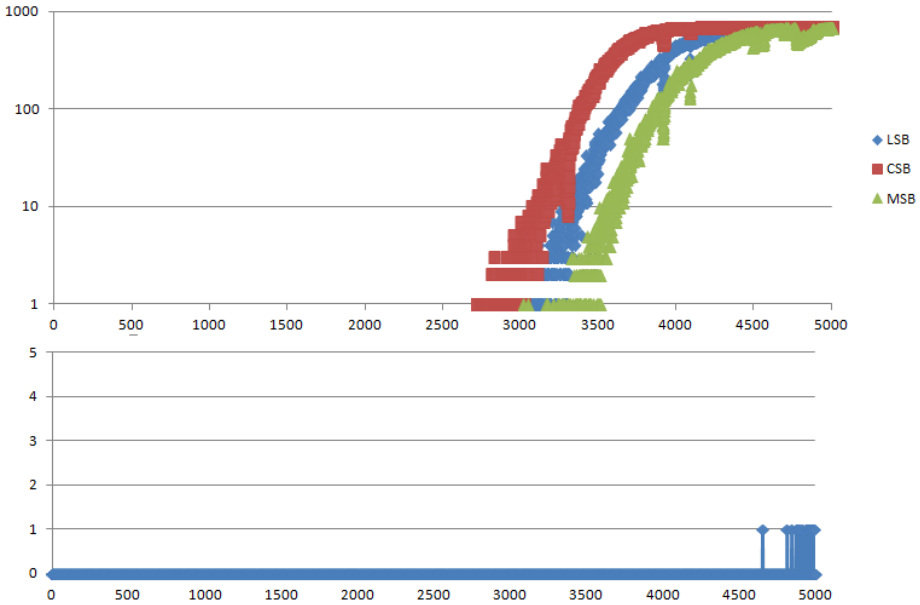




TLC Error Behavior on Endurance

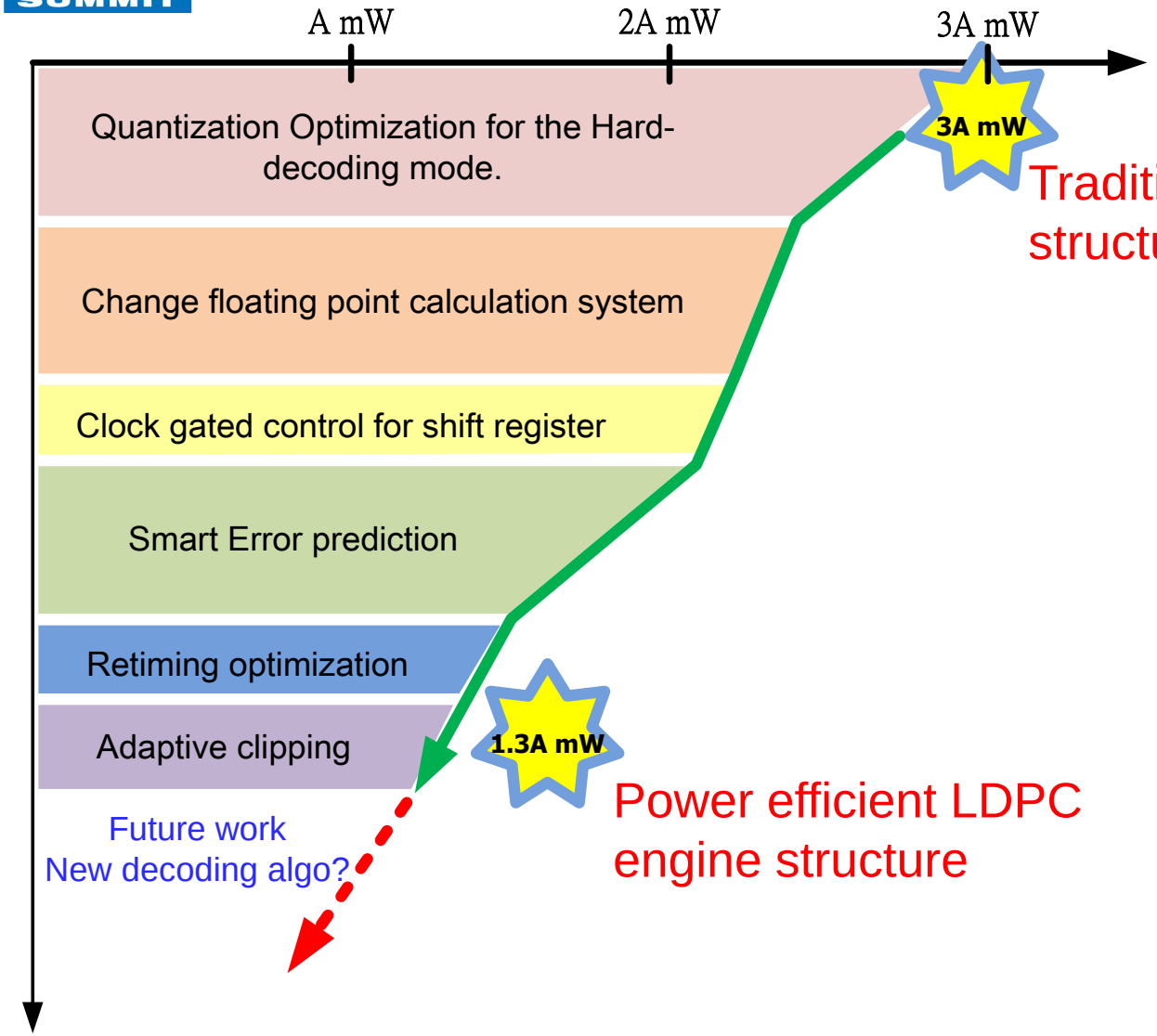


- X: Number of error bit
- Y: Number of ECC chunk
- Endurance 2K, 90% of the error bit number is less than 30 bits
- 2K: CSB-RBER = 2.7e-3
- 1K: CSB-RBER = 1.3e-3



- Soft-decoding/RAID trigger rate
- X: P/E cycle
- After the 2.7K cycling, it needs LDPC soft-decoding.
- RAID redundant overhead ~ 0.07%.
- Double strong endurance from LDPC hard to soft decoding.
- First RAID recovery occurs on 4.5K cycles.

LDPC Low Power Decoding Technology



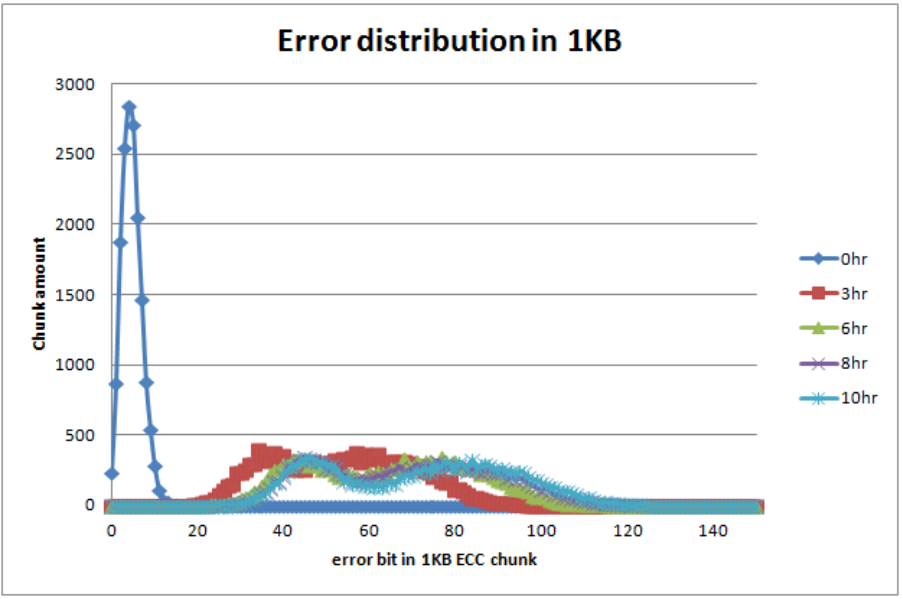
1KB BCH vs. LDPC decoding power consumption TSMC40nm on TLC flash

Error bit range /1KB	BCH	LDPC	NOTE
1~20 bit	A mW	0.9A mW	~400MB/sec
20~40 bit	B mW	1.4B mW	~400MB/sec
40~60 bit	C mW	2.6 C mW	~300MB/sec

Endurance	BCH	LDPC	NOTE
0~1K P/E	A mW	0.9A mW	Hard-bit only
1.~2K	B mW	1.4B mW	Hard-bit only
2K~5K	NA	2.6C mW, poor throughput	soft-decoding trigger frequently .

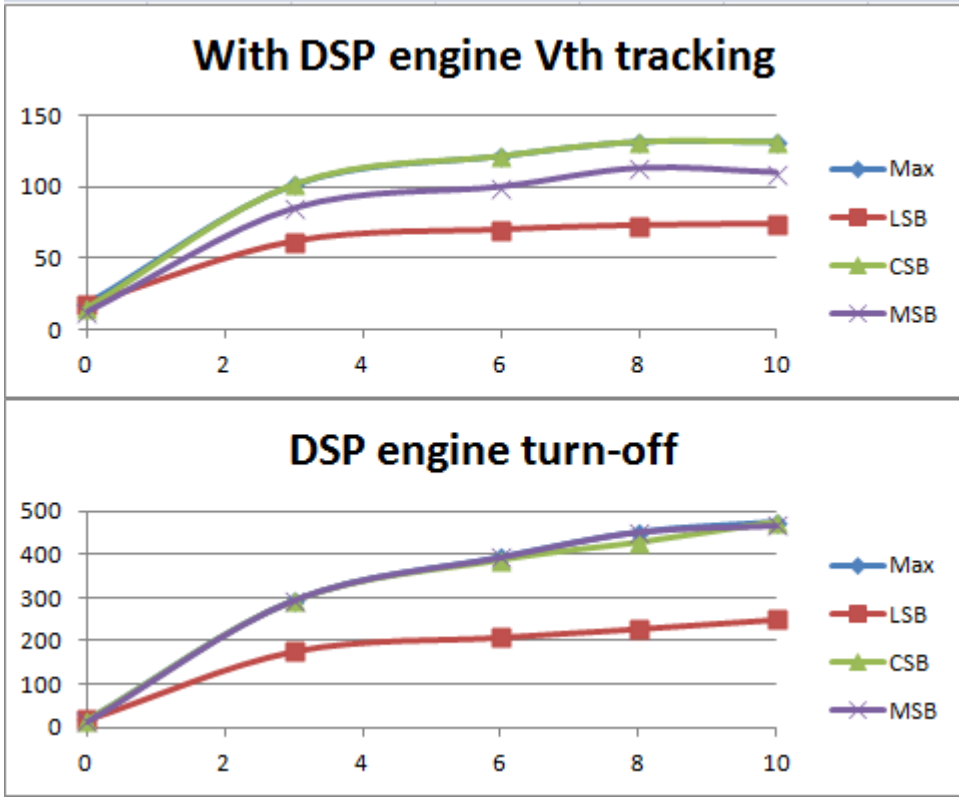
If requirement is 1K cycles, Will be the BCH enough to support the TLC?

After Data Retention at 500P/E



125C

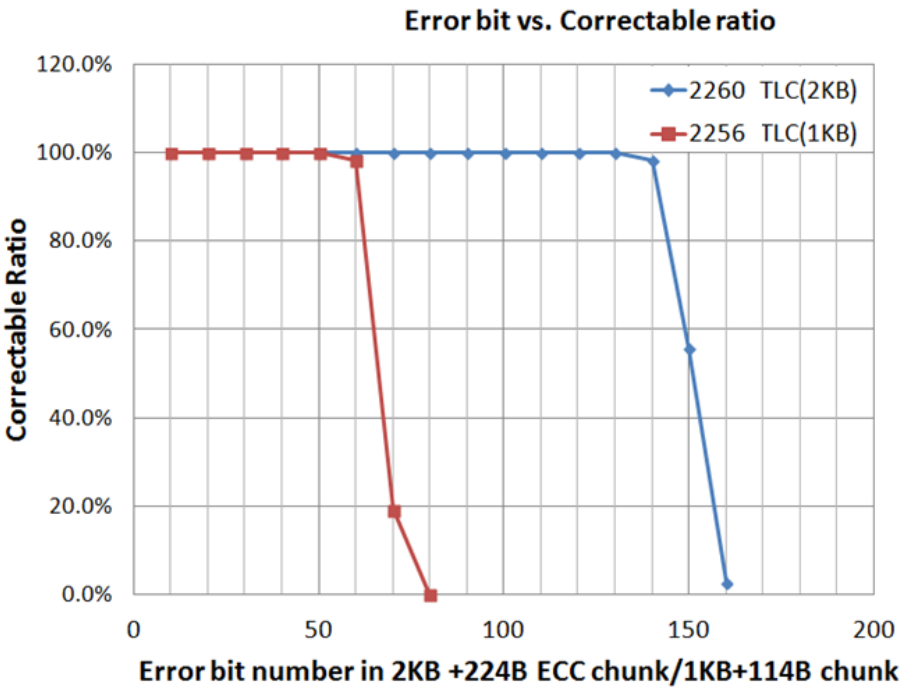
hr	BCH	LDPC	Soft decode trigger	RAID trigger	Max err	RBER
0	o	o	0	0	19	0
3	x	o	0.556686047	0	102	0.000366
6	x	o	0.668120155	0	122	0.000732
8	x	o	0.687015504	0	132	0.000977
10	x	o	0.710755814	0	132	0.001221



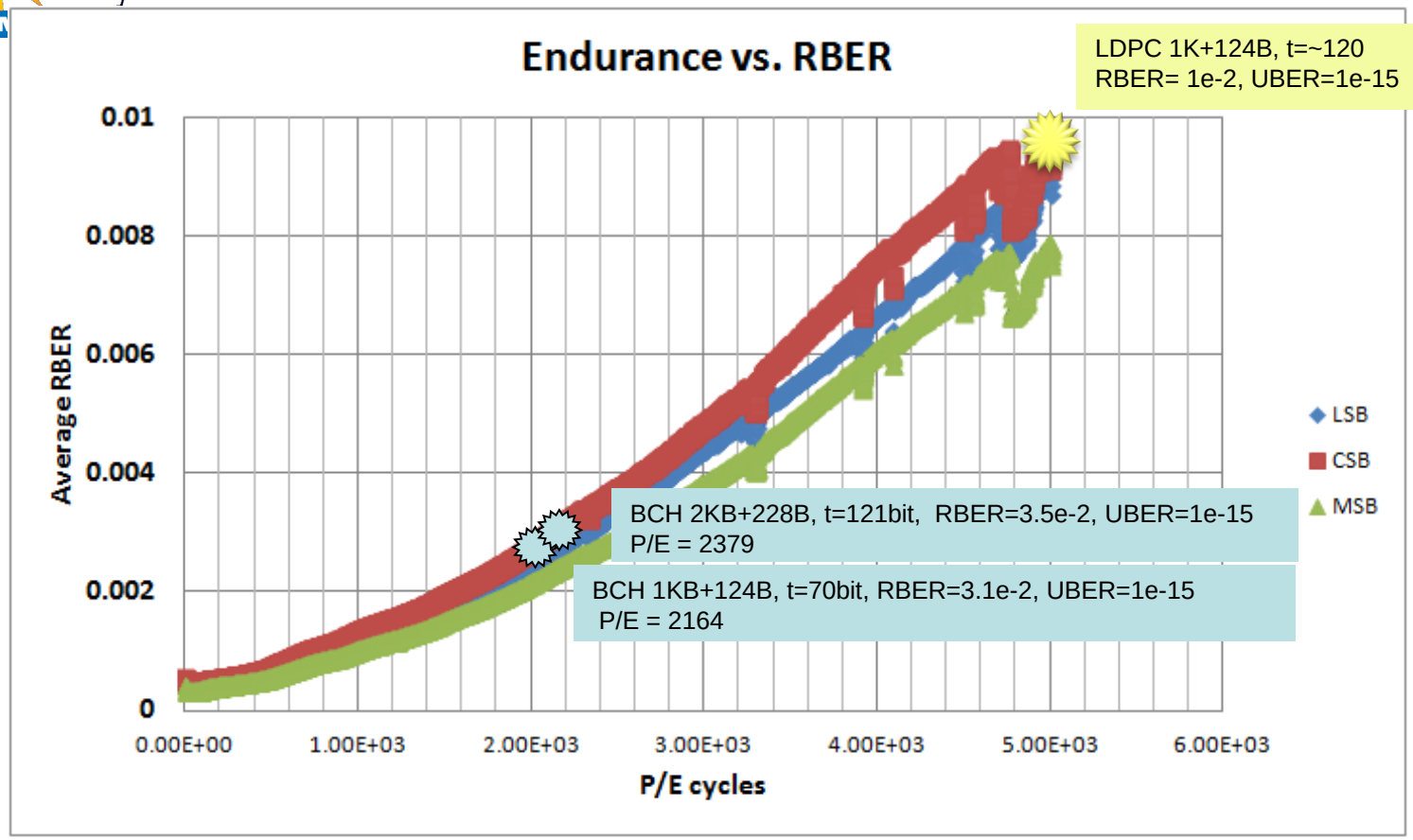
Comparison between 1KB and 2KB

- Error bit under 2KB chunk is 110bit.
  - Almost 100% correctable rate for Hard-decision only.
  - 851 MB/sec under 400MHz operation frequency.
- When the error bit under 1KB chunk is 60bit.
  - Almost 100% correctable rate for Hard-decision only.
  - 330 MB/sec under 400MHz operation frequency.
- 1KB vs. 2KB under the same error condition

	1KB/60bit	2KB/110bit
Area (gate)	1A	1.8A
TP (@400MHz)	330 MB/sec	851 MB/sec
Power (W)	1A	2.15A
Power Efficiency	1A MB/J	1.2A MB/J
Area Efficiency (per gate)	1A B/s	1.4A B /s
UBER=1e-15	RBER=1e-2	RBER=1.25e-2



Ideal Solution for TLC-based SSD



- The 2KB BCH engine only has limited improvement on endurance and retention.
- LDPC ideally fits TLC and maximizes the endurance of TLC-based SSD solution.
- LDPC + RAID is the ONLY reliable solution for TLC-based SSD.

THANK YOU!

Q & A

Disclaimer Notice
Although efforts were made to verify the completeness and accuracy of the information contained in this presentation, it is provided “as is” as of the date of this document and always subject to change.