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LDPC CODES WITH LOW ERROR-FLOOR

(Invited Paper)

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Remark: This work was done at the UC-Davis
while Dr. Diao was a Ph.D Student from 2011-2013.

I. Performance of an LDPC Code

- The performance of an LDPC code with iterative decoding is measured by:

  1. The error performance (or coding gain or how close to the Shannon limit),
  2. The rate of decoding convergence (how fast the decoding process terminates),
  3. Error-floor (how low the error rate can achieve).

Error-Floor

II. Performance Factors

- The performance of an LDPC code is determined by a number of structural properties collectively:

  1. Minimum distance (or minimum weight);
  2. Girth of its Tanner graph;
  3. Cycle distribution of its Tanner graph;
  4. Connectivity;

5. Trapping set configurations and distribution of its Tanner graph;
6. Degree distributions of variable and check nodes of its Tanner graph;
7. Row redundancy of the parity-check matrix,
8. Other unknown structures

- No single structural property dominates the performance of a code.
- It is still unknown how the code performance depends on the above structural properties analytically as a function.

III. Categories of Constructions

- Major methods for constructing LDPC codes can be divided into two general categories:

  1. graph-theoretic-based constructions
  2. algebraic-based methods

- Most well known graph-theoretic-based construction methods are PEG (progressive edge growing) and protograph-based methods.

- Algebraic constructions of LDPC codes are mainly based on finite fields, finite geometries, and combinatorial designs.

- Algebraic constructions, in general, result in mostly QC-LDPC codes, especially QC-LDPC codes whose parity-check matrices are arrays of circulant permutation matrices (CPMs) and/or zero matrices (ZMs).

- We refer to this type of QC-LDPC codes as codes with CPM-structure or CPM-QC-LDPC codes.

- QC-LDPC codes have advantages over other types of LDPC codes in hardware implementations of encoding and decoding.

- Encoding of a QC-LDPC code can be efficiently implemented using simple shift registers.

- In hardware implementation of a QC-LDPC decoder, the quasi-cyclic structure of the code simplifies the wire routing for message passing.

- Well designed QC-LDPC codes perform as well as any other types of LDPC codes in the waterfall region.

- All these advantages inevitably will make QC-LDPC codes the mainstream LDPC codes for future applications in communication and storage systems.

- Algebraic LDPC codes in general have lower error-floor and their decoding converges faster than graph-theoretic-based LDPC codes.

IV. A Very Low Error-Floor RS-Based QC-LDPC Code

- Let α be a primitive element of the field $GF(2^7) = \{0, 1, \alpha, \alpha^2, \ldots, \alpha^{126}\}$ which consist of 128 elements.

- For the following 6x127 matrix over $GF(2^7)$:

$$B = \begin{bmatrix} 1 & \alpha & \alpha^2 & \cdots & \alpha^{126} \\ 1 & \alpha^2 & (\alpha^2)^2 & \cdots & (\alpha^2)^{126} \\ 1 & \alpha^3 & (\alpha^3)^2 & \cdots & (\alpha^3)^{126} \\ 1 & \alpha^4 & (\alpha^4)^2 & \cdots & (\alpha^4)^{126} \\ 1 & \alpha^5 & (\alpha^5)^2 & \cdots & (\alpha^5)^{126} \\ 1 & \alpha^6 & (\alpha^6)^2 & \cdots & (\alpha^6)^{126} \end{bmatrix}$$

- The base matrix $\boldsymbol{B}$ is the conventional parity-check matrix of a cyclic (127, 121) Reed-Solomon code over GF(2^7) whose generator polynomial has α, α^2, α^3, α^4, α^5, α^6 as roots.

- Dispersing each entry in $\boldsymbol{B}$ by a 127×127 CPM, we obtain a 127×127 array $\boldsymbol{H}$ of CPMs of size 127×127.

- $\boldsymbol{H}$ is a 762×16129 matrix with column and row weight 6 and 127, respectively. The rank of this matrix is 757. $\boldsymbol{H}$ has 5 redundant rows.

- The null space of $\boldsymbol{H}$ gives a (6, 127)-regular (16129, 15372) QC-LDPC code C with rate 0.953.

- The Tanner graph $\mathcal{G}$ of the code C has girth 6 and each variable node of $\mathcal{G}$ has a large degree of connectivity.

- $\mathcal{G}$ has no small trapping set with size smaller than 11.

- With 50 iterations of the MSA, the code achieves a bit-error rate (BER) of 10^{-15} and a block-error rate (BLER) of almost 10^{-12} without visible error-floors

- The bit and block error performances of this QC-LDPC code decoded with 5, 10, 50 iterations of the min-sum algorithm (MSA) with a scaling factor 0.75 are shown in Fig.1 (computed with an FPGA decoder).

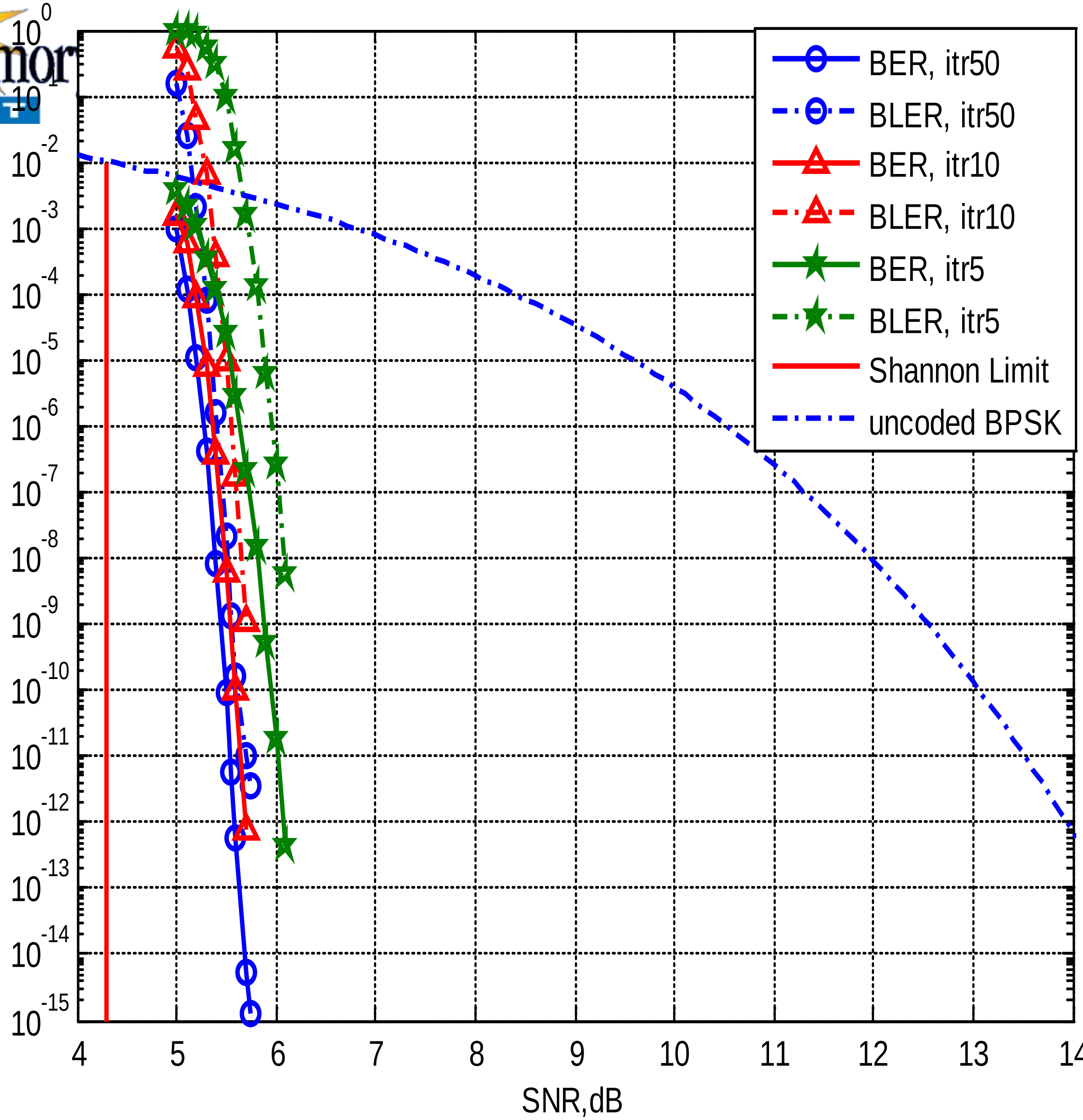

Figure 1: Performances of the (16129,15372) QC-LDPC code calculated by an FPGA decoder.

V. Important Decoder Implementation Issues

- Number of logic gates (or number of message processing units);
- Number of wires connecting the message processing units;
- Memory requirement;
- Power consumption;
- Decoding latency.

VI. Conclusion

- To construct LDPC codes with good waterfall error performance and very low error-floor, algebraic construction is the way to go.

- A solution to the decoder implementation is the Merry-Go-Round decoder architecture.

- This presentation is simply an academic point of view.

Thank you!