Is it possible to transform a native TLC- NAND into an enterprise-MLC?

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Outline

- TLC challenges
- New technologies for transforming TLC into MLC:
  - 4LevelER
  - Hi-Track
  - CLAP-LDPC
- Summary

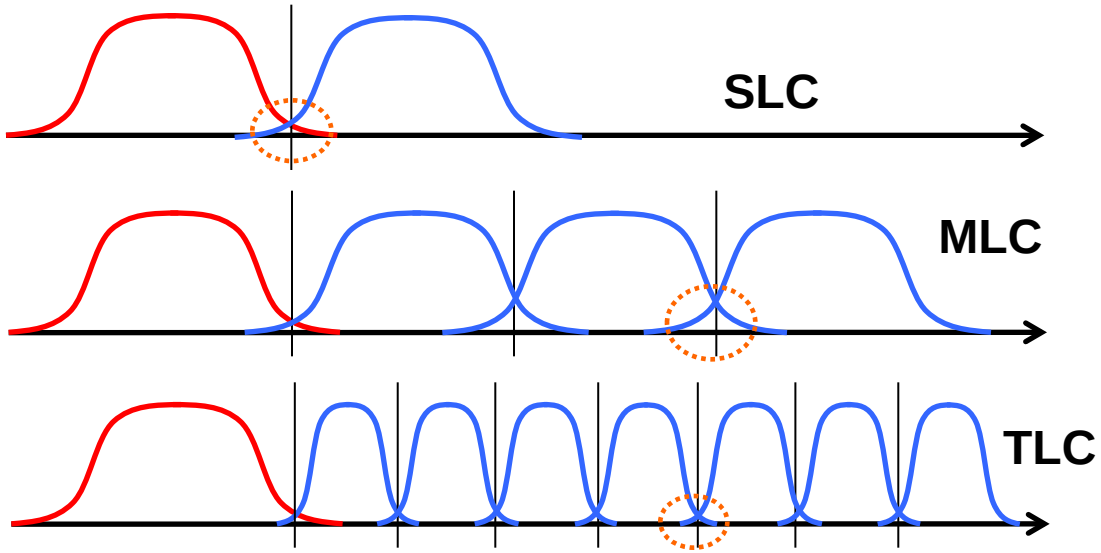
TLC Challenges

- TLC reliability prevents its adoption in systems where more than few hundreds of P/E cycles are required, but it is cost effective
- Flash vendors charge a premium for enterprise MLC (it is usually same silicon as standard MLC but with different settings)
- Can we buy TLC and use it as eMLC? This would enable: cost reduction, procurement flexibility, hybrid TLC/MLC/SLC storage

From TLC to MLC

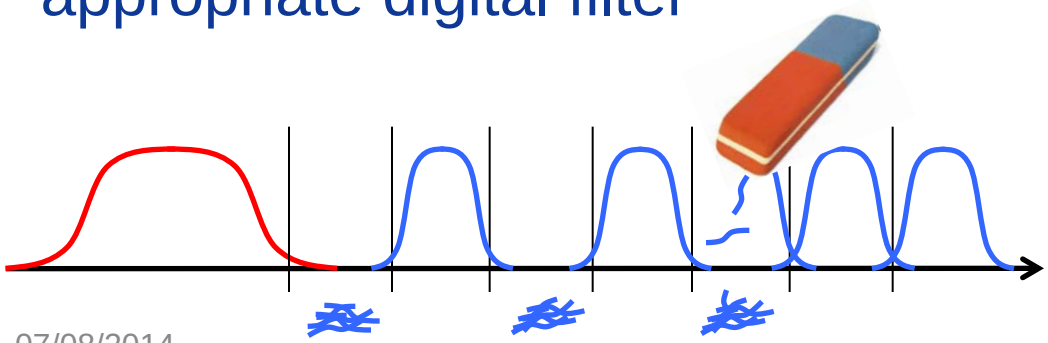
- A lot of Flash management routines are widely adopted (wear leveling, read scrubbing, read retry, data randomization...) to make NAND more reliable
- LDPC is becoming popular @1x nm
- Additional technologies are required for promoting TLC to a “reliable” MLC
- 4LevelER, Hi-Track, and CLAP-LDPC technologies are introduced to fill the gap

NAND Distributions



- Distribution overlaps limit reliability because BER exceeds the Shannon limit

- TLC distributions can be deleted by applying an appropriate digital filter



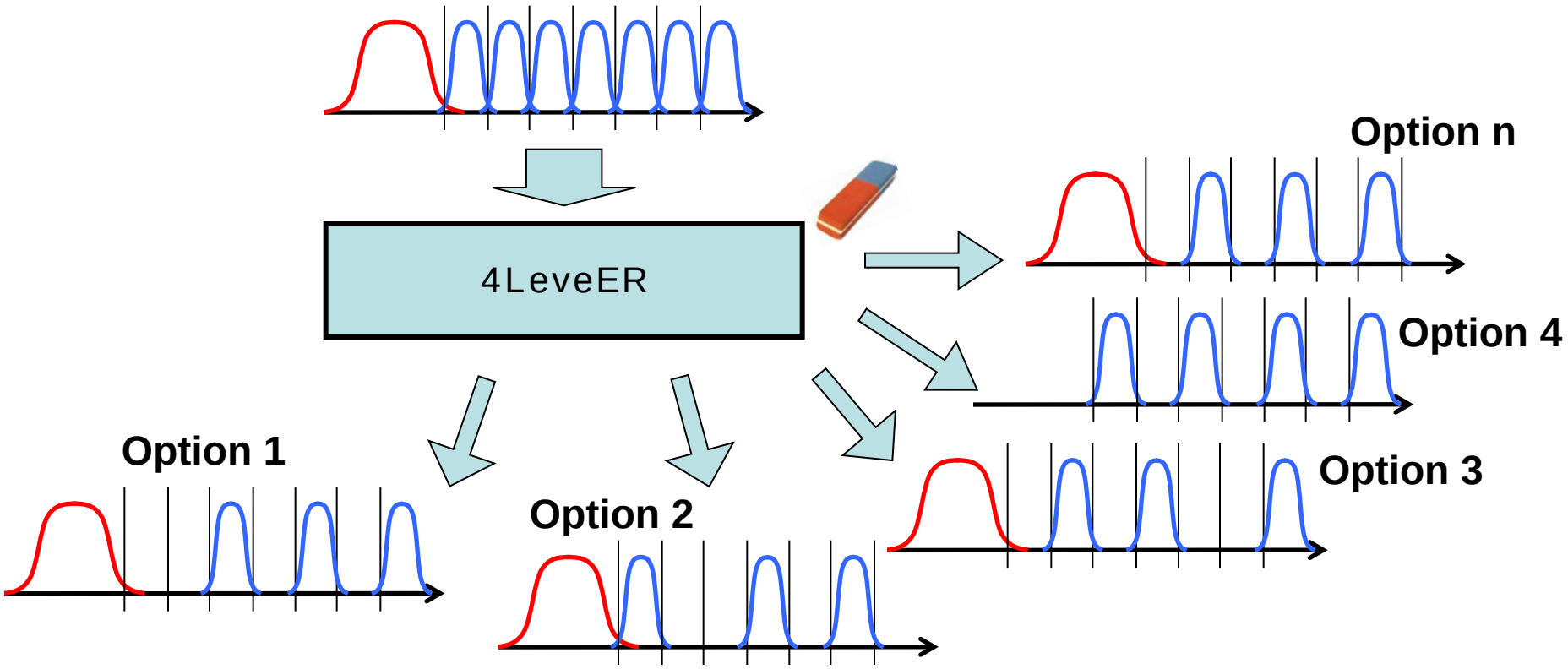
4LevelER technology

Distribution Selection -> “4LevelER”

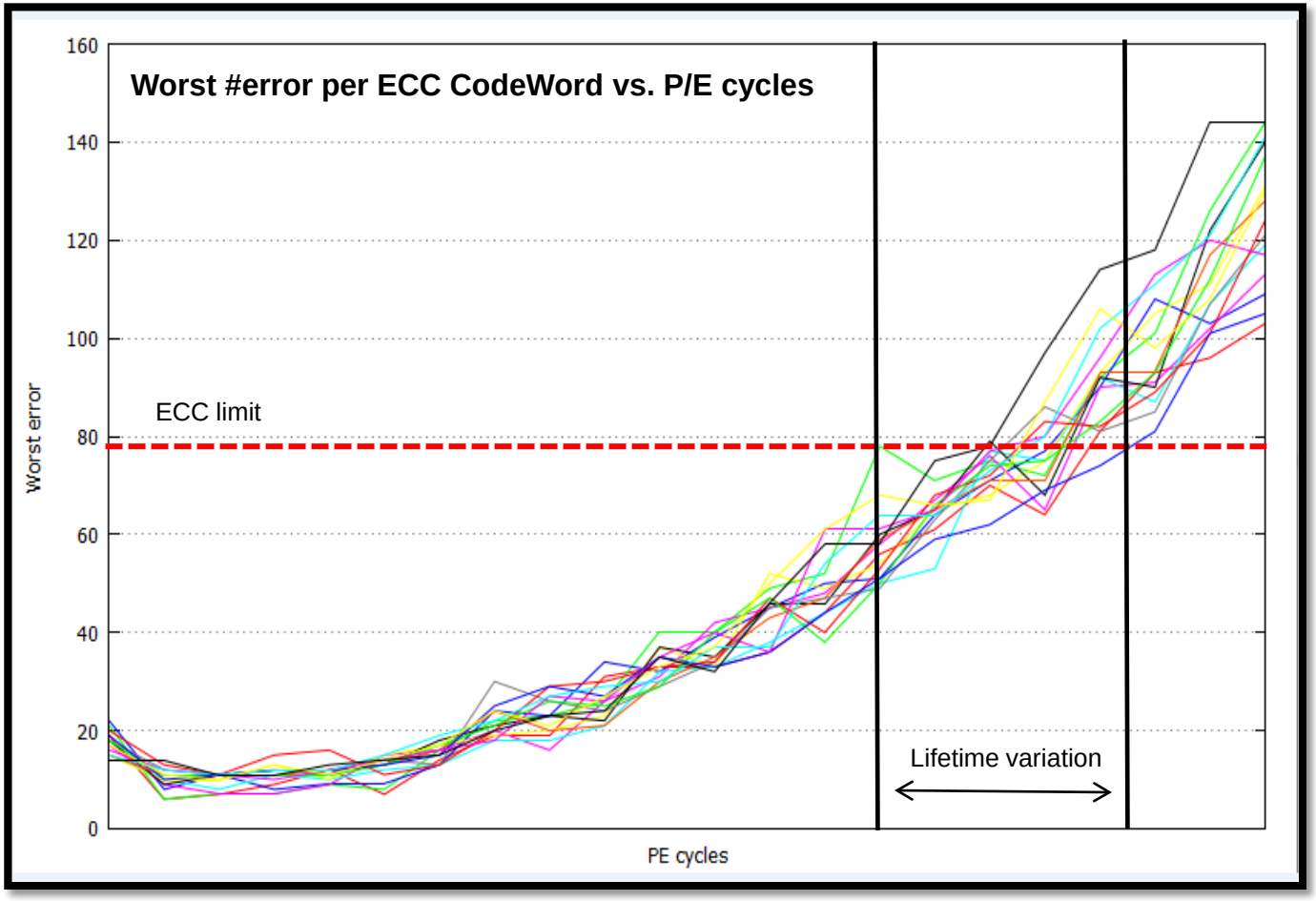
- From TLC to MLC, 4 distributions can be removed
- There are a bunch of different options
- Depending on the application, number of P/E cycles, retention, etc., the best option is different
- “4LevelER” technology enables the right selection by maximizing the distance between specific distributions
- Removal is done by applying a digital filter on incoming data

4LevelER

- Task of the 4LevelER is to select and Erase 4 Levels from commercial TLC

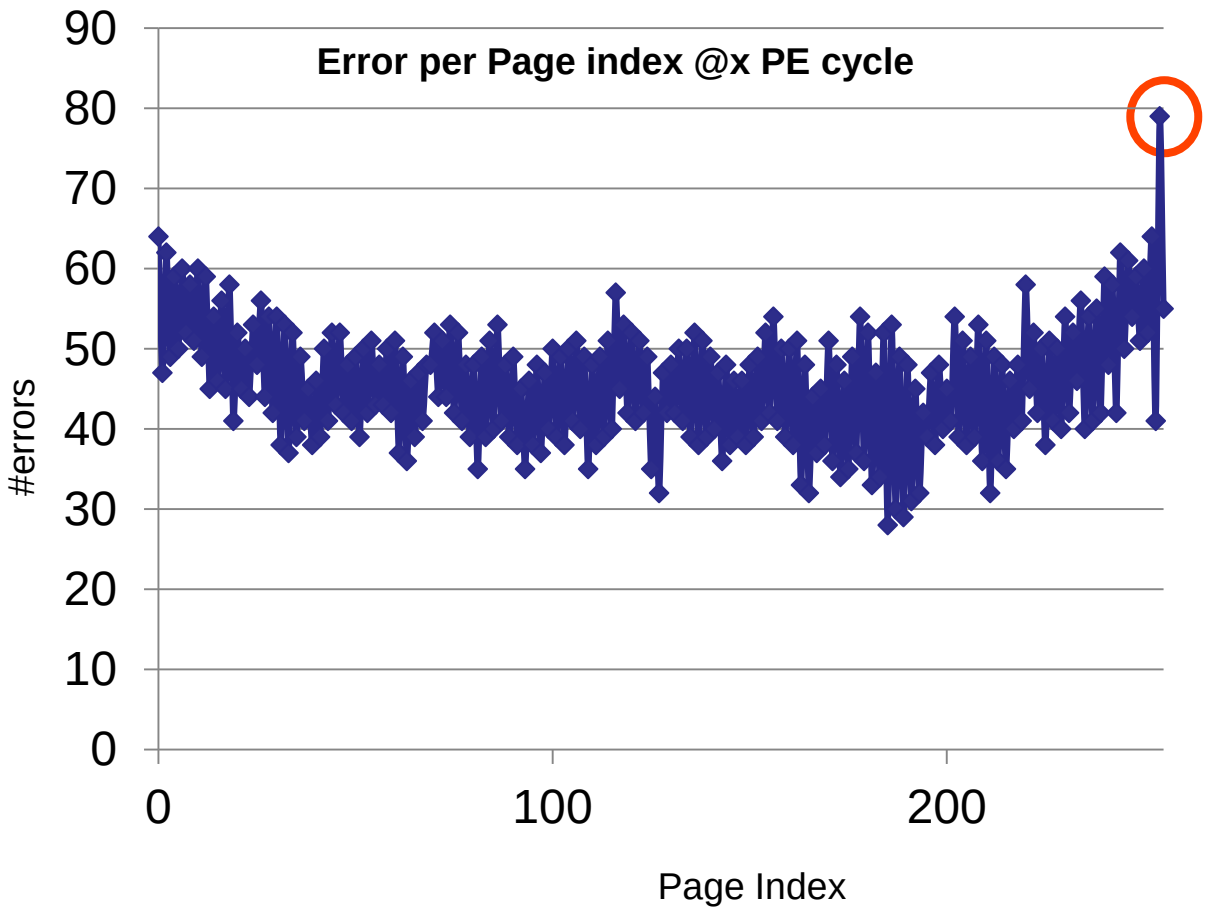


BER variations



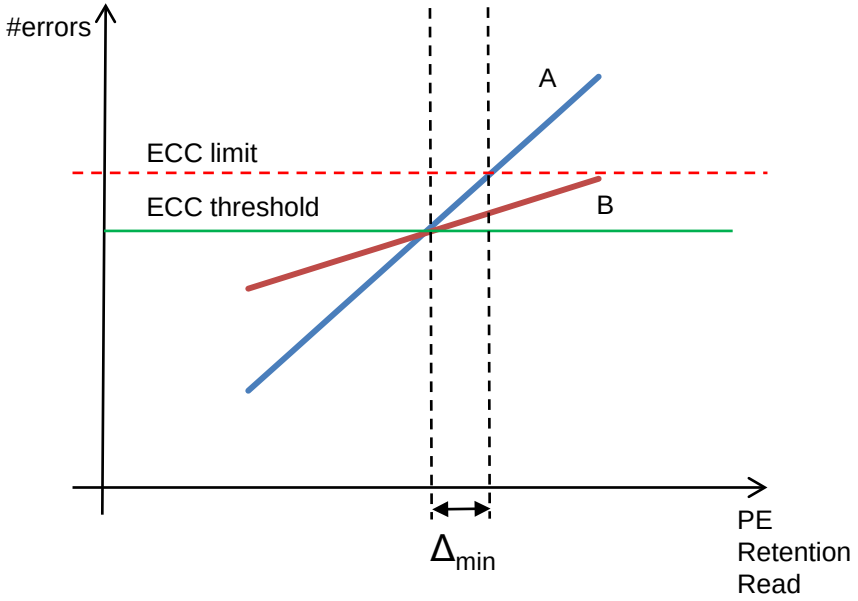
- 2x nm NAND
- Different lines -> different blocks
- When a page hits the ECC limit, the block is usually retired
- Lifetime variation is significant
- Capacity drop is used to determine SSDs EOL

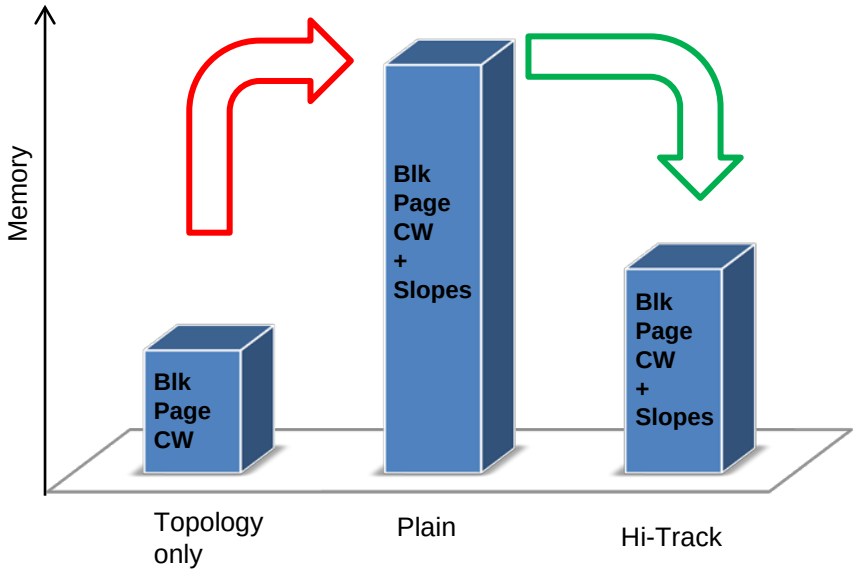
Hi-Track (History-Tracker)



- One page or few pages are worse than others
- In this example, block reclaim is due to a single page
- Reclaim at page level extends the lifetime
- Tracking the history of each page (or even codeword) requires computing power and memory
- Hi-Track technology enables a detailed tracking at a reduced cost

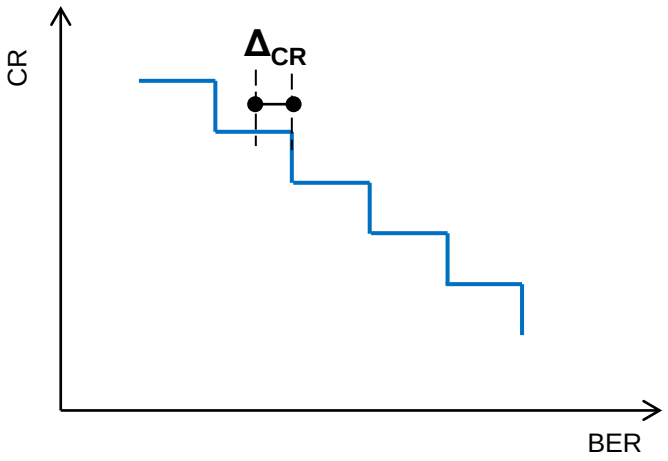
Hi-Track -> BER slopes

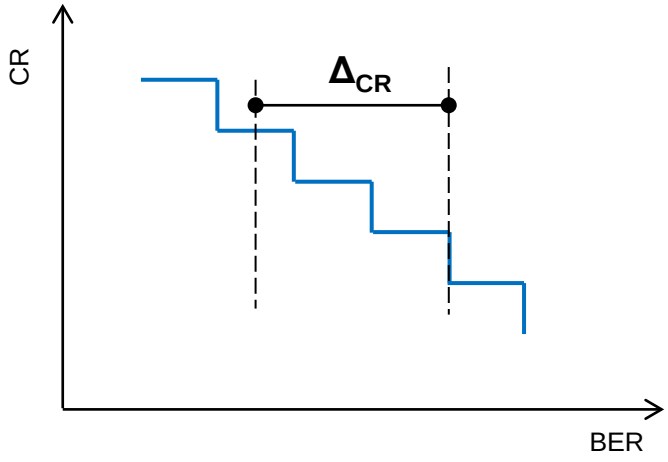




- Δ_{min} guarantees that CWs are still correctable at the next “check” point
- Blocks A and B hit the ECC threshold at the same time
- If we knew the slope, B could keep going
- Hi-Track minimizes the memory requirements for tracking topology and slopes

Multi Code-Rate LDPC





- LDPC w/ Multi-Code-Rate is becoming popular
- Multi-CR works fine in theory, but "switching margin" (Δ_{CR}) is a killer in practice
- Δ_{CR} is a design margin because Flash management algos use thresholds
- Δ_{CR} burns capacity sooner than needed
- Some Flash controllers provides a lot of CRs, but some of them fall within Δ_{CR} and can't be used

CLAP-LDPC

- In order to exploit the full benefit of Multi-Code-Rate solutions, we need to remove/reduce Δ_{CR}
- CLAP-LDPC (CLosed Abstracted Proactive LDPC) is introduced
- CLAP-LDPC implements advanced decoder / H matrix
- “Closed” -> decisions are based on decoding parameters -> switching margins are strongly reduced
- “Abstracted” -> first order, it doesn’t depend on a specific NAND technology
- “Proactive” -> it automatically triggers the CR change
- It can be combined with Hi-Track to remove Δ_{CR}

Summary

- TLC can be promoted to a reliable MLC
- Besides the standard Flash Signal Processing, we introduced 3 new technologies
- 4LevelER
  - to properly choose which distributions to use
- Hi-Track
  - to keep track of ECC CodeWords history
- CLAP-LDPC
  - to exploit the full benefit of Multi-Code-Rate LDPC

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Thank You