System Design for mainstream TLC SSD
Meeting the performance challenge

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Forward-Looking Statements

During our meeting today we may make forward-looking statements.

Any statement that refers to expectations, projections or other characterizations of future events or circumstances is a forward-looking statement, including those relating to industry and market trends and future memory technology and performance. Information in this presentation may also include or be based upon information from third parties which reflects their expectations and projections as of the date of issuance.

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We undertake no obligation to update these forward-looking statements, which speak only as of the date hereof.

Agenda

- **MLC, TLC Raw NAND comparison**
- **TLC NAND Attributes and Challenges**
- **TLC SSD: Bridging the Performance Gap with MLC SSDs**
- **Optimal use of DRAM**
- **NAND Parallelism for optimal performance**
- **Tiered Storage Approach**
- **The SLC advantage**
- **Writes to TLC**
    - **Direct**
    - **TLC writes via SLC**
- **Further performance improvement techniques**
- **Knobs to fine tune cost vs. performance**
- **Performance Comparison**
- **Conclusion**

MLC, TLC Raw NAND comparison

Metrics	2 Bit Per Cell (MLC) 1ynm 64Gb/128Gb *	3 Bit Per Cell (TLC) 1ynm 64Gb/128Gb **	
Read (Page)	45 us	80 us	(Lower Page)
		105 us	(Middle Page)
		80 us	(Upper Page)
Program (Page)	1350 us	550 us	(First Cycle)
		1700 us	(Second cycle)
		4650 us	(Third Cycle)
Erase (Block)	4 ms	10 ms	

*   **SanDisk 1Ynm 128 Gb eX3 datasheet**
** **SanDisk 1Ynm 64 Gb eX2 datasheet**

SLC: Single level cell
MLC: Multi level cell
TLC: Three level cell

TLC NAND Attributes and Challenges

Cost
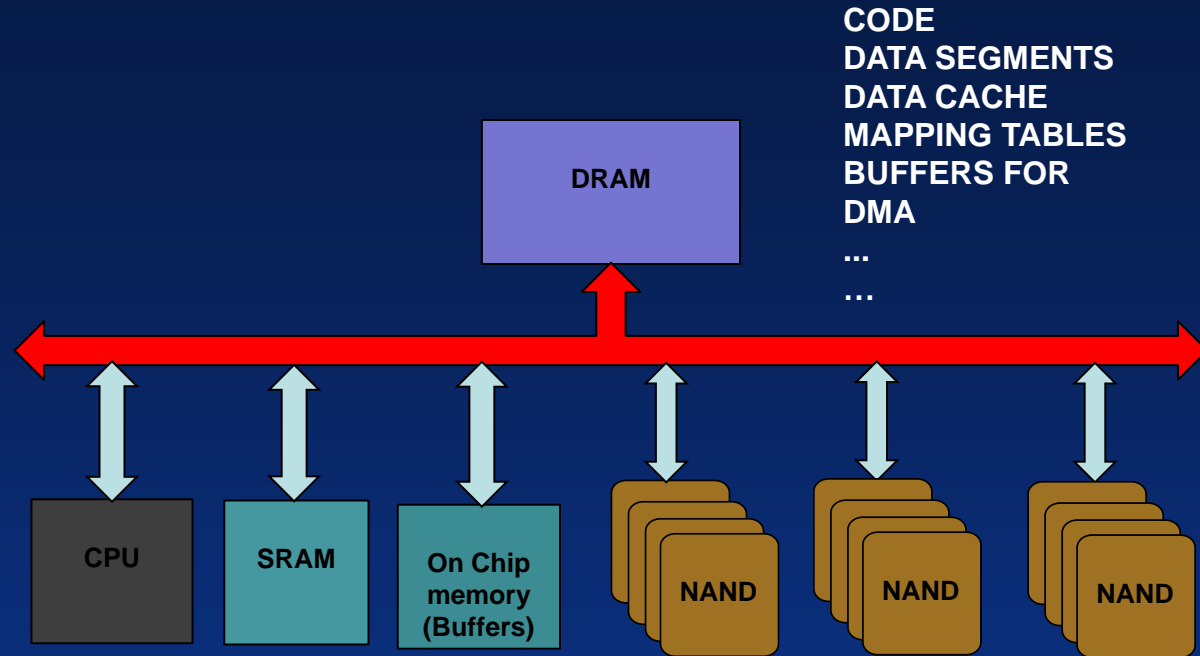**Density (small FF)**

Reliability
Endurance
Performance

How to Make a competitive TLC SSD for cost-sensitive mainstream market?

Bridging the Performance Gap with MLC SSDs

Optimal use of DRAM

CODE
DATA SEGMENTS
DATA CACHE
MAPPING TABLES
BUFFERS FOR
DMA
...
...

DRAM

DRAM access can become the **bottleneck.**

CPU **SRAM** **On Chip memory (Buffers)** **NAND** **NAND** **NAND**

# What can be done?

Control structures
- **Align to Cache boundary (Cached access)**

Data Cache
- **Cache implementation for Quick lookup**
  - **Algorithm to determine optimal caching benefit**
  - **Sequential read stream - Read look ahead**
- **Sequential Write stream - Bypass cache**

NAND Parallelism for optimal performance

- **Multiple Parallel Flash Channels enough to saturate Front End Interface bandwidth.**

- **Map host sector range for optimal use of multiple flash devices**
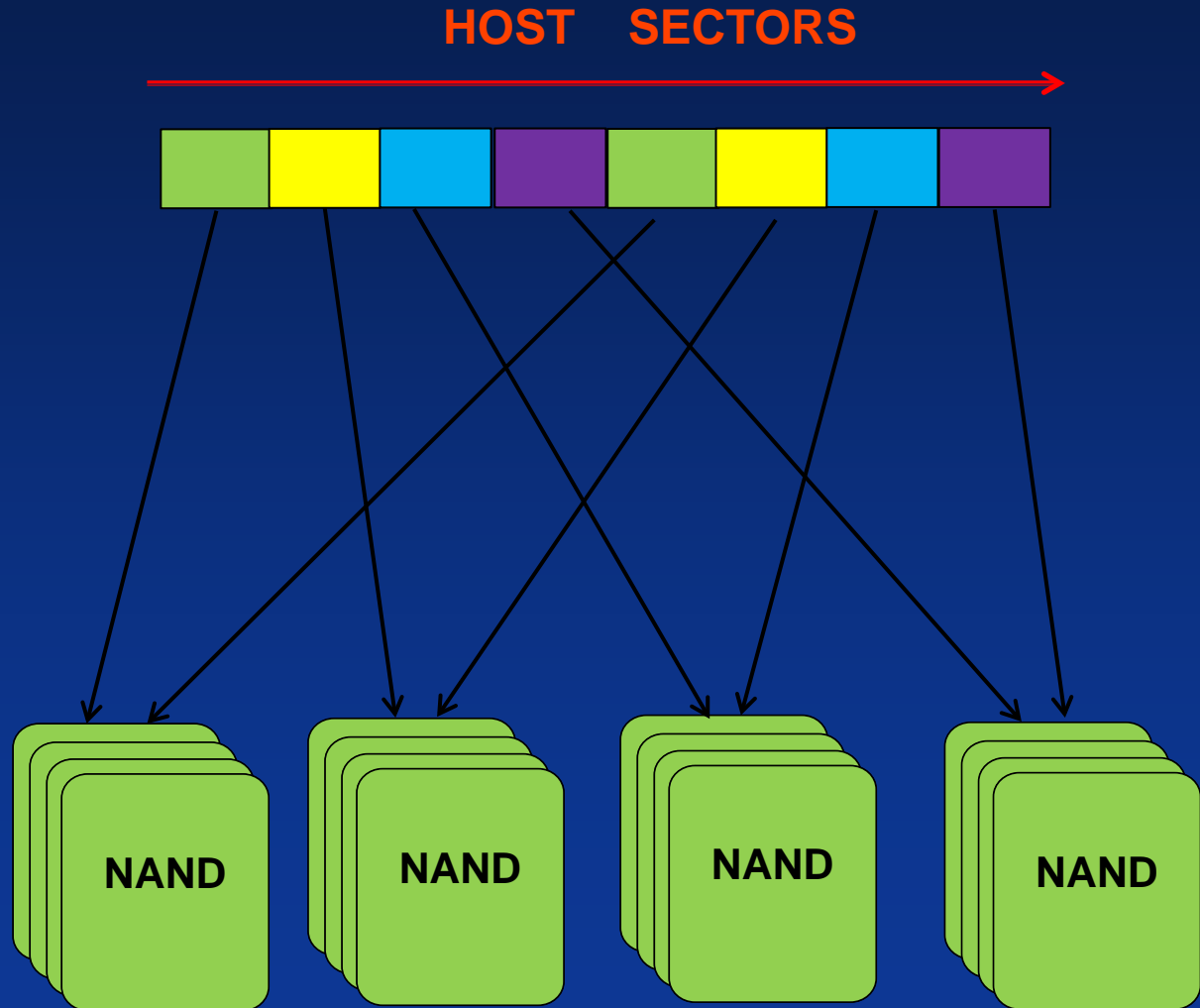
Use part of TLC Blocks as SLC
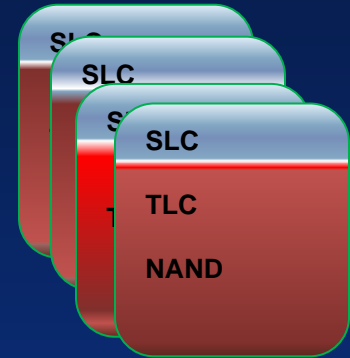
Comparison Metrics	TLC 1ynm 128Gb *	
	SLC mode	TLC mode
Read (page)	50 us	80 us (Lower Page)
		105us (Middle Page)
		80 us (Upper Page)
Program (page)	350 us	550 us (First Cycle)
		1700 us (Second cycle)
		4650 us (Third Cycle)
Erase (block)	10 ms	10 ms

*   **SanDisk 1Ynm 128 Gb eX3 datasheet**

- **SLC block size is 1/3 of TLC**
- **Reduced Capacity**

*. Faster access time of SLC
*. Higher Program / Erase cycles

Tiered Storage Approach

SLC: control structures, data cache,
TLC : Bulk Storage
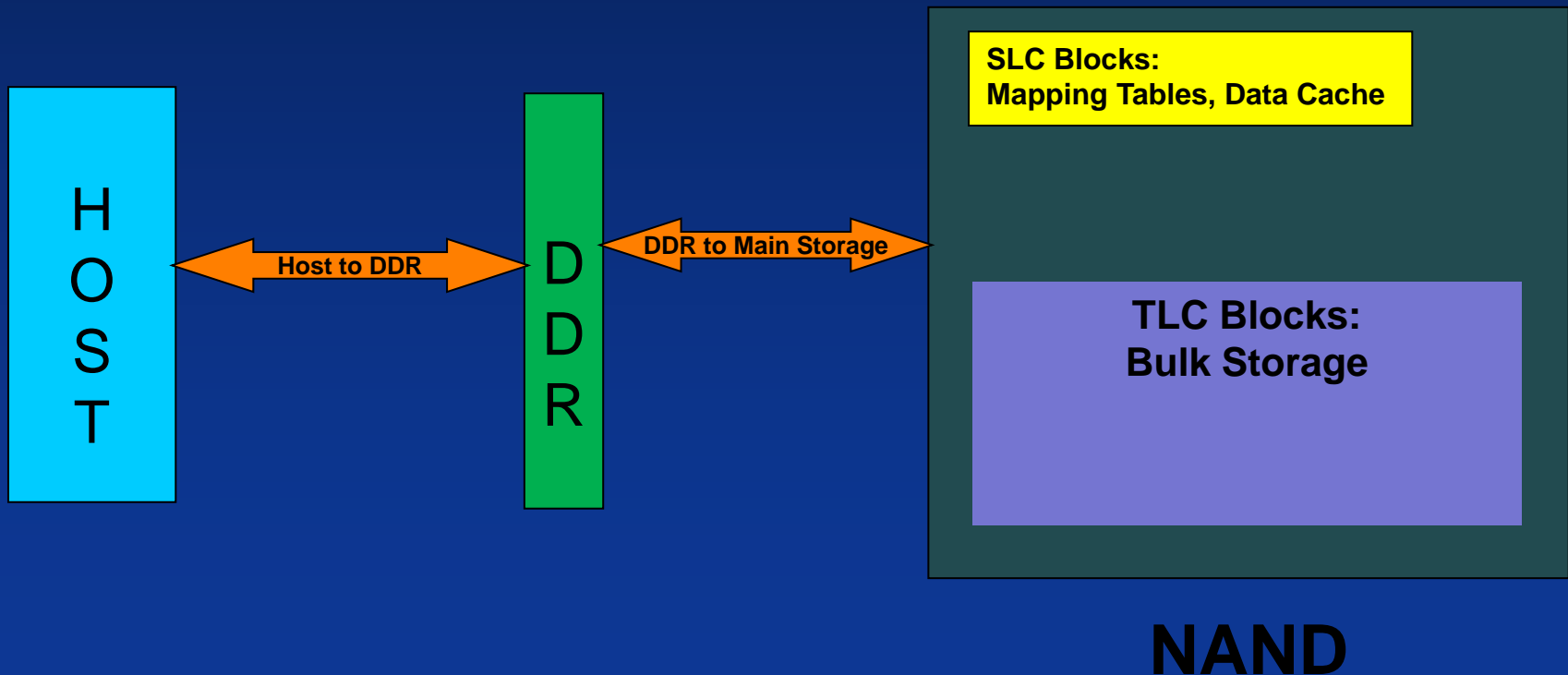
The SLC advantage

Mapping Tables in SLC
- **Speeds up drive boot and shutdown time**
- **Shorter wake up time from Dev Sleep**
- **Faster mapping table updates**
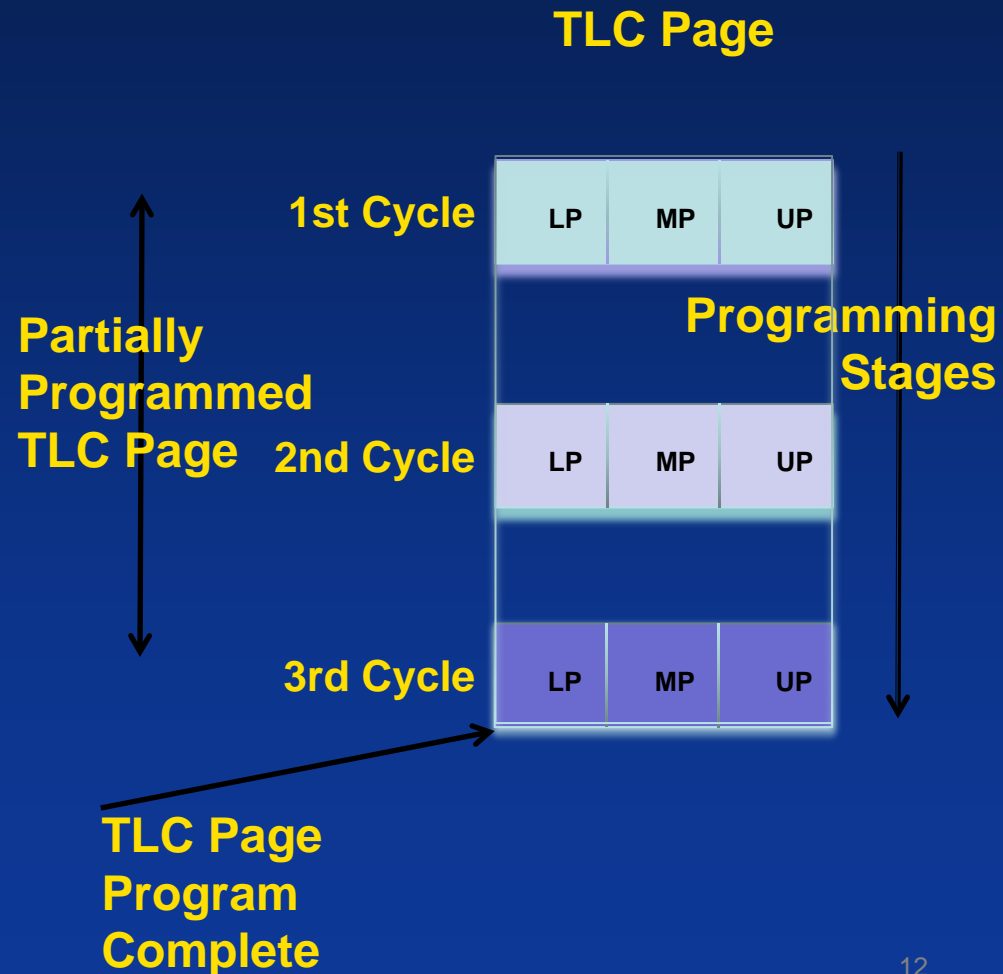- **More table updates possible during drive's life**

SLC as Data Cache
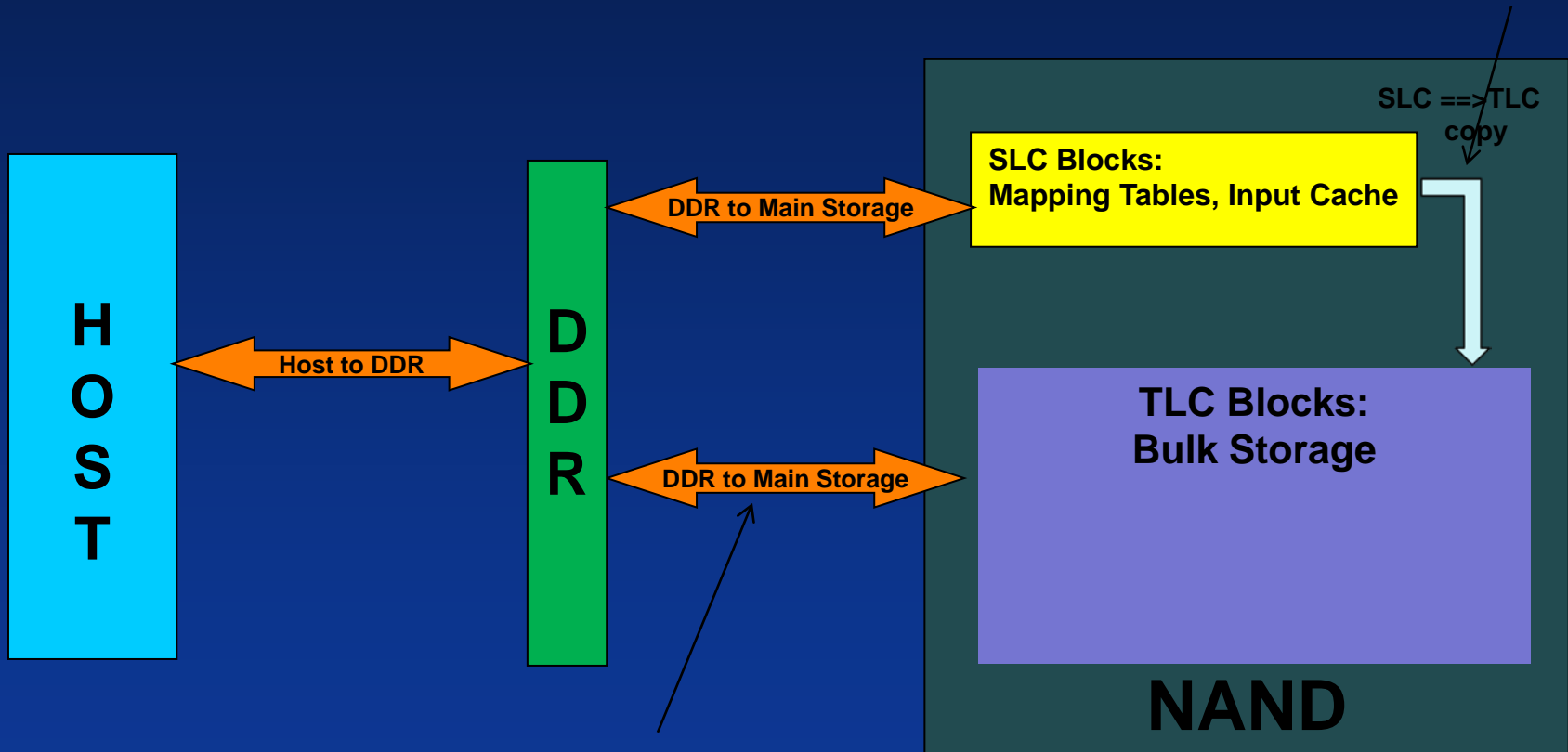- **Fast completion of most host IOs**

Writes to TLC Blocks

TLC writes

- **Multiple steps in TLC page programming**

- **Expensive (slow) operations**

TLC Page

	1st Cycle	LP	MP	UP
	2nd Cycle	LP	MP	UP
	3rd Cycle	LP	MP	UP

Partially Programmed TLC Page

Programming Stages

TLC Page Program Complete

Writes to TLC Blocks: Options

TLC Writes Via SLC

HOST

DDR

Host to DDR

DDR to Main Storage

SLC ==>TLC copy

SLC Blocks:
Mapping Tables, Input Cache

DDR to Main Storage

TLC Blocks:
Bulk Storage

NAND

Direct TLC Writes

Direct host data write to TLC blocks

Host data is directly programed to TLC blocks from DDR buffer

- **No intermediate writes**
- **Lower Write Amplification**
- **Higher sustained sequential write performance**

- **TLC program sequence requires buffering multiple pages.**
  - **More DRAM requirement for buffers**
- **Some pages are not readable during programming**
- **Higher Flush Command response time**
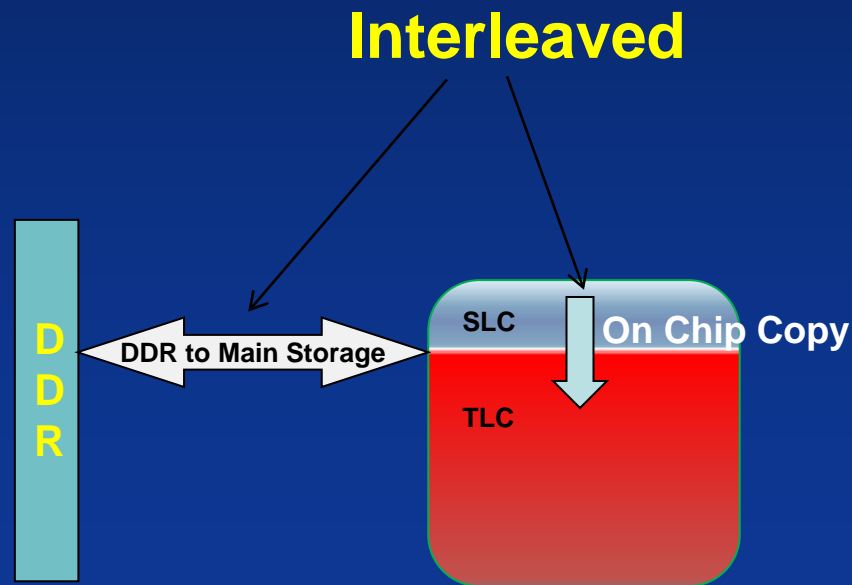- **System Complexity**

TLC writes via SLC

2 Stages

- Write host data first to SLC
- Copy data from SLC to TLC

- **High Burst write performance**
- **TLC writes are mostly background activity.**
- **No additional DDR requirement**
- **No penalty for read operations**

- **Lower sustained Sequential write performance**
- **Higher WA as data is rewritten**
- **Possible Silent error build up during Copy**

Further performance improvement techniques

- Plane interleaving using multi-plane operations

- Interleave NAND bus interface and internal NAND operations during On-Chip-Copy

- Cached access to SLC & TLC

Interleaved

DDR

DDR to Main Storage

SLC

On Chip Copy

TLC

Knobs to fine tune cost vs. performance

SLC

TLC

Adjustable SLC / TLC ratio

Larger SLC block pool

- **Keep most of the host program traffic operations satisfied from SLC pool**

- **TLC writes occur mostly during background activity.**

Capacity Loss

TLC block overprovisioning

- **Reduced need to free (erase) blocks**
- **More NAND bandwidth for host traffic**

Capacity Loss

SATA 6Gb/s MLC and TLC SDD performance comparison*

CrystalDiskMark on Win7 platform

Secondary drive

| Parameter	Unit	Queue Depth	480 / 512 GB MLC SSD **	480 / 512 GB TLC SSD***
Sequential Read	MB/s	32	520	At Par
Sequential Write	MB/s	32	460	At Par
Random Read[4KB]	IOPS	1	8,500	At Par
		32	96,000	At Par
Random Write[4KB]	IOPS	1	19,000	At Par
		32	80,000	At Par
Read / Write Latency	Us	1	55/65	At Par
OFF to ON Resume Time	Ms	N/A	690	At Par
PCMark (Secondary)	IOPS		75K	At Par

* SanDisk Internal Test
** SanDisk X300s
*** Sample TLC SSD

Conclusion

Mainstream SSD market is cost-sensitive. It demands storage capacity, reliability and performance at lower price.

TLC SSD meets the middle ground on metrics for mainstream client SSD and price sensitive segments of enterprise (hyper scale) storage markets.
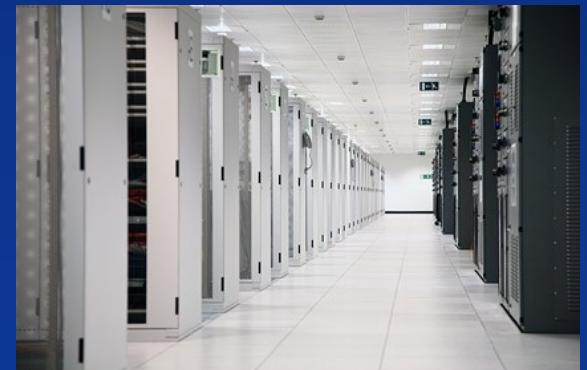
Thank You!

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