

# High Density SSD Structure with RAID

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## Concept

- RAID is originally redundant array of inexpensive disks
- Now commonly redundant array of independent disks) is a data <u>storage virtualization</u> technology that combines multiple <u>disk drive</u> to a logical unit
- For the purposes of data redundancy or performance improvement

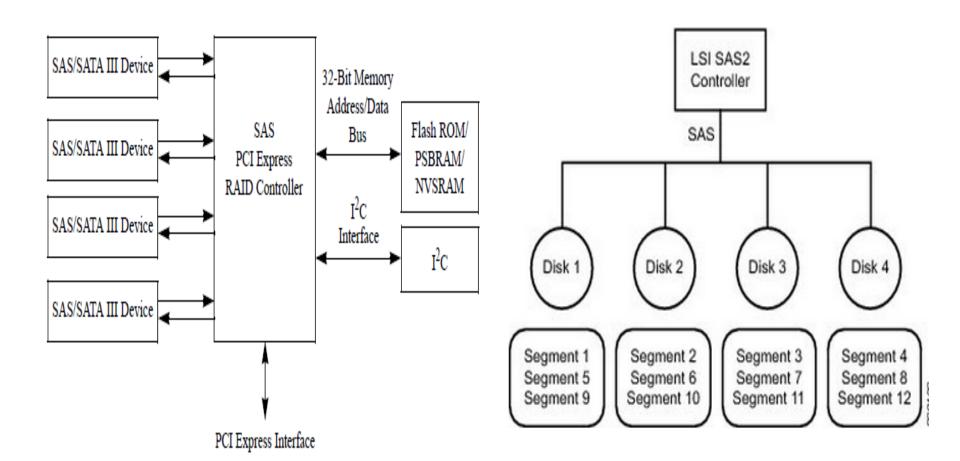


#### Benefit

- Emphasis on inexpensive but reliable then disks RAID
  - Back to original concept
- Shield from flash vendor secret backdoor
  - No worry of undocumented scramble techniques
  - Isolate from LDPC/BCH ecc etc
- Time to the market
  - In sync with flash vendor's technologies
  - Ever need early involvement



## **HD RAID**





## Flash vs HD

Characteristic	ISK HDD	NAND Flash	Improvement
Performance	250 IOps	30,000 IOps	86X greater
Latency	10 ms	0.3 ms	30X faster
Reliability (MTBF)	I.2 M Hours	2.0 M Hours	67% greater
RAID Rebuild Times	10-20 Hours	0.3-0.5 Hours	40X faster
Power (Watts per TB)	30	5	83% lower
Efficiency (I/O per watt)	15K HDD	6,500	433X higher

•But Flash need to deal with wearing and ECC, HD does not as eMMC



# eMMC + Striping

- Sandisk eMMC 4.51
  - ■Interface HS200 ( 200 MB/sec)
  - Sustain read/write (150/45MB/s)
  - •4KB random read/write(4k/800 IOPS)
- Samsung Ultra Fast eMMC 5.0
  - ■Interface HS400 (400 MB/sec)
  - Sustain read/write (250/90MB/s)
  - •4KB(?) random read/write(7k/7K IOPS)
- •Use striping (RAID 0) to boost the performance



## RAS

- Reliability
  - Single device wear leveling is solved by eMMC
  - Global wear leveling is done by cluster ASIC
  - SMART alike will be achieved by vendor command
  - •RAID 10, 50, 60 can be easily implement
- Availability
  - eMMC is a JEDEC standard like SDDR
- Serviceability
  - Modula design with current MMC housing



## Challenge

- Electronic challenge
  - Power interrupt reliability
  - No control of Flash type of the shelf
    - ■Today's eMMC are generally used MLC(3K), SLC (100K) or eMLC(30K) are rarely to find
  - SMART like command is not a standard for eMMC
- Mechanical challenge
  - •Hot wrap mechanism reliability
  - As speed increase, MMC housing is not the best solution, vibration is also an issue



#### **ASIC Schedule**

- •SATA version of eMMC bridges are available
- •PCIe FPGA Proto type done As July 1st, 2014
- •First version ASIC with be single line PCIe 2.0 RAID 0, 1, 5
- •First Silicon 4Q14