Memory Subsystems for IoT

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Spansion

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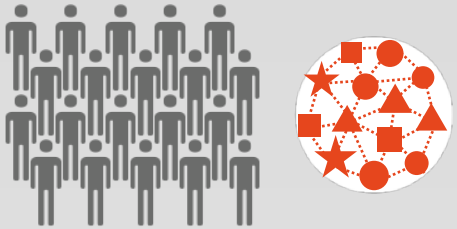
Explosion of More Intelligent and Connected Devices

2003

6.3B people

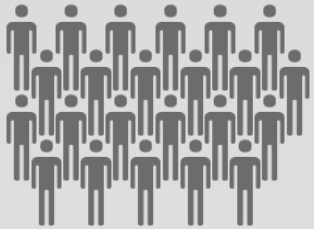
Devices starting to connect to the internet



2008

6.7B people

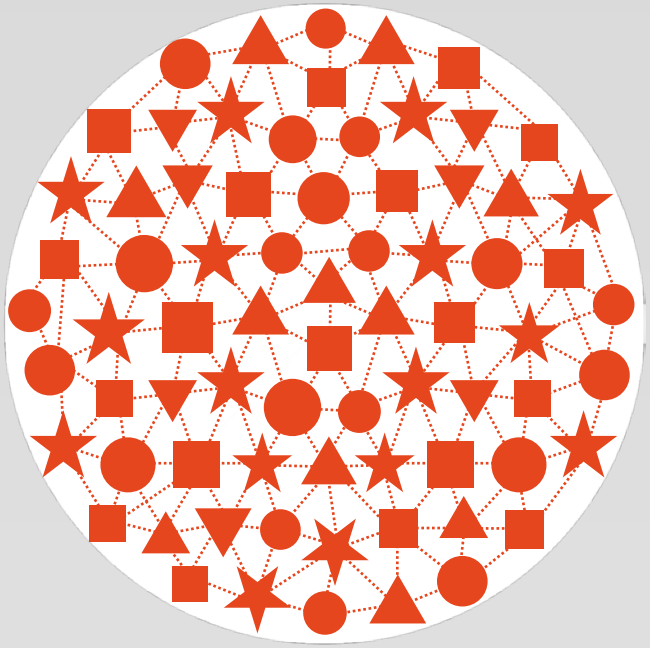
More connected devices than people on earth



2020

7.7B people

50 – 70 billion connected devices; ~7x the number of people on earth



Connected devices

World population

Interconnected Systems in the Connected World

SPANSION

Smartphones | STB | DTV | Smartwatch Wearable | Portable scanner POS | Portable medical meters

Home Entertainment
- 4G
- Appliances
- Smart Meter
- Energy Management

Traffic Flow Optimization
- SDL
- GPS
- Traffic Cameras and Lights
- Connected Ambulances
- Digital Signage
- Parking Meter
- Connected Car
- Automated Car System

Horizontal Optimization
- Security
- Switch
- Inverter
- Medical Devices
- Responsive Store
- Municipal Command & Control Center

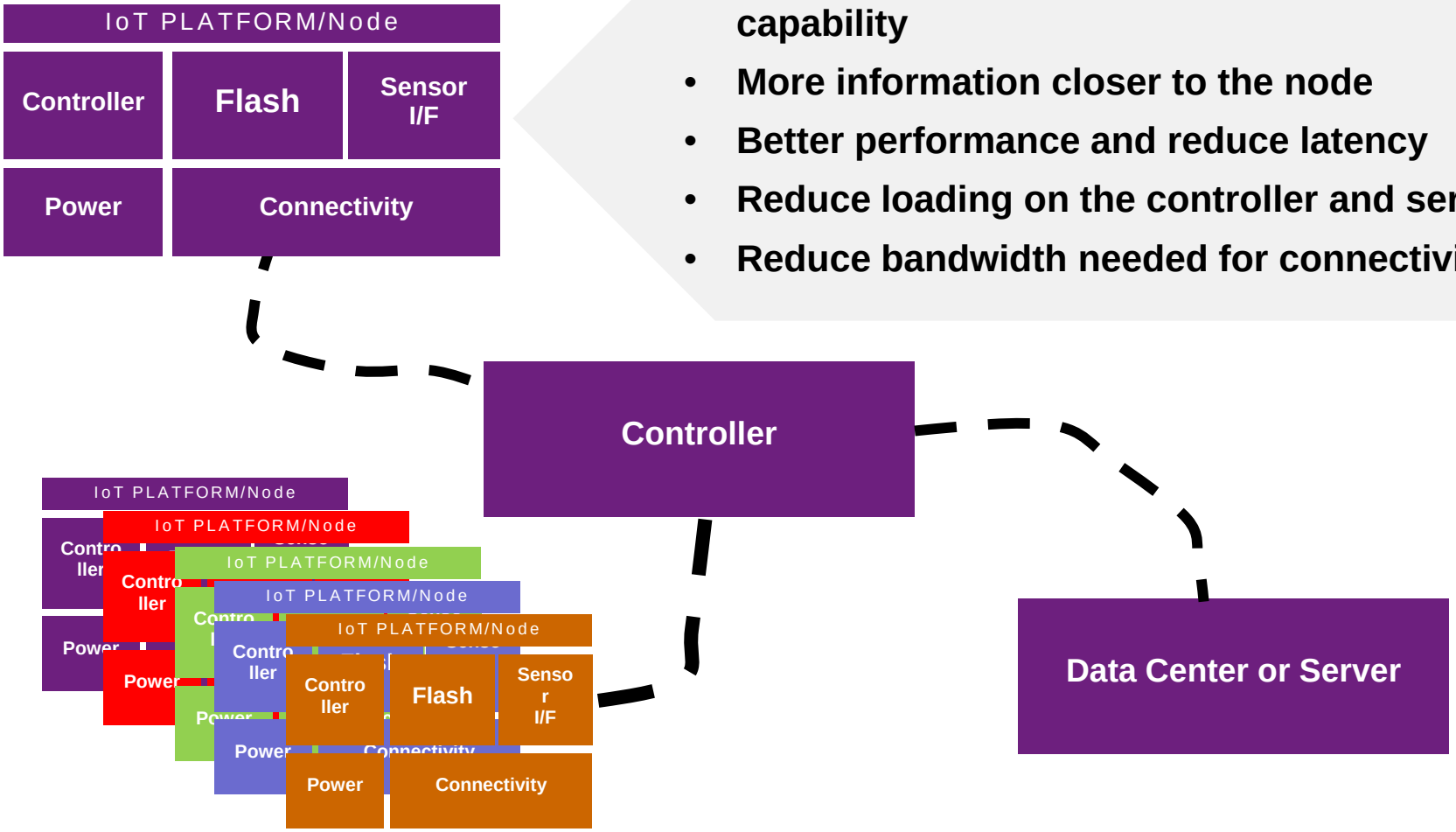
Factory Optimization
- FA
- Test control
- Logistics Optimization

Communication Network Optimization
- HVAC
- Inverter
- Smart Grid

Memory | **Sensors** | **Automation** | **Managed Power** | **Connectivity** | **Security**

Powerful Nodes → Faster Controller → Faster Flash

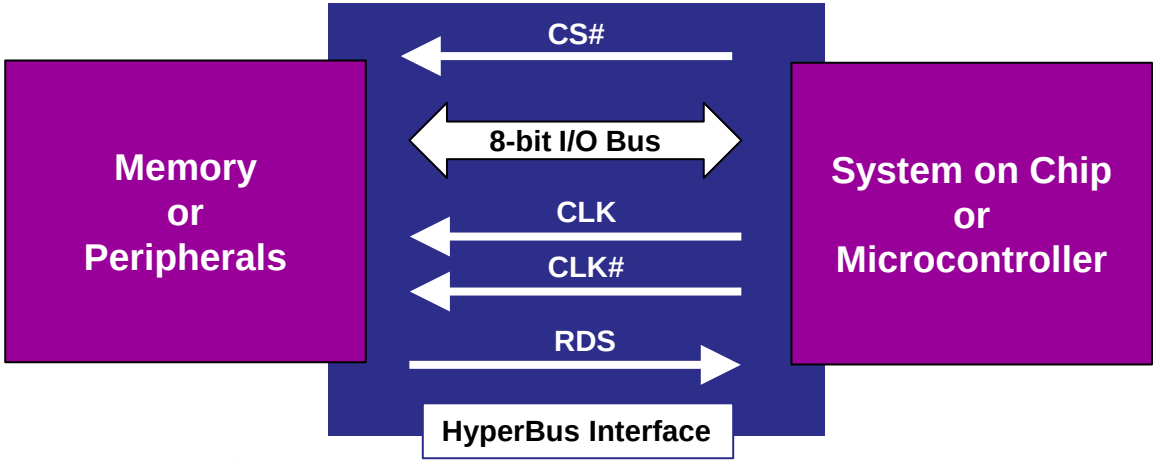
- IoT nodes getting smarter, more processing capability
- More information closer to the node
- Better performance and reduce latency
- Reduce loading on the controller and server
- Reduce bandwidth needed for connectivity



Spansion HyperBus™ Interface and HyperFlash™ Memory

Spansion® HyperBus™ Interface

- 12 pin interface
- Dramatically improves read performance while reducing pin-count and board space
- Reuse of existing SPI pins
- Applicable to flash, RAM and peripheral devices



Compelling Features:

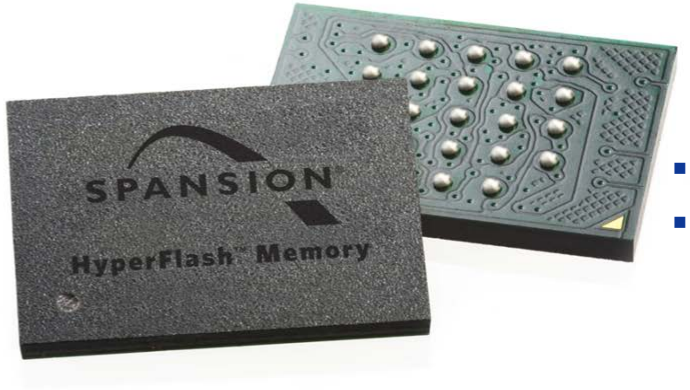
- 5x the Read Speed of Quad SPI
  - 333MB/sec VCC = 1.8V
  - 200MB/sec VCC = 3.0V
- 96ns Initial Read Access Time
- 128, 256, 512 Mb densities

Automotive Temperature

- Supports Extended Temp Range
  - -40°C to 125°C

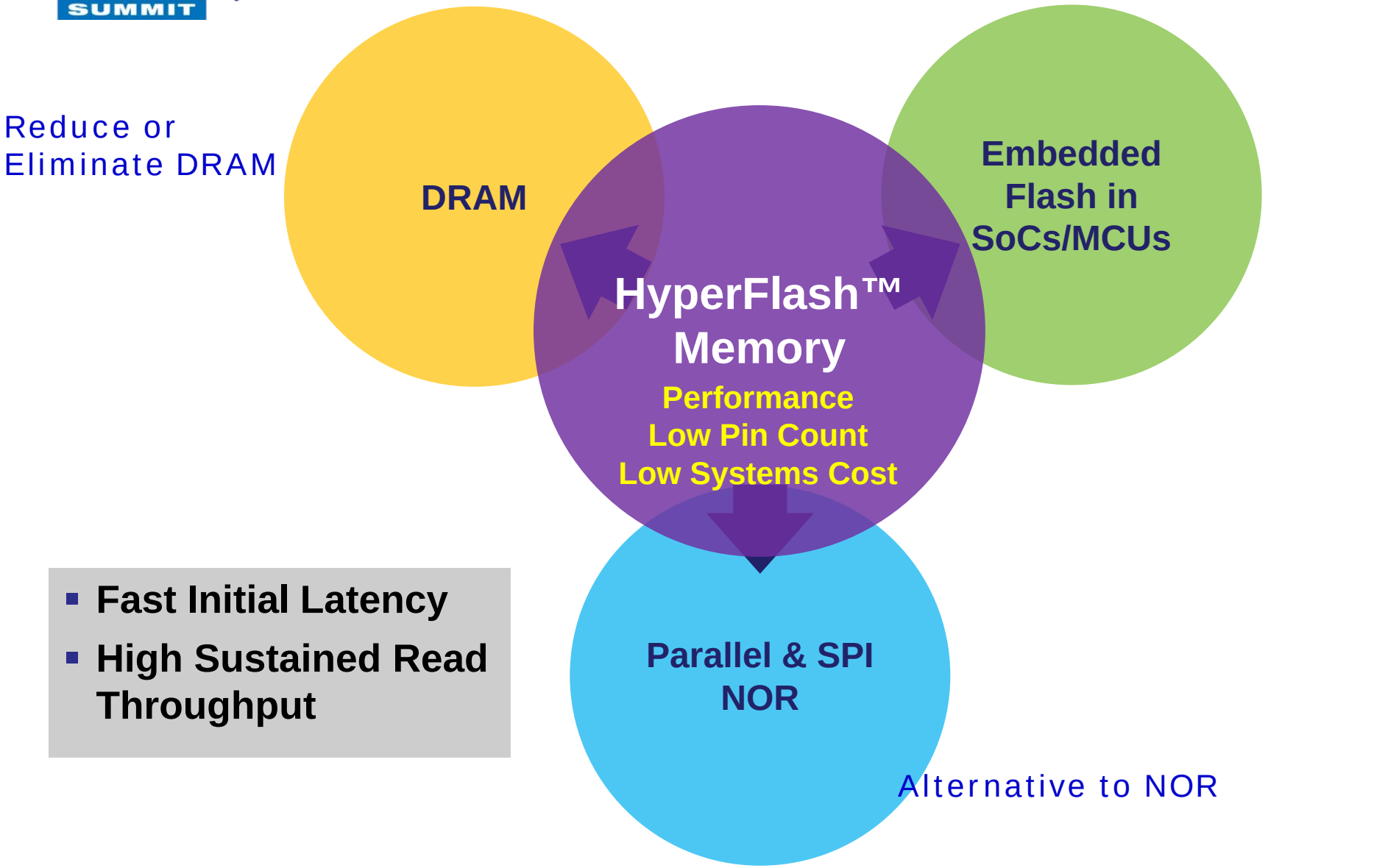
Space-Saving 8x6mm BGA

- Common 24-ball BGA footprint
- SPI, QSPI, Dual QSPI or HyperFlash Memory



- **Chip Select (CS#)**
- **8-bit up to 166MHz Double-Data-Rate (DDR) I/O bus for high throughput**
- **Differential Clock (CLK & CLK#)**
- **Read Data Strobe (RDS) for accurate read data capture by host**

HyperFlash™ Memory Usage



- **Fast Initial Latency**
- **High Sustained Read Throughput**