RRAM in IoT

Cliff Zitlaw
Product Architect
Crossbar Inc.

IoT In the Next Few Years

Internet Connection Demands Increasing

3B PCs, tablets and smartphones today

IoT nodes increasing from:

9B in 2013 ▶ **28B** by 2020

Computation Increasingly Moving to Nodes

Technology Drivers Supporting Node Deployment

- Sensors becoming increasingly affordable
- Smartphones as a gateway for IoT nodes to the internet
- Bandwidth cost dropped by 40x in the last 10 years
- Processing costs dropped 60x in the last 10 years

RRAM as NVM Alternative in IoT

Data Center – Block Oriented Data Storage

- Low latency(10^{-5} s), high bandwidth, low power
- Native 3D compatible array architecture
- Alternatives: SSD, DRAM (disk cache), hard disk

Nodes – XiP Code and Random Access Data

- Low latency (10^{-8} s), high bandwidth, low power
- CMOS BEOL compatible
- Alternatives: embedded NOR, discrete NOR

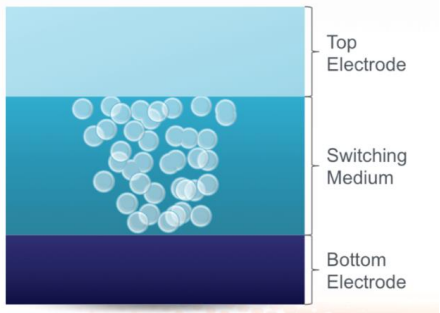
Existing NV Memory Technology Comparison

Feature	Embedded NOR	NAND	RRAM	
			Embedded 1T1R	1TnR
Non-Volatility	Yes	Yes	Yes	
Random Read Time	40ns	50us	20ns	1us
Program Time	268us/128B	>1000us /8KB (MLC)	12us/4B	64us/8KB
Erase Time/Size	168ms/16KB	>2ms(Block)	**Erase Not Required EEPROM Emulation!**	
Endurance	10^5	MLC 10^3	10^8 - 10^{12}	
Cell Size	0.1um^2@40nm	SLC 5F^2 MLC	0.1um^2@40nm	SLC 4F^2, Stacking, MLC
Cost	Med	Low	Low	Very Low

Crossbar's RRAM-based Technology

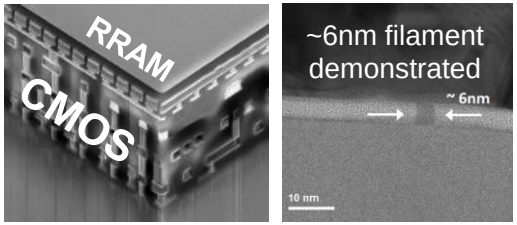
Simple, 3 layer Approach

- Metallic top electrode
- Resistive switching medium
- Non-metallic bottom electrode
- Electric field based filamentary switching



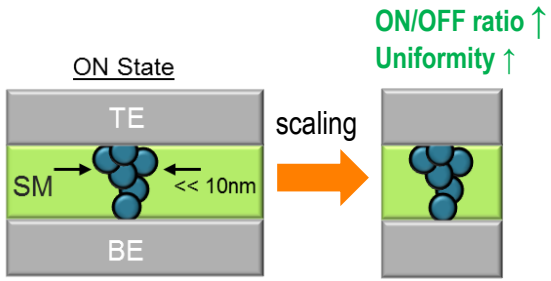
CMOS Back-End-Of-Line Compatible

- RRAM layer(s) on top of CMOS logic
- Filament sizes less than 10nm demonstrated
- On/Off ratio improves with smaller geometries



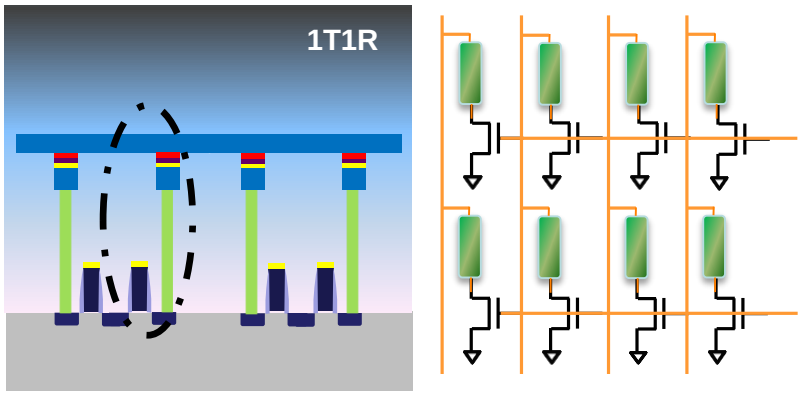
Array Architectures

- Data storage
  - Approaching $4F^2$ memory cell for data storage
  - Natively 3D stackable
- Code storage
  - Low latency



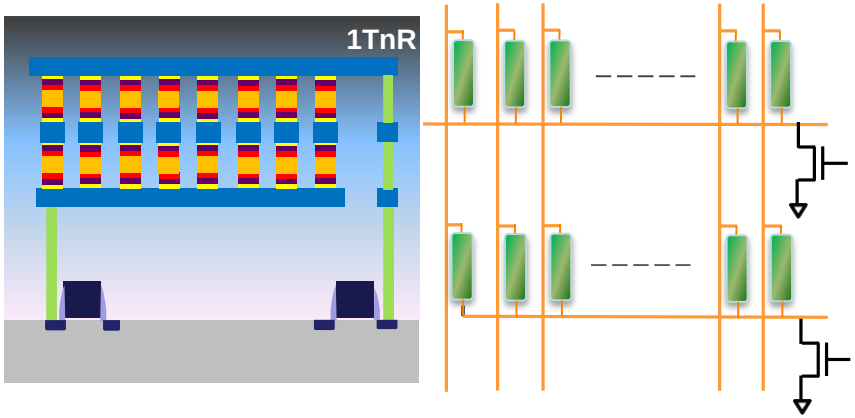
RRAM Array Architectures

1T1R with Linear RRAMs



- Cell size dominated by the select transistor
- Suited for high speed embedded memory operation or high performance discrete NOR products

1TnR with Non-Linear RRAMs



- Effective cell size $4F^2$/ (number of RRAM layers)
- Under array is utilized for peripheral circuits – provides high array efficiency
- Suited for high density high performance memory (NAND/SCM memory)

Crossbar Development Schedule

1T1R Embedded NOR Macro → **1TnR Discrete Device**

- 2Mb to 64Mb densities
- Hard macro using 40um logic

Flash Memory SUMMIT

Thank You