Flash Memory SUMMIT

Emulating Rank Modulation in Flash Memories

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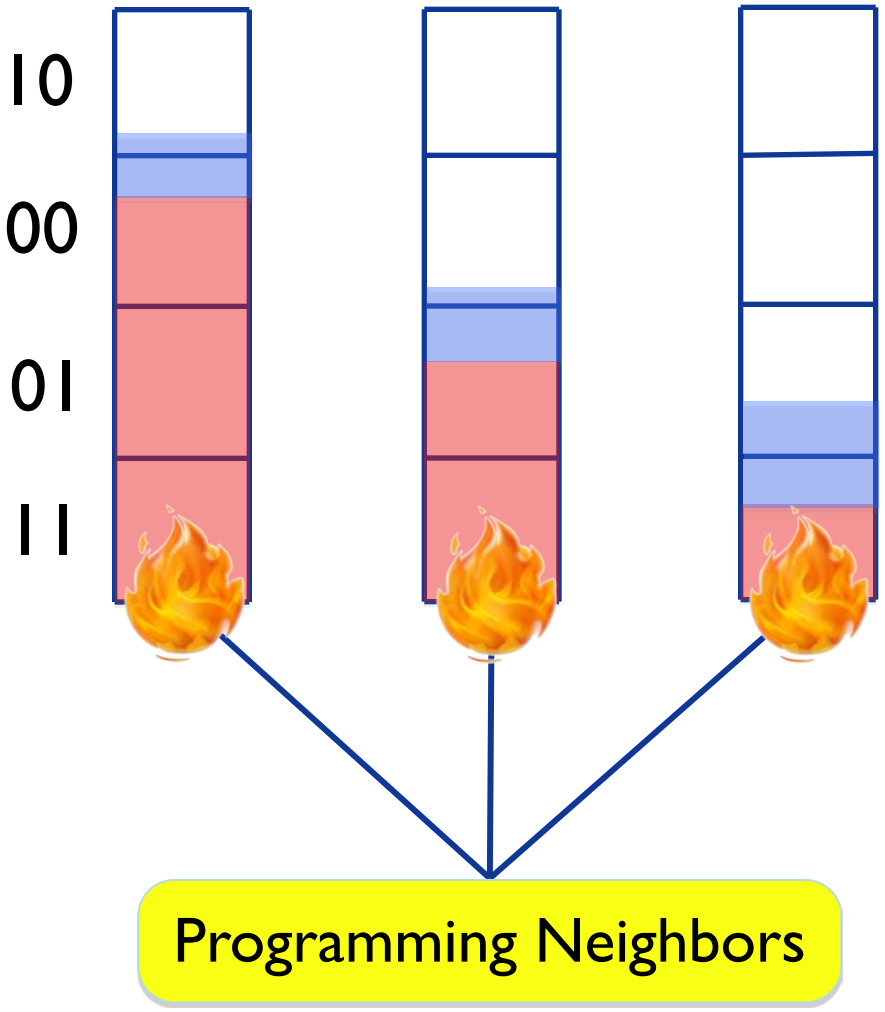
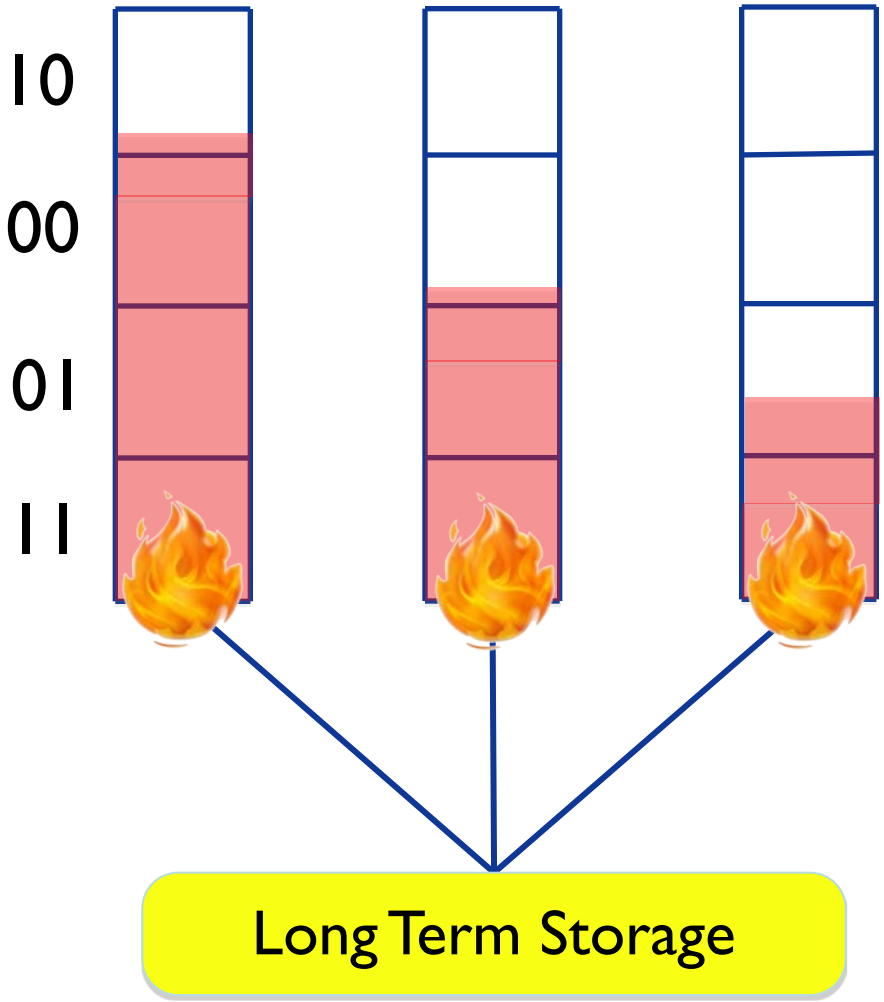
Disturbance Issue

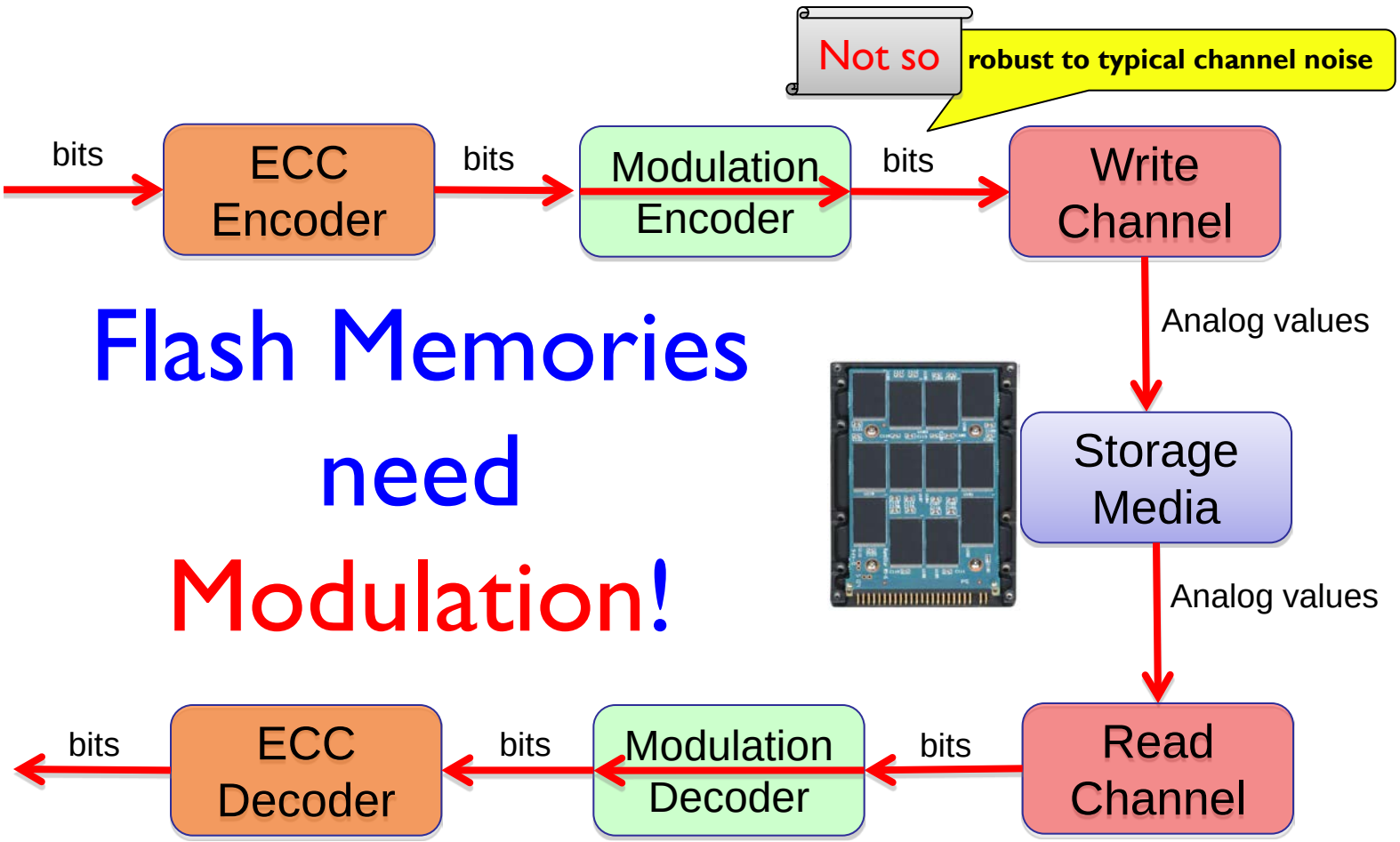


Data Retention Issue



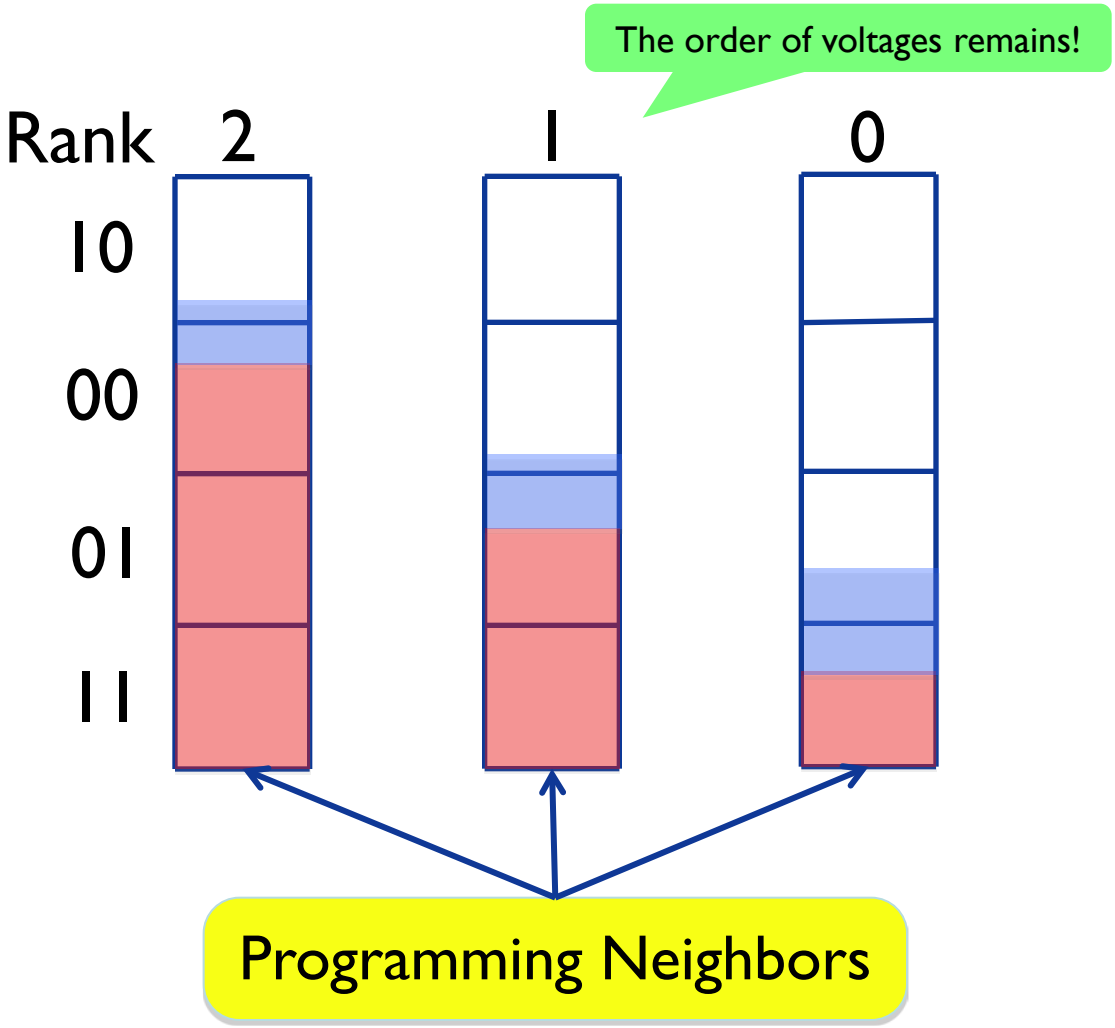
Are there
better data representations?

Magnetic Recording vs Flash



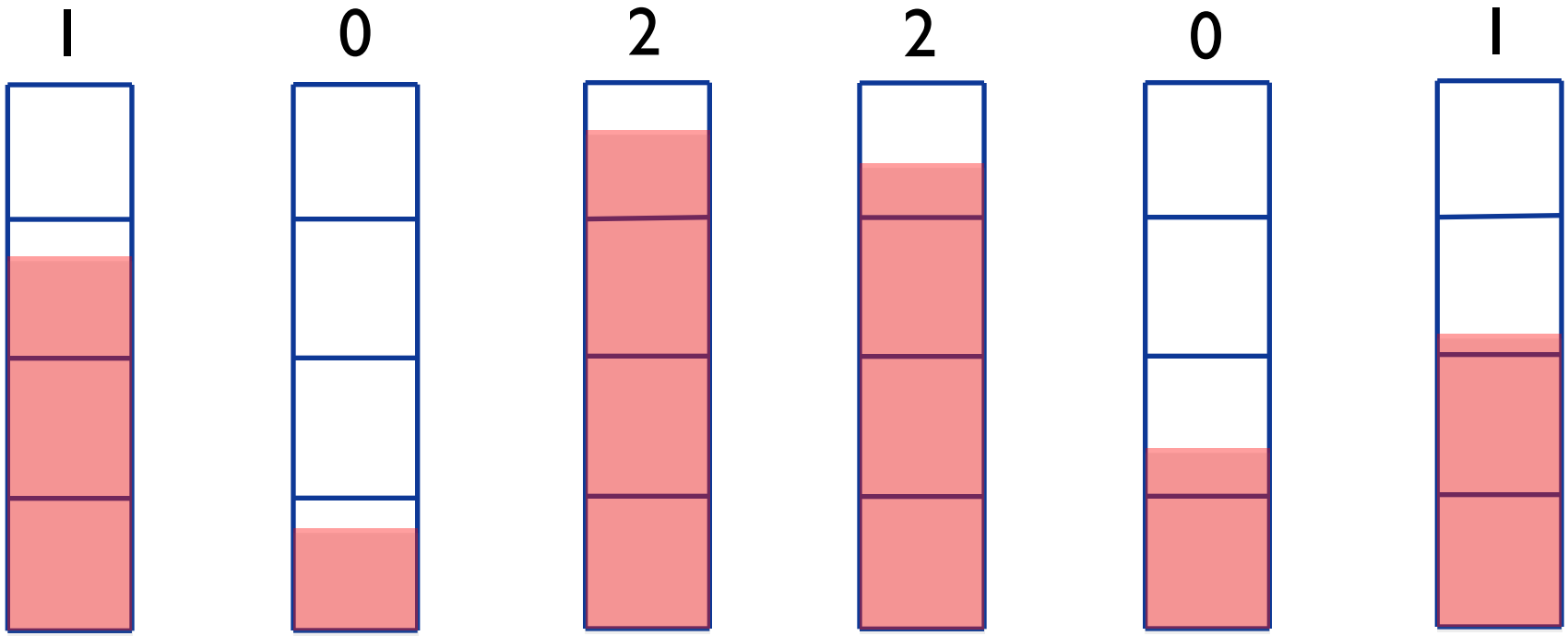
Flash Memories need Modulation!

Rank Modulation: Use Relative Order!



[2] A. Jiang, R. Mateescu, M. Schwartz, and J. Bruck, "Rank Modulation for Flash Memories," IEEE Transactions on Information Theory , vol.55, no.6, pp.2659-2673, June 2009

Put More Cells in Each Rank



Example: 3 Ranks, 2 Cells/Rank

[3] E. En Gad, A. Jiang and J. Bruck, "Trade-offs between Instantaneous and Total Capacity in Multi-Cell Flash Memories," ISIT 2012.

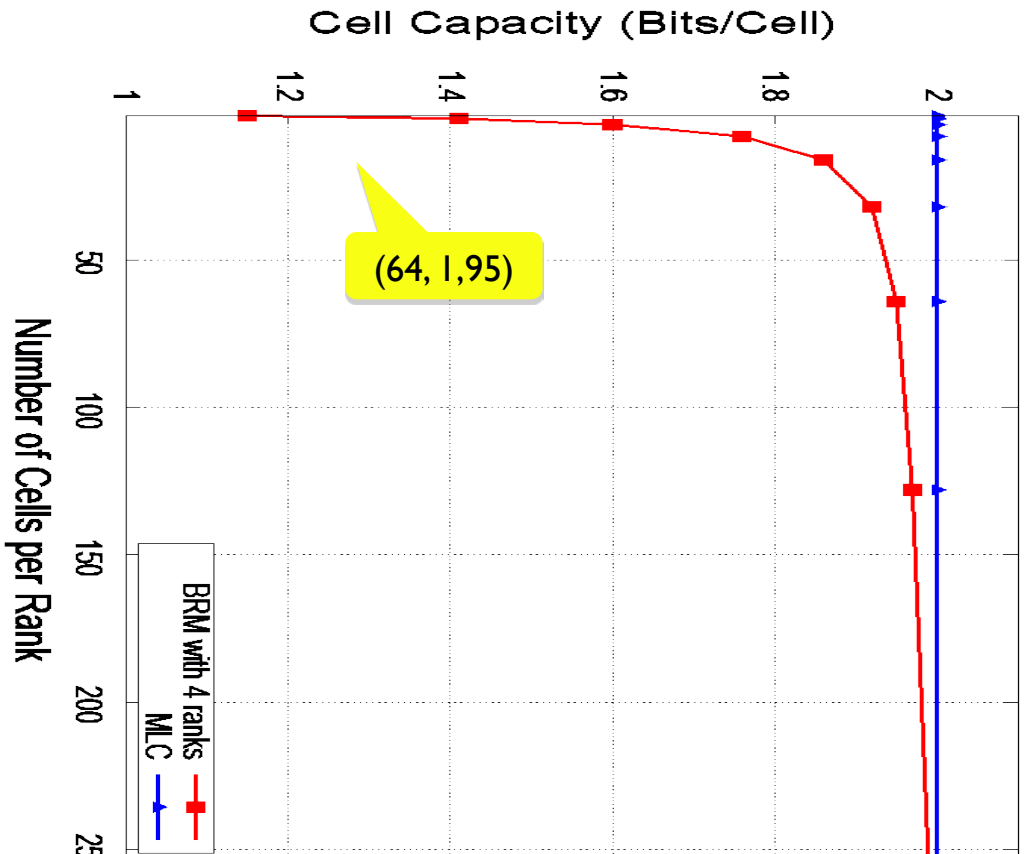
Capacity

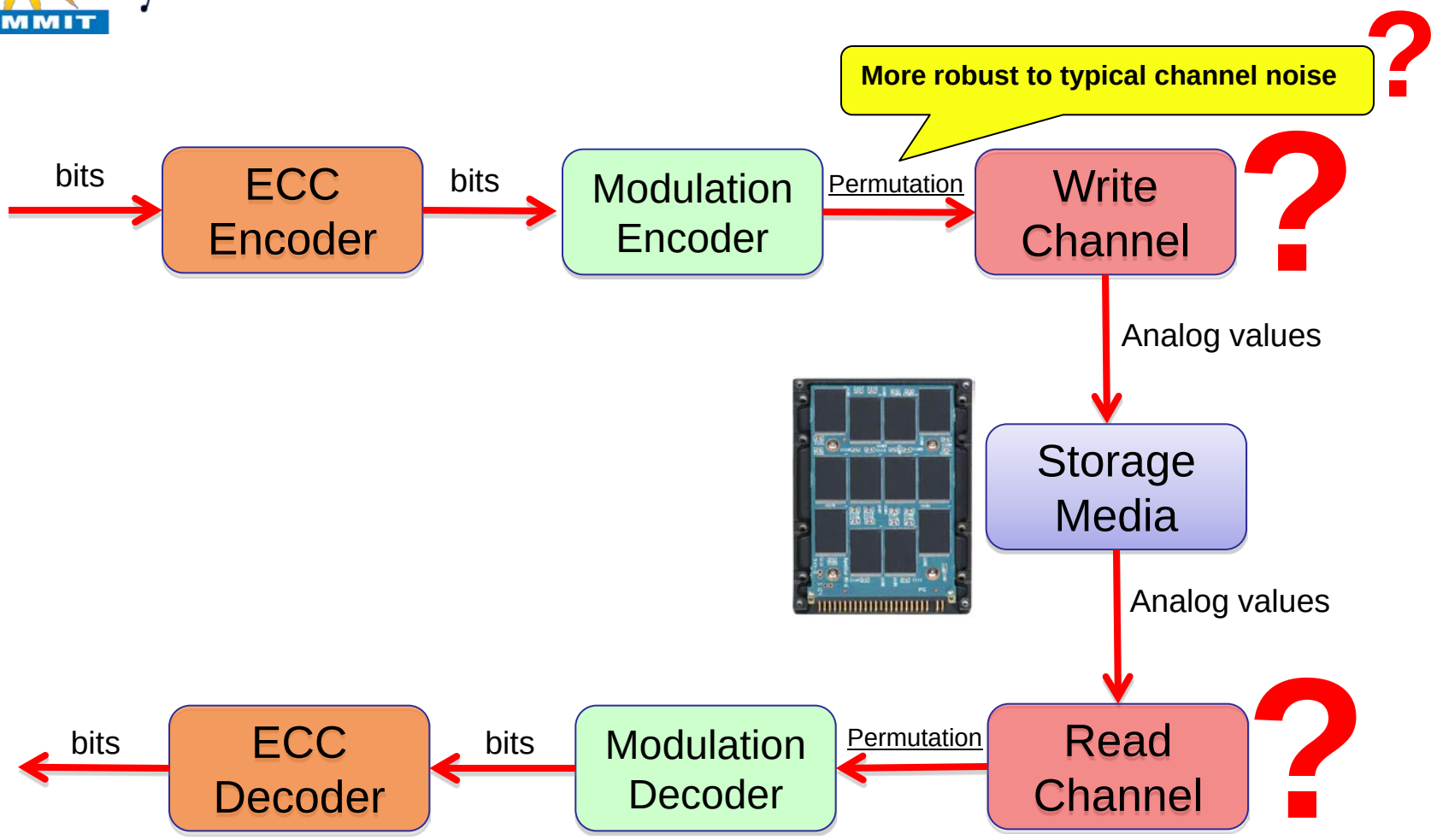
n: total number of cells

m: number of cells per rank

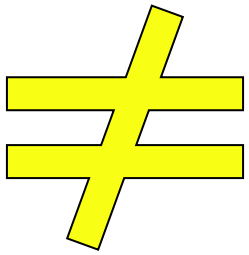
r: number of ranks, r = n / m

$$\log_2(n!/(m!)^r) / n \quad \text{(bits/cell)} \approx \log_2 r$$




More robust to typical channel noise
bits
ECC Encoder
bits
Modulation Encoder
Permutation
Write Channel
Analog values
Storage Media
Analog values
Read Channel
Permutation
Modulation Decoder
bits
ECC Decoder
bits

Doing Rank Modulation

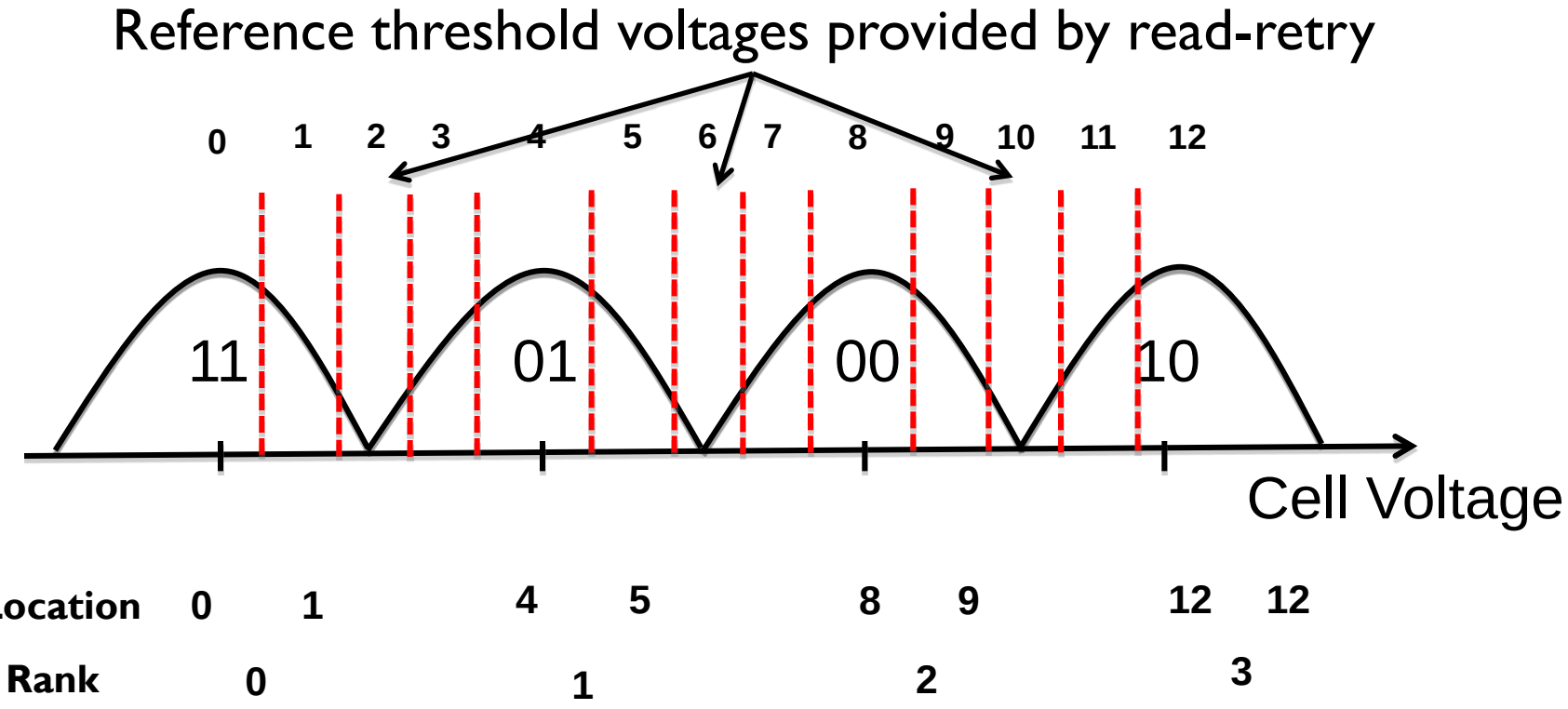


Redesigning NAND Flash

Writing and Reading for Rank Modulation

- Program via standard interfaces
  - Focus on r = 4 ranks for MLC
  - Cell with rank k is programmed to level k (k = 0, 1, 2, 3)
- Read via read-retry and sorting

Rank Modulation in MLC



Example: n = 8, rank = 4

(0, 1, 0, 3, 2, 2, 1, 3)

Experimental Configurations

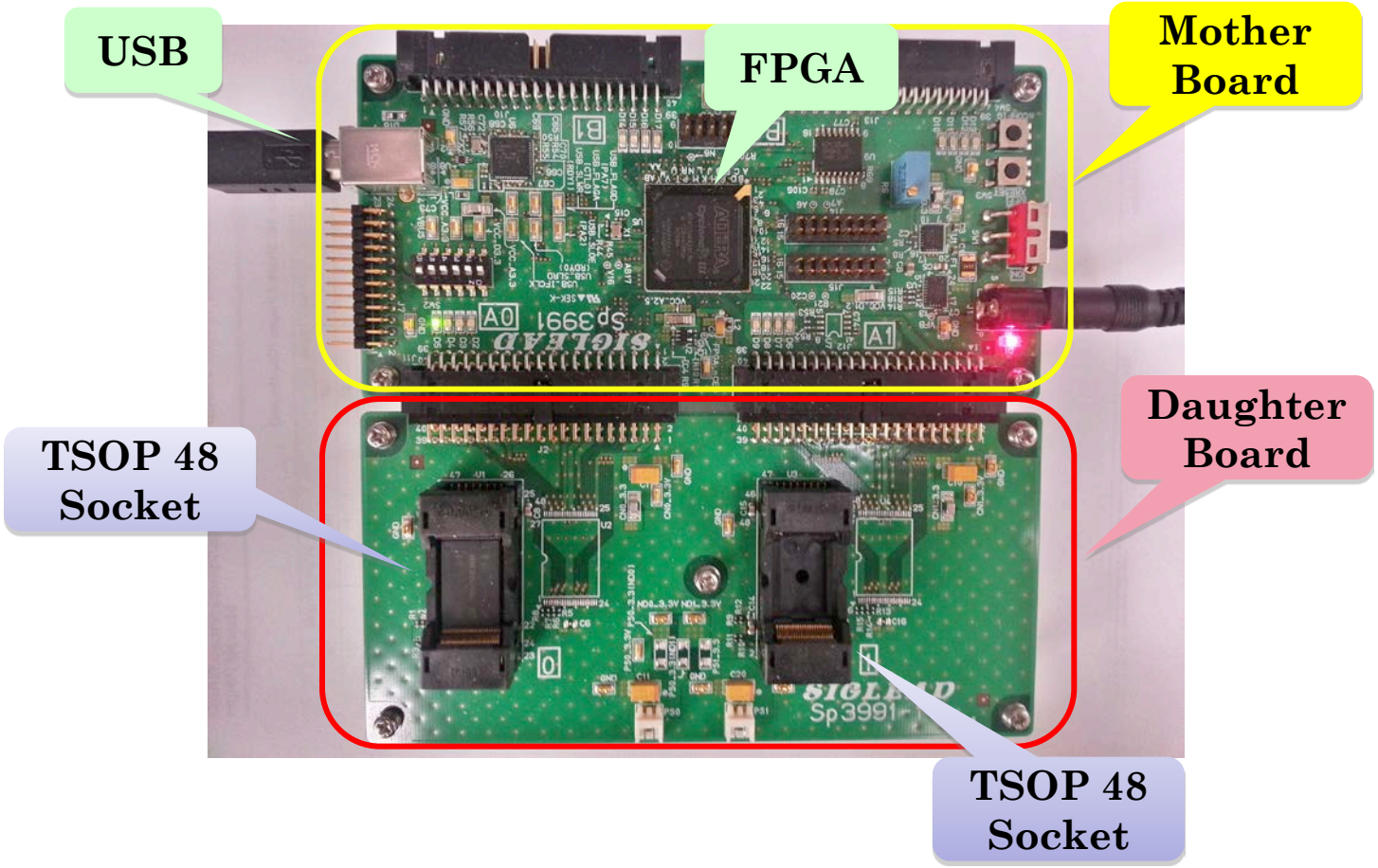
- NAND flash chip
  - Micron L84A 20nm MLC (MT29F64G08CBAB)
  - 8 read-retry modes (we use modes 0 – 3)
- MLC v.s. RM without interference
  - Cells tend to be underprogrammed
  - Only program the even page of a wordline (WL)
  - Skip the next WL after writing the current WL
- MLC v.s. RM with interference
  - Cell voltages drift to larger values
  - Sequentially program each page in a block

Comparing Cell Error Rates

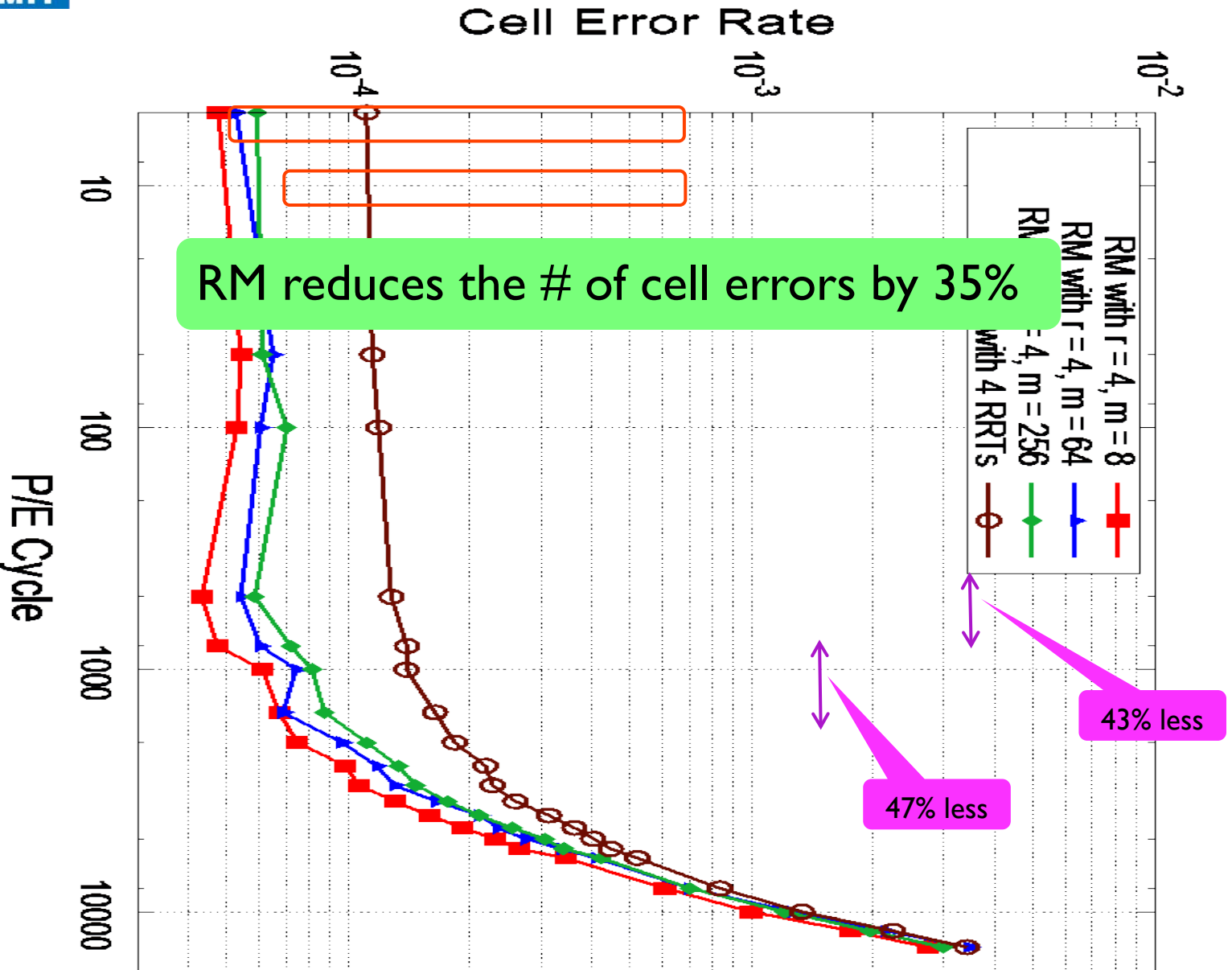
- MLC
  - A cell error happens if at least one bit of the cell is wrong
- Rank modulation
  - A cell error happens if two cells switch their ranks
  - e.g. (0, 1, 0, 3, 2, 2, 1, 3) ←→ (0, 0, 1, 3, 2, 2, 1, 3)
- Cell error rate = $\frac{\text{Number of cell errors}}{\text{Total number of cells written}}$

NAND Evaluation Platform

- SigNAS-II
  - FPGA based, produced by Siglead Inc. (Japan)

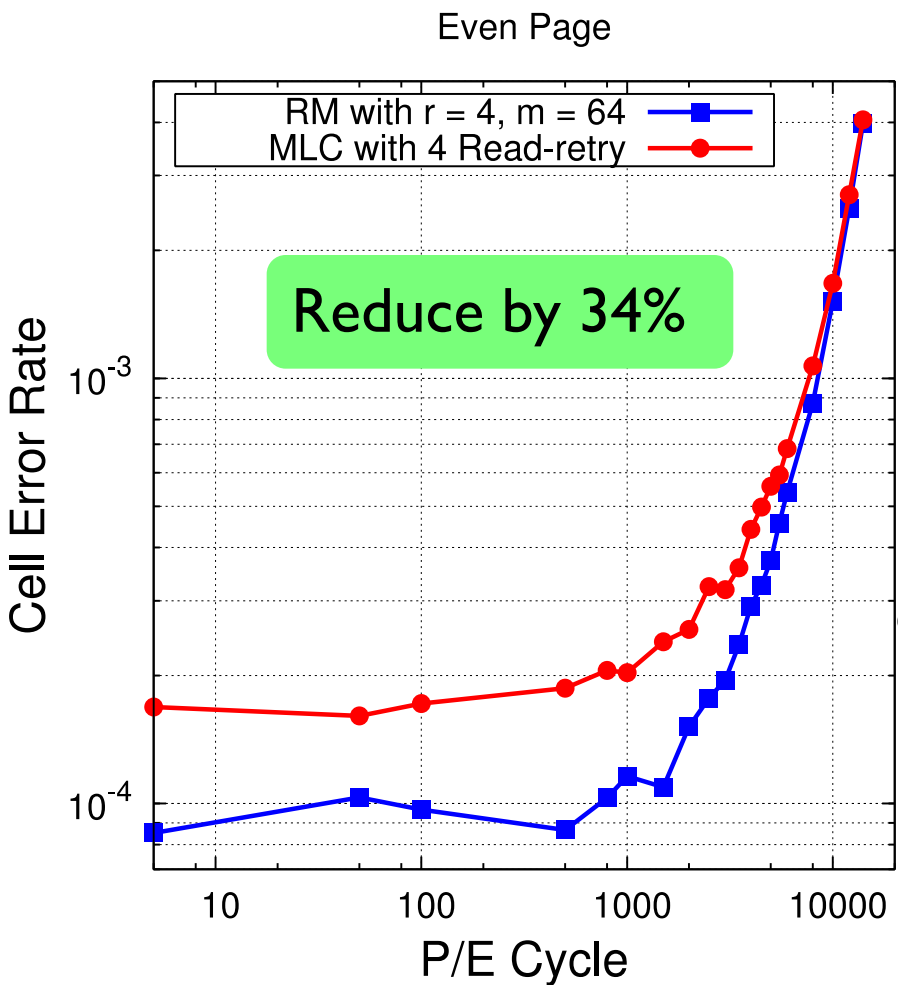


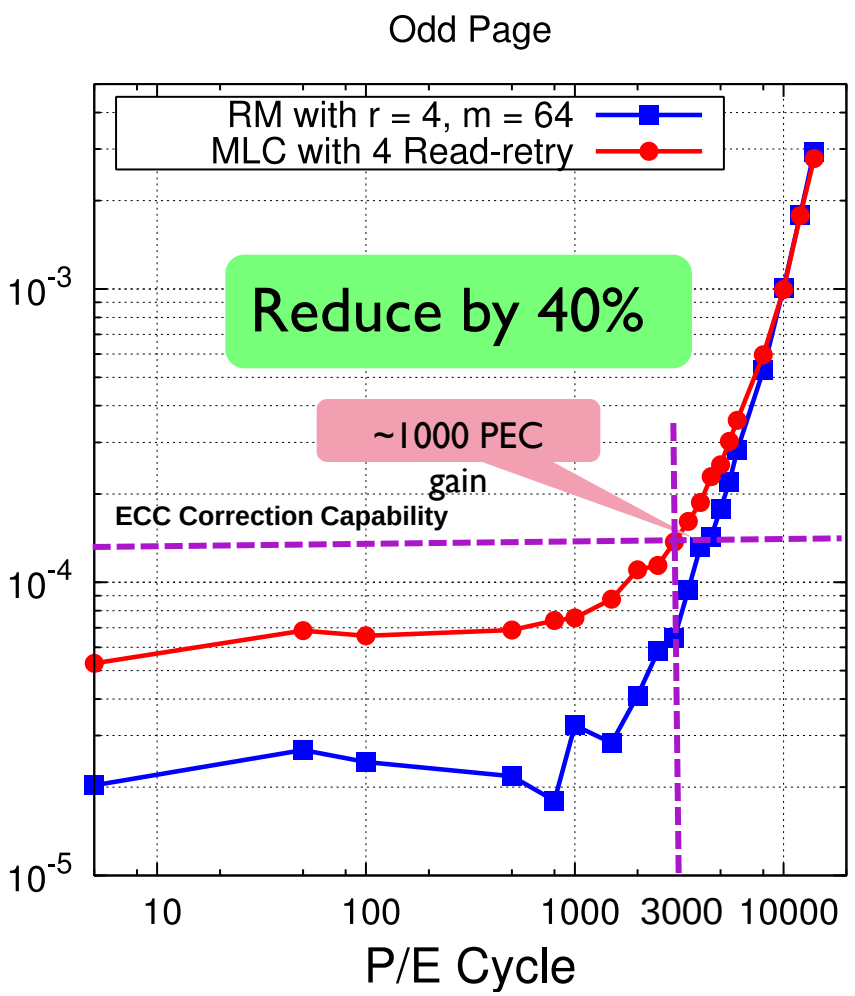
Interference-free Performance



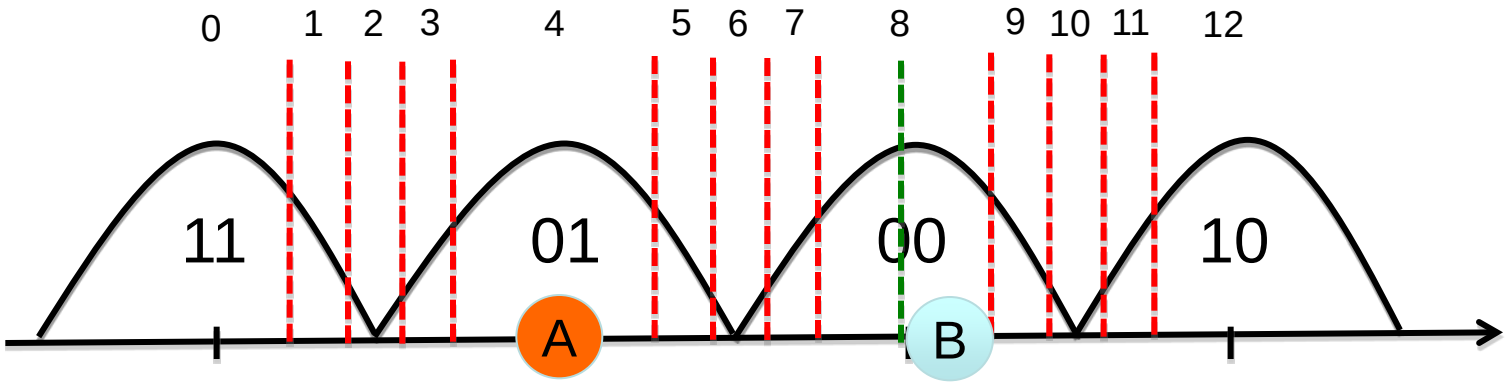
RM reduces the # of cell errors by 35%

Performance under Interference





Dominant Errors



Better control of reference threshold voltages, and access to more read-retry modes will help!

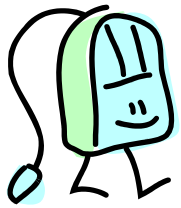
Summary

- Rank modulation
  - is a modulator using relative order of voltages
  - does not require redesigning flash
  - reduce cell errors by 35% ~ 40% (comparing to MLC)

- Ongoing work
  - More characterizations, e.g. under retention, hardware latency
  - Life time characterizations with ECC
  - Supporting more chips from different vendors

Acknowledgement

- Collaborators
  - Eyal En Gad (Caltech)
  - Dr. Yanjun Ma (Intellectual Ventures)
  - Prof. Edwin Kan (Cornell)
  - Kai Li and Oliver Hambrey (Siglead)
- Vendors
  - Micron NAND support team
  - Hynix NAND flash technical marketing/FAQE team
- Funding agencies
  - Caltech office of technology transfer
  - Intellectual Ventures



THANK YOU