

# Error Characterization and Comparison of ECCs on MLC and TLC Flash Memories

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# Outline

- Flash Memory Basics
- Error Characterization
- Performance comparison of BCH, LDPC codes
  - Various decoding techniques
- Polar Codes
  - LP Decoding of Polar codes



# Acknowledgment

## **CMMR – STAR Group Members**

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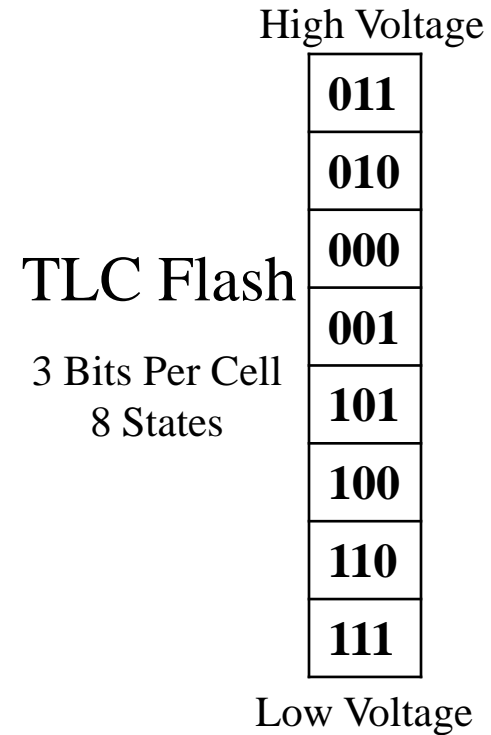
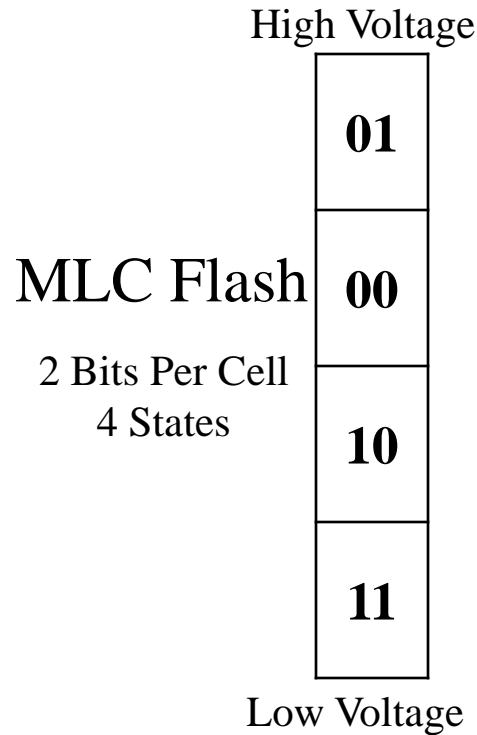
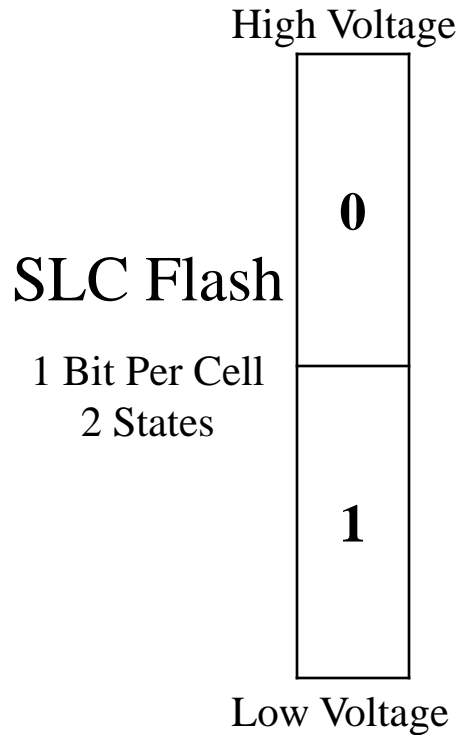
Aman Bhatia

Minghai Qin

# Flash Memory Basics

- Arrays (“blocks”) of floating-gate transistors (“cells”)
- A cell can support  $q$  voltage levels e.g.,  $q = 2, 4, 8$ .
- Increasing the voltage level (program) of a cell is easy to do.
- To decrease a cell level, we must first erase its entire block, then re-program all cells.
- A block erase is costly in time, power and cell wear

# SLC, MLC, TLC Flash



# Flash Memory Structure - SLC

- Group of cells → Page
- Group of Pages → Block

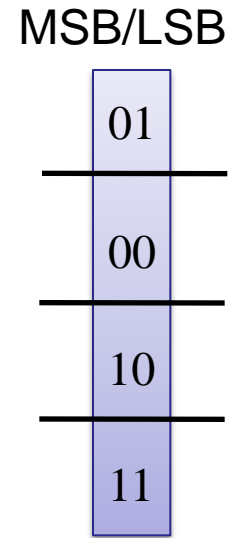
## Typical SLC Block Layout

page 0	page 1
page 2	page 3
page 4	page 5
.	.
.	.
.	.
page 62	page 63

# Flash Memory Structure - MLC

- 2 bits/cell → **MSB** and **LSB** pages

Row index	<b>MSB</b> of first $2^{14}$ cells	<b>LSB</b> of first $2^{14}$ cells	<b>MSB</b> of last $2^{14}$ cells	<b>LSB</b> of last $2^{14}$ cells
0	page 0	page 4	page 1	page 5
1	page 2	page 8	page 3	page 9
2	page 6	page 12	page 7	page 13
3	page 10	page 16	page 11	page 17
⋮	⋮	⋮	⋮	⋮
30	page 118	page 124	page 119	page 125
31	page 122	page 126	page 123	page 127



# Flash Memory Structure - TLC

- 3 bits/cell → **MSB**, **CSB** and **LSB** pages

Row index	<b>MSB</b> of first $2^{16}$ cells	<b>CSB</b> of first $2^{16}$ cells	<b>LSB</b> of first $2^{16}$ cells	<b>MSB</b> of last $2^{16}$ cells	<b>CSB</b> of last $2^{16}$ cells	<b>LSB</b> of last $2^{16}$ cells
0	page 0			page 1		
1	page 2	page 6	page 12	page 3	page 7	page 13
2	page 4	page 10	page 18	page 5	page 11	page 19
3	page 8	page 16	page 24	page 9	page 17	page 25
4	page 14	page 22	page 30	page 15	page 23	page 31
⋮	⋮		⋮	⋮		⋮
62	page 362	page 370	page 378	page 363	page 371	page 379
63	page 368	page 376		page 369	page 377	
64	page 374	page 382		page 375	page 383	
65	page 380			page 381		



# Error Characterization

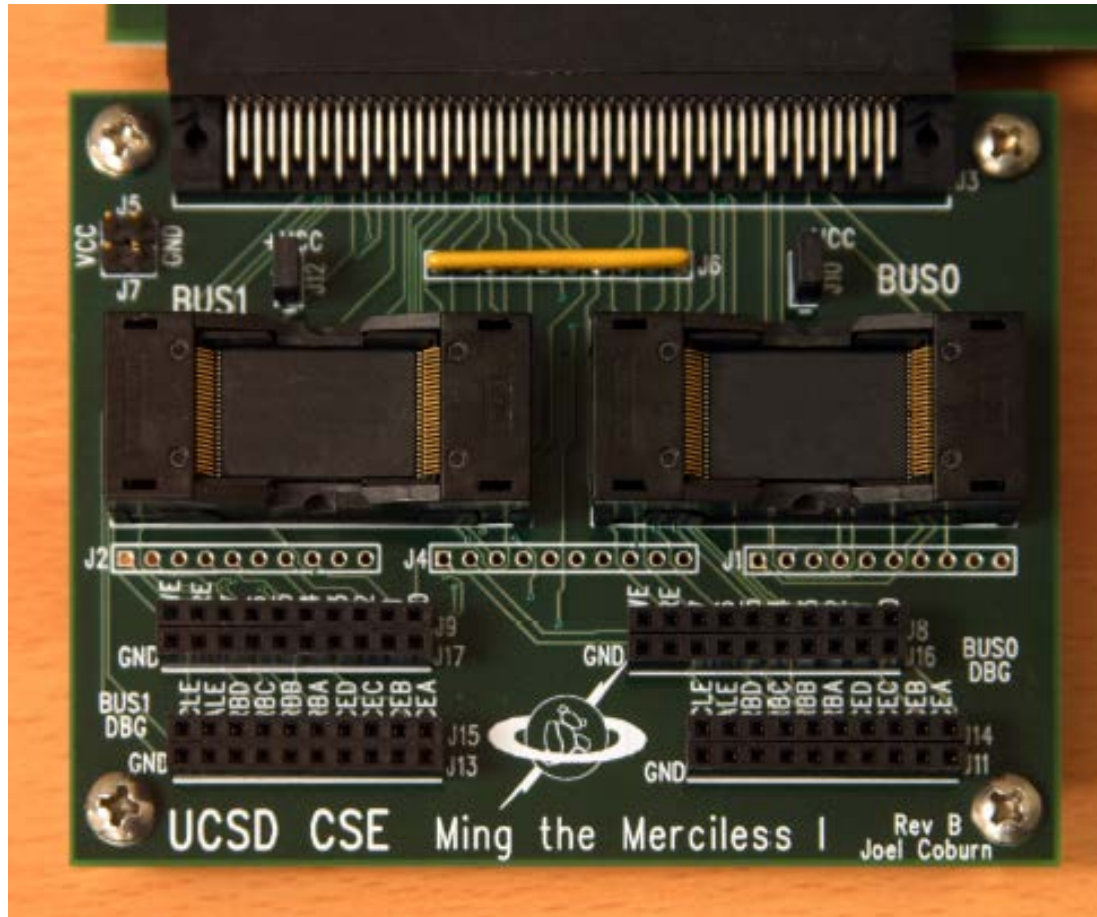
- Program/Erase (P/E) cycling of many blocks on MLC and TLC flash memories
- For each block the following steps were repeated:
  - The block is **erased**.
  - Pseudo-random data are **programmed** to the block.
  - The data are **read** and **errors** are identified.

## Disclaimers:

- We measured many more P/E cycles than the manufacturer's guaranteed lifetime of the device.
- The experiments were done in laboratory conditions and related factors such as temperature change, intervals between erasures, or multiple readings before erasures were not considered.

# Experiment Setup

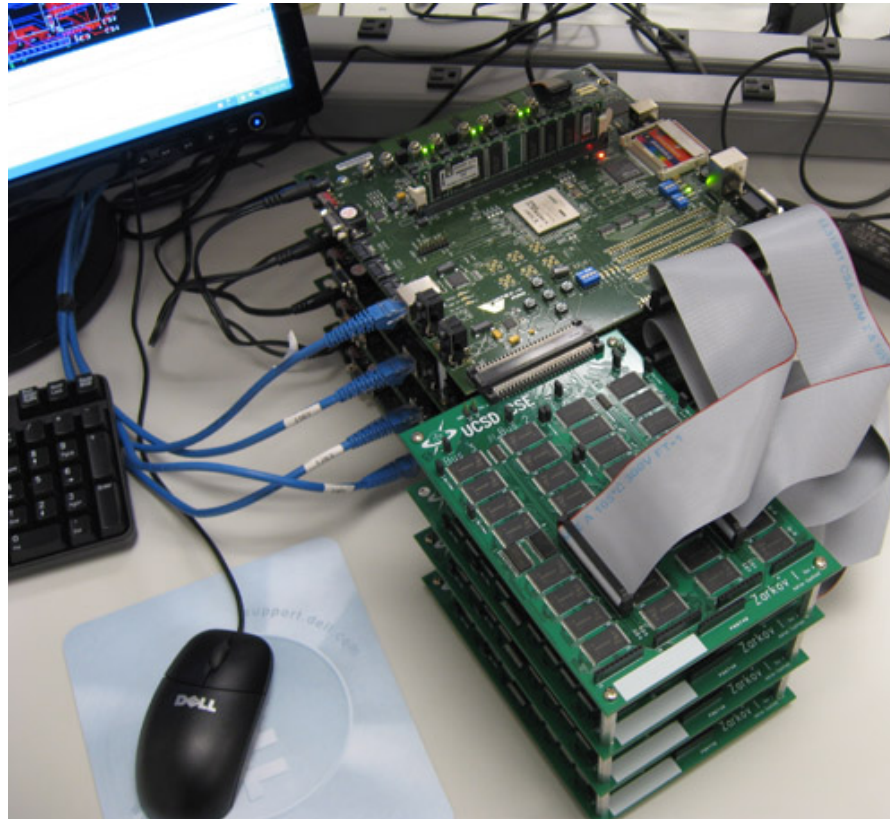
## Flash Chip Interface (Ming I Board)



Courtesy: Non-volatile Systems Laboratory, UCSD



# Experiment Setup FPGA Controller

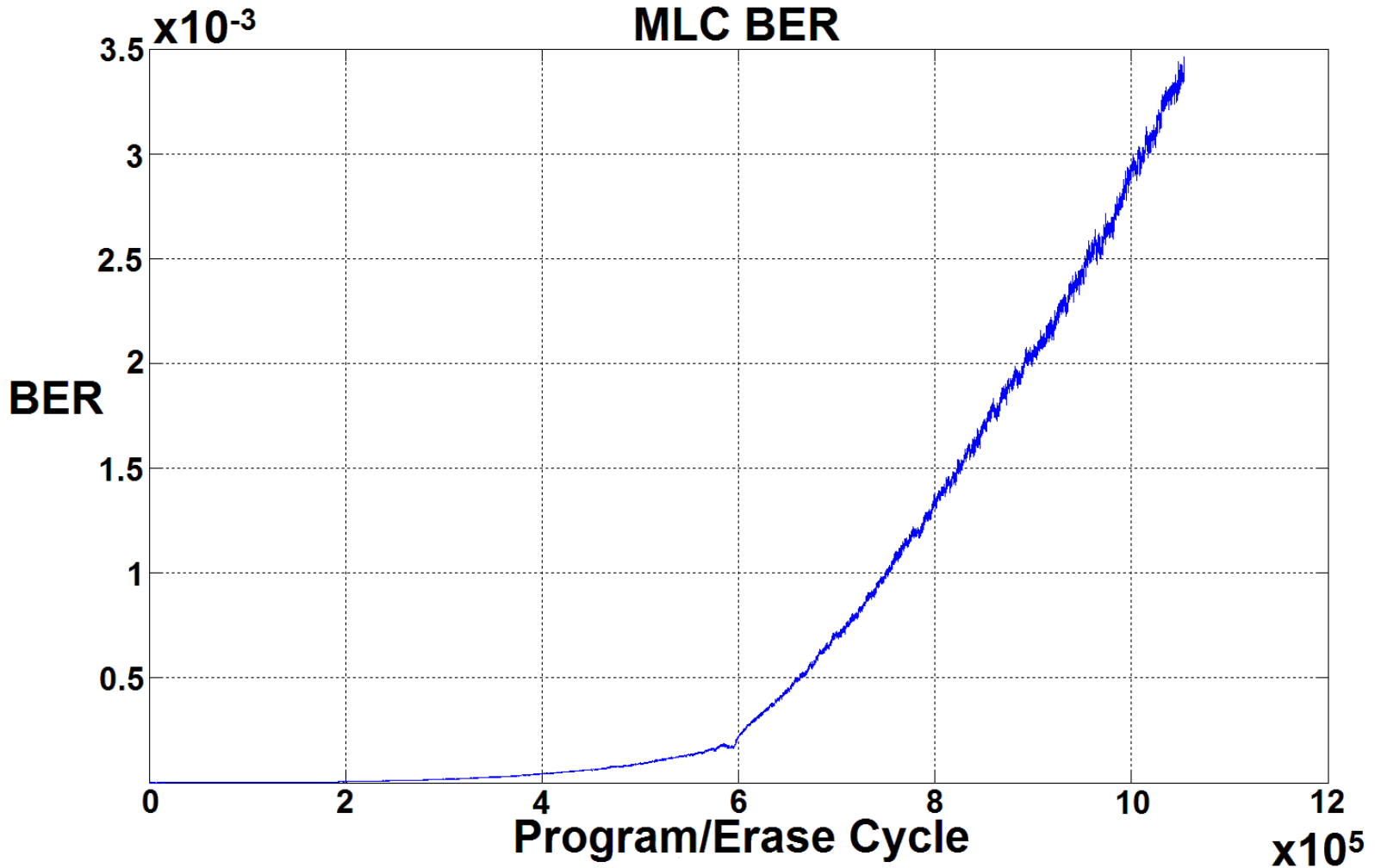


Courtesy: Non-volatile Systems Laboratory, UCSD

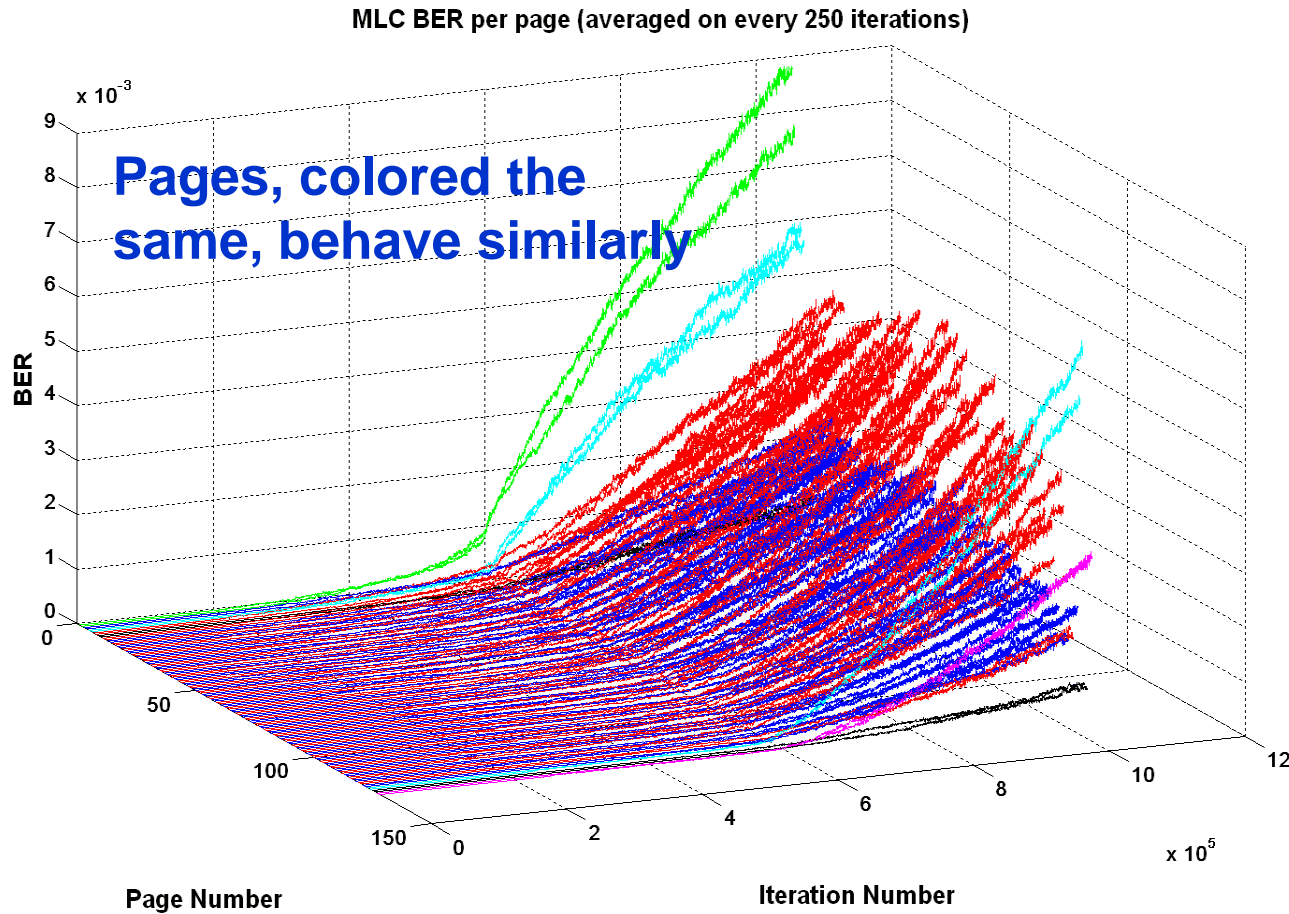


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Santa Clara, CA

# Results – BER, MLC



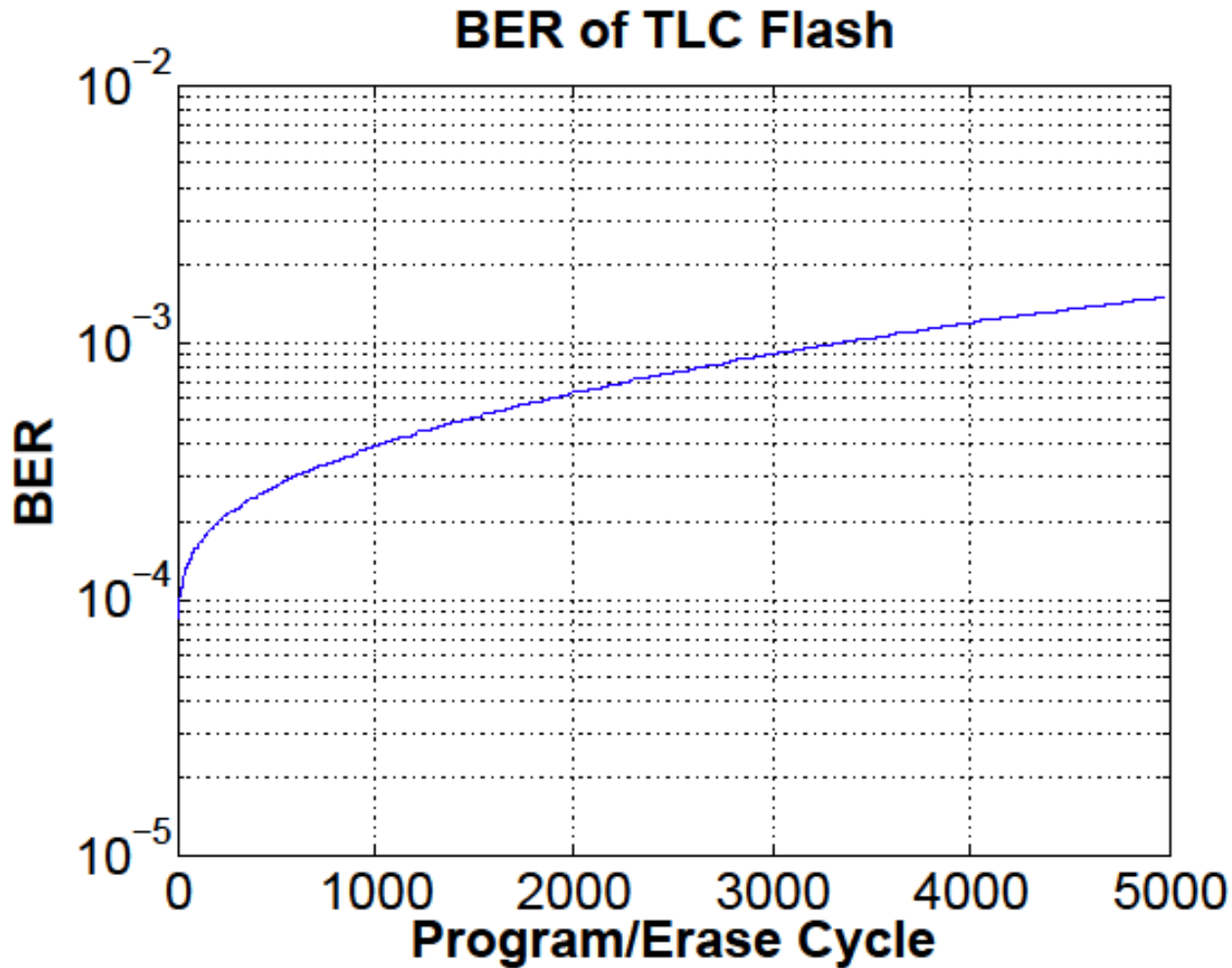
# Results – BER per page, MLC



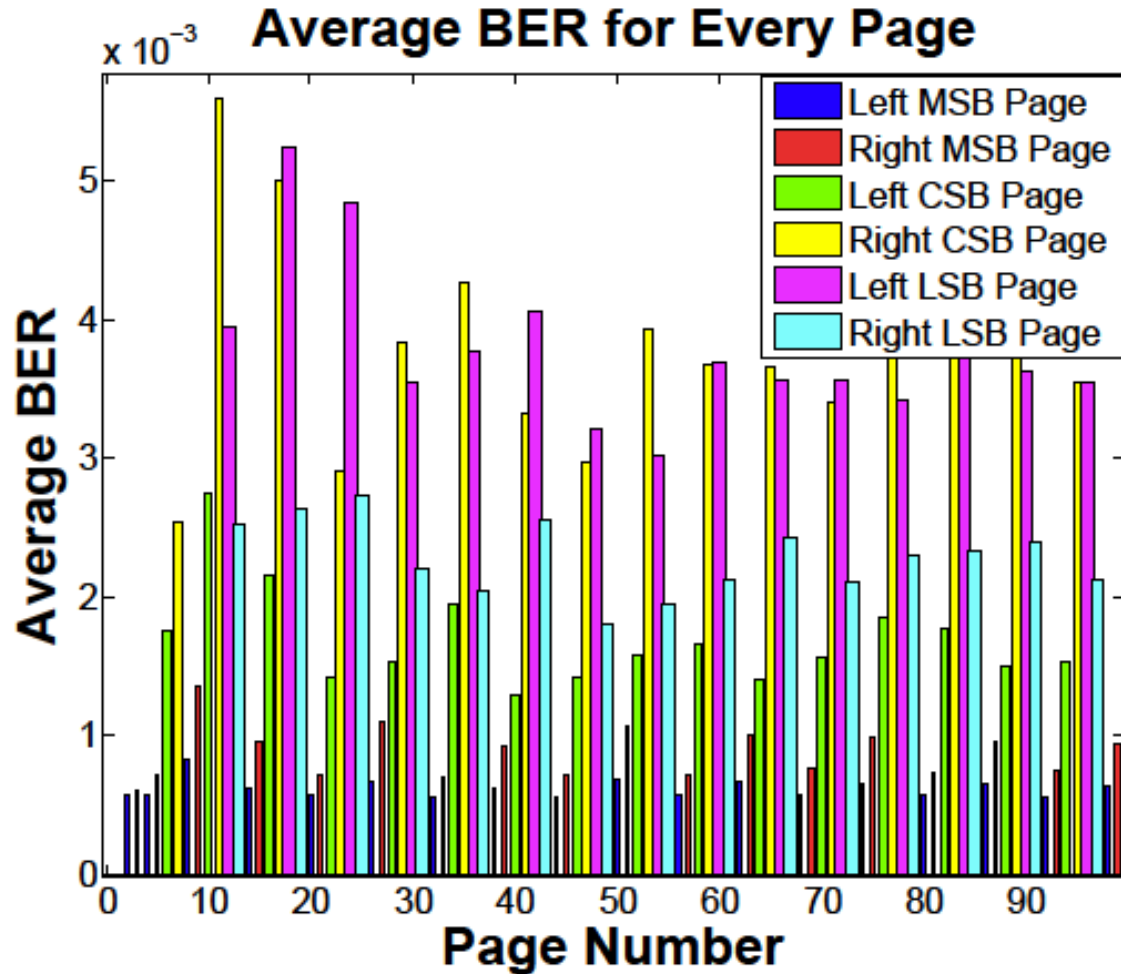
MSB/LSB

01
00
10
11

# Results – BER, TLC



# Results – BER per page, TLC



**M/C/L**

<b>011</b>
<b>010</b>
<b>000</b>
<b>001</b>
<b>101</b>
<b>100</b>
<b>110</b>
<b>111</b>



# ECC Comparison for TLC Flash

- BCH Codes
  - Length  $2^{16}$
  
- LDPC Codes
  - Gallager codes (3,k)-regular,  $R=0.8, 0.9, 0.925$ , length  $2^{16}$
  - AR4JA protograph-based codes,  $R=0.8$ , lengths 1280, 5120, 20480
  - MacKay codes variable-regular degree (3 or 4) ; no 4-cycles,  $R=0.82, 0.87, 0.93$ ; lengths 4095, 16383, 32000.
  - IEEE 802.3an\* (10Gb/s Ethernet),  $R \approx 0.84$ , length 2048.

\* Djurdjevic et al., *IEEE Commun. Letters*, July 2003.



# ECC Comparison for TLC Flash

- BER computed for the first 100 iterations, then every 25<sup>th</sup> iteration from then on.
- Data averaged over 6 TLC blocks.
- BCH decoder: corrects error patterns with up to  $t$  errors; detects and leaves unchanged more than  $t$  errors.
- LDPC decoders: assume binary symmetric channel model  $BSC(p)$ , with empirical error probability  $p$ .

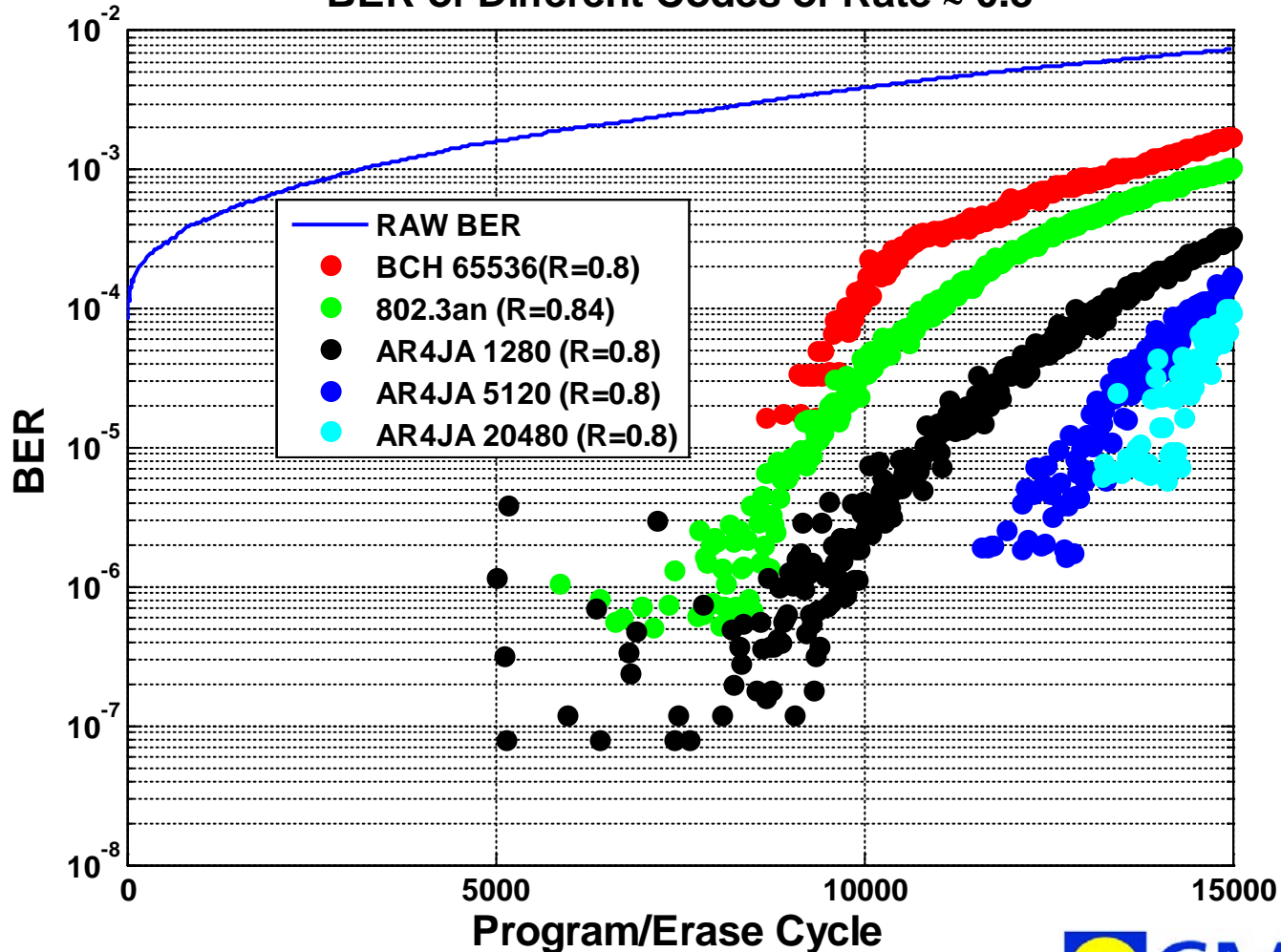
# LDPC Decoders

- Sum-product algorithm (SPA)
  - Floating-point, max iterations 200
  - (5+1)-bit quasi-uniform quantization
- Min-sum algorithm (MSA)
  - No LLR limits, max iterations 200
- Linear programming (LP) decoding
  - Alternating Direction Method of Multipliers (ADMM)\* with new fast “projection step”

\* Barman, et al., *Proc. 46<sup>th</sup> Allerton Conference*, Sept. 2011.

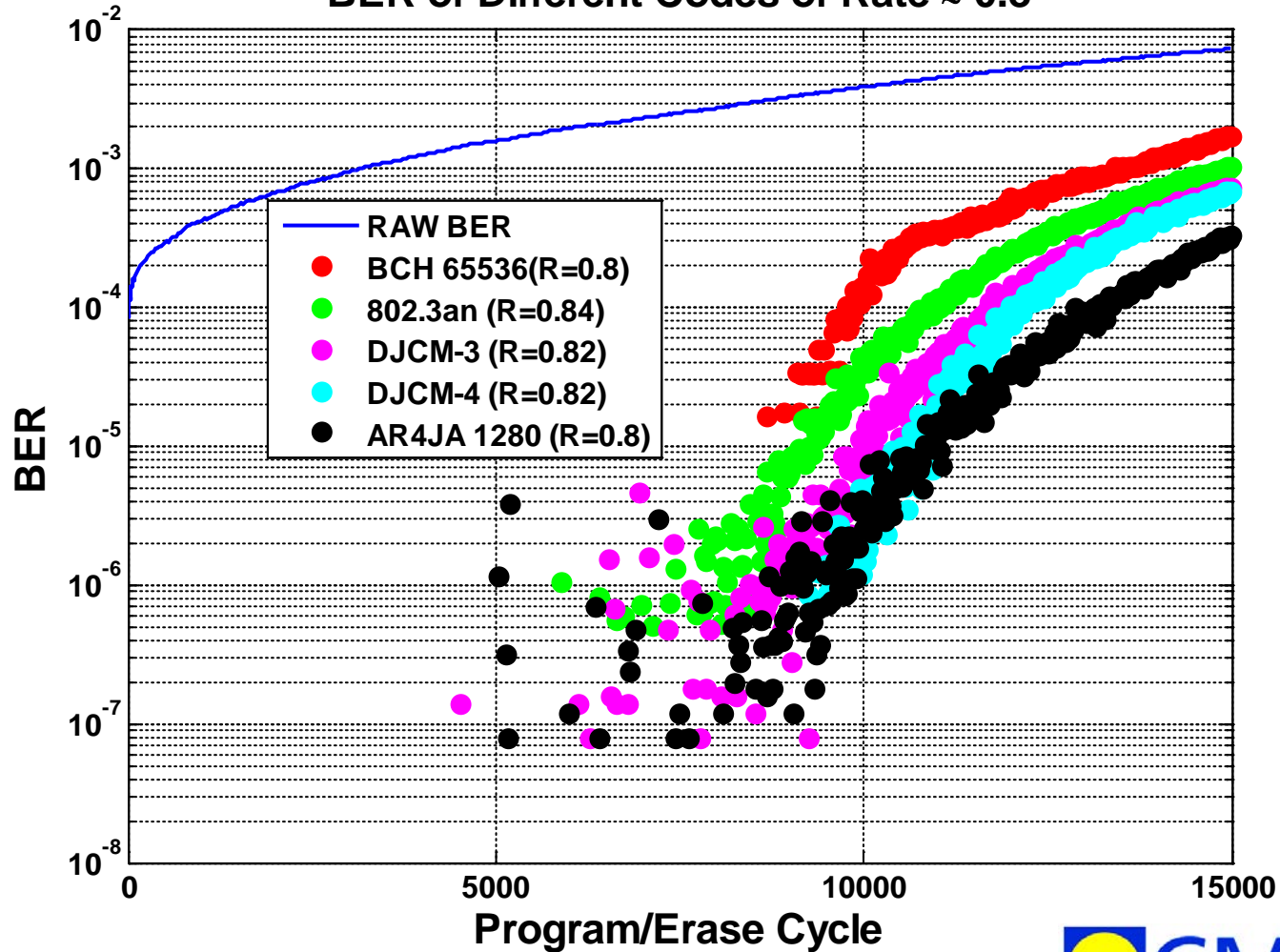
# Rate $\approx 0.8$ , LDPC codes with SPA Decoding

BER of Different Codes of Rate  $\approx 0.8$

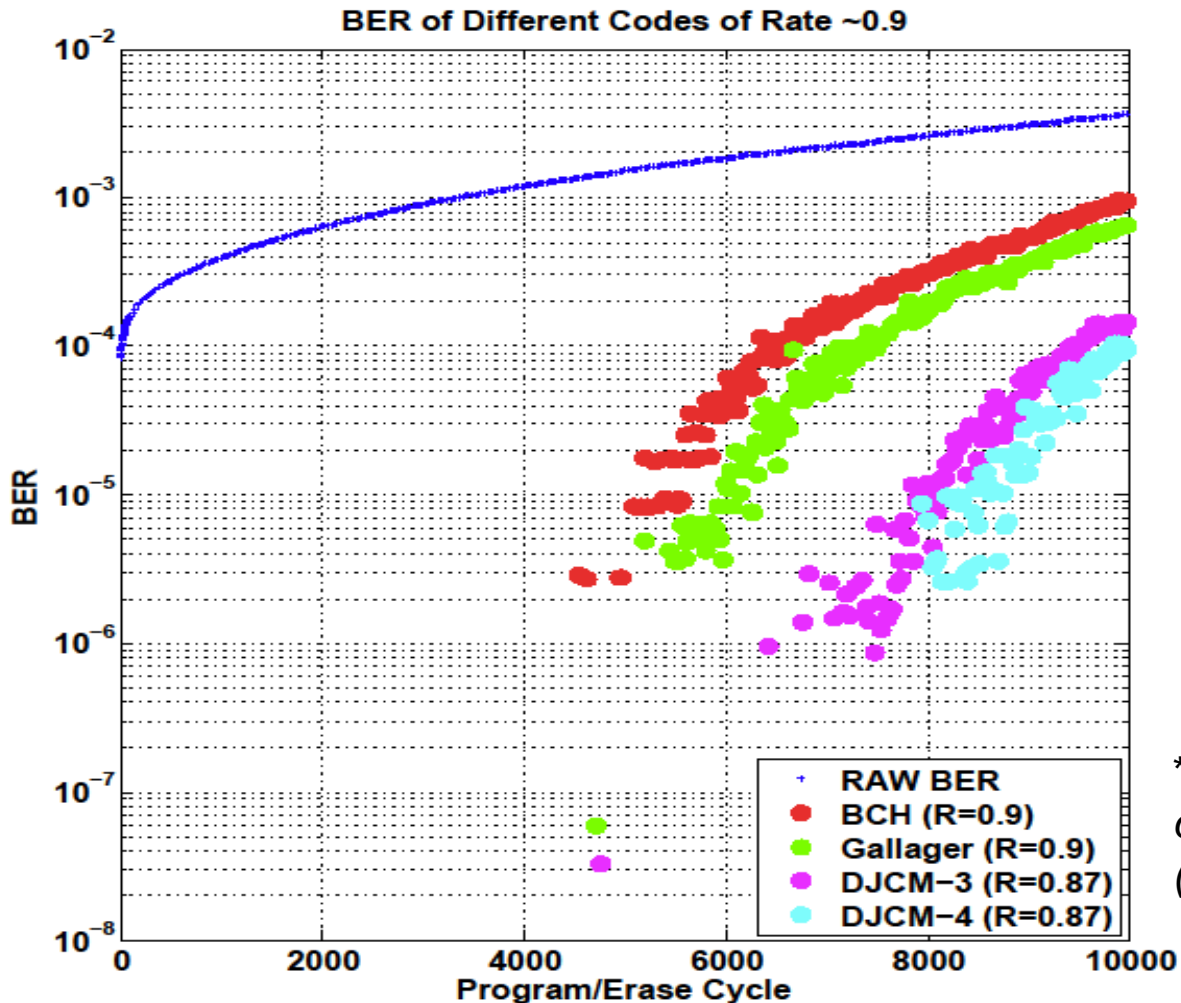


# Rate $\approx 0.82$ , LDPC codes with SPA Decoding

BER of Different Codes of Rate  $\approx 0.8$

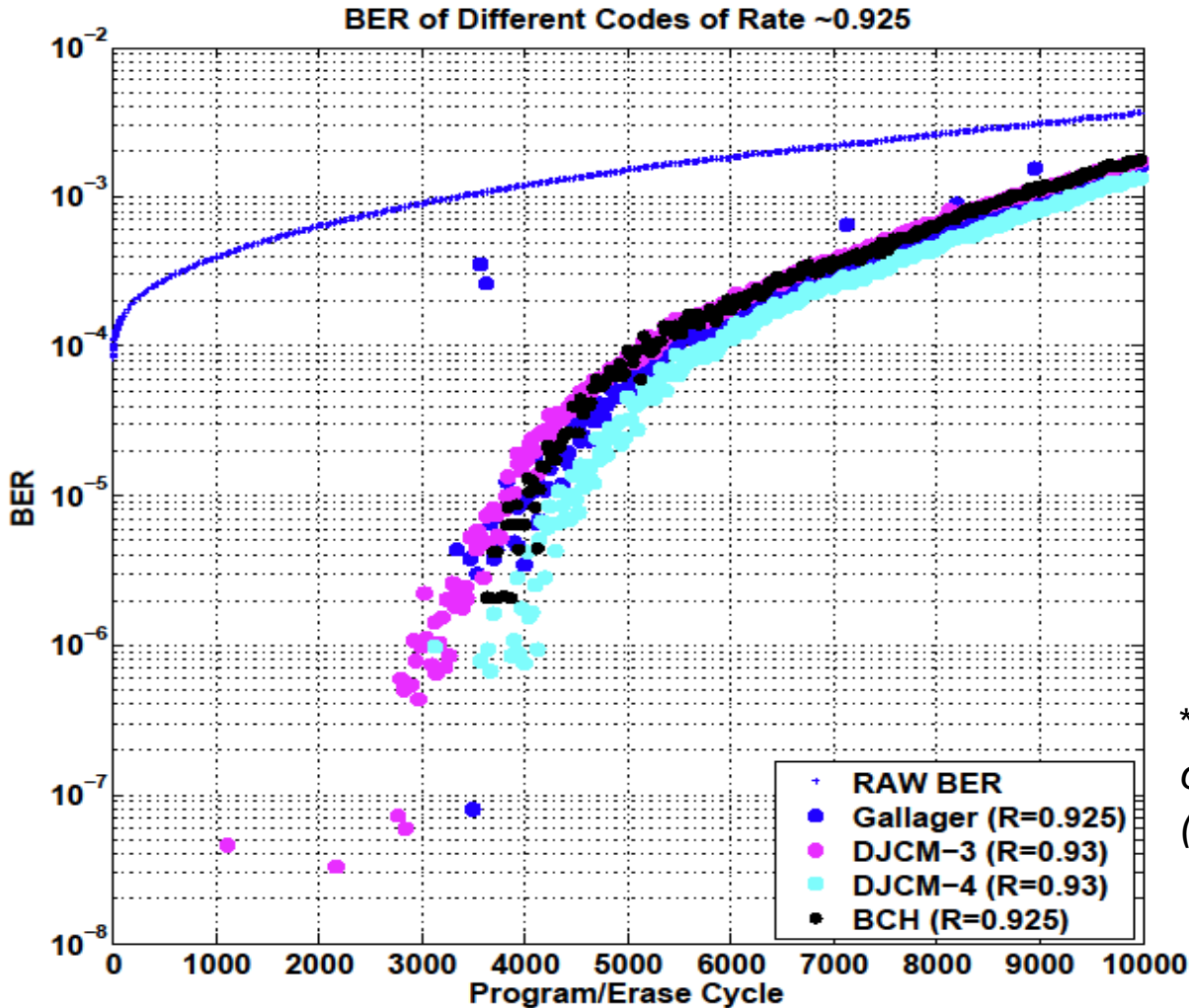


# Rate $\approx 0.9$ , LDPC codes with SPA Decoding \*



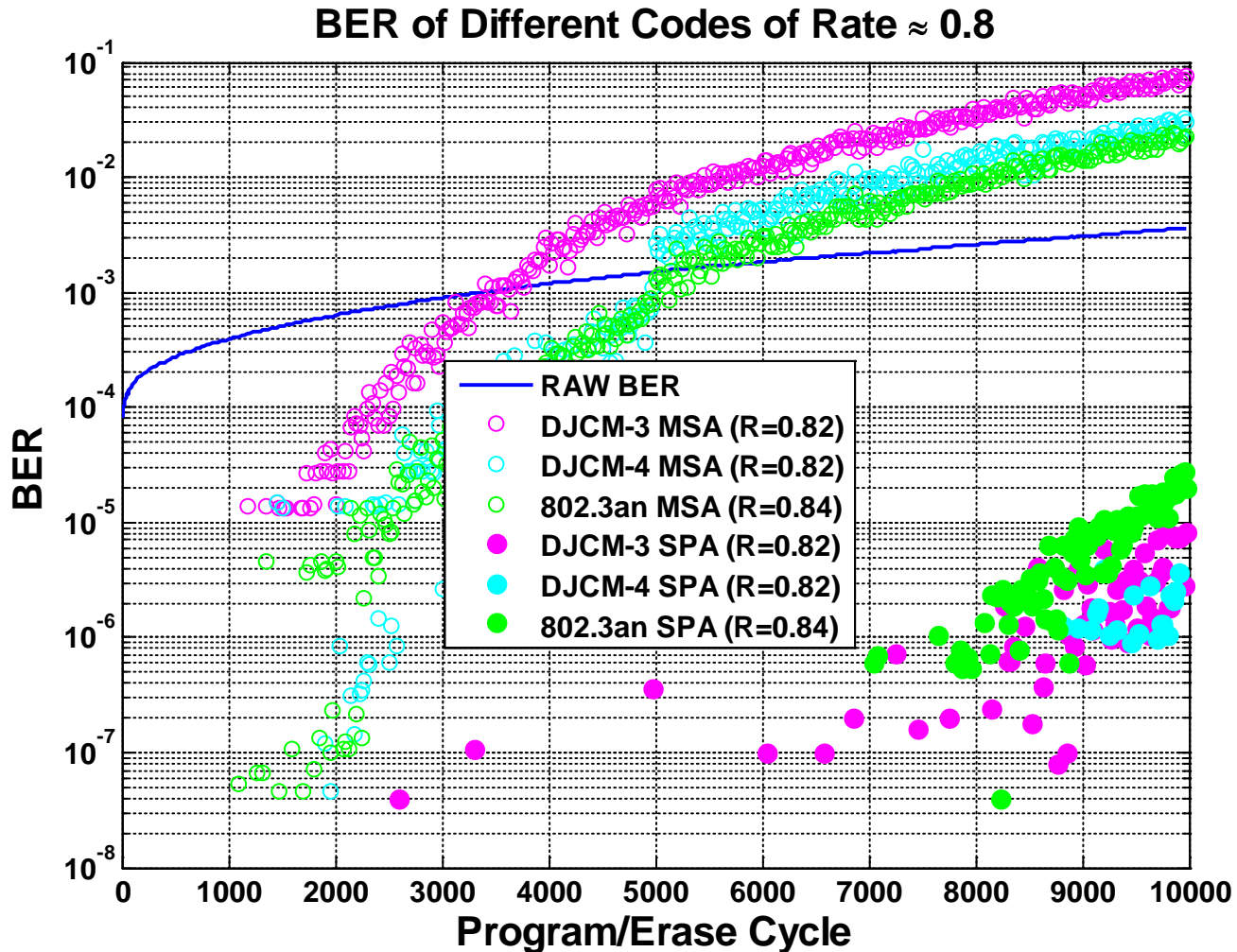
\*Yaakobi, et al., *Proc. Int. Conf. on Comp., Network. Commun. (ICNC)*, Jan.-Feb. 2012.

# Rate $\approx 0.925$ , LDPC codes with SPA Decoding



\*Yaakobi, et al., *Proc. Int. Conf. on Comp., Network. Commun. (ICNC)*, Jan.-Feb. 2012.

# Rate $\approx 0.8$ , MSA v/s SPA Decoding





# Other Decoding Techniques

- Linear Programming (LP) decoding of LDPC codes
  - Introduced by Feldman in 2003.
  - LP decoding with Alternating Direction Method of Multipliers (ADMM) proposed by Barman, et al., in 2011 to speed up LP decoding
  - A more efficient scheme based upon Adaptive LP decoding (ALP) with fast Cut-Search Algorithm (CSA) to further speed up the key “projection step” in LP-ADMM. <sup>1</sup>
- SPA with  $(q+1)$ -bit Quasi-uniform Quantization <sup>2</sup>

<sup>1</sup>X. Zhang and P. H. Siegel, *Proc. Int. Symp. on Info. Theory (ISIT)*, July. 2013.

<sup>2</sup>X. Zhang and P. H. Siegel, *Proc. IEEE SPCOM*, July. 2012.

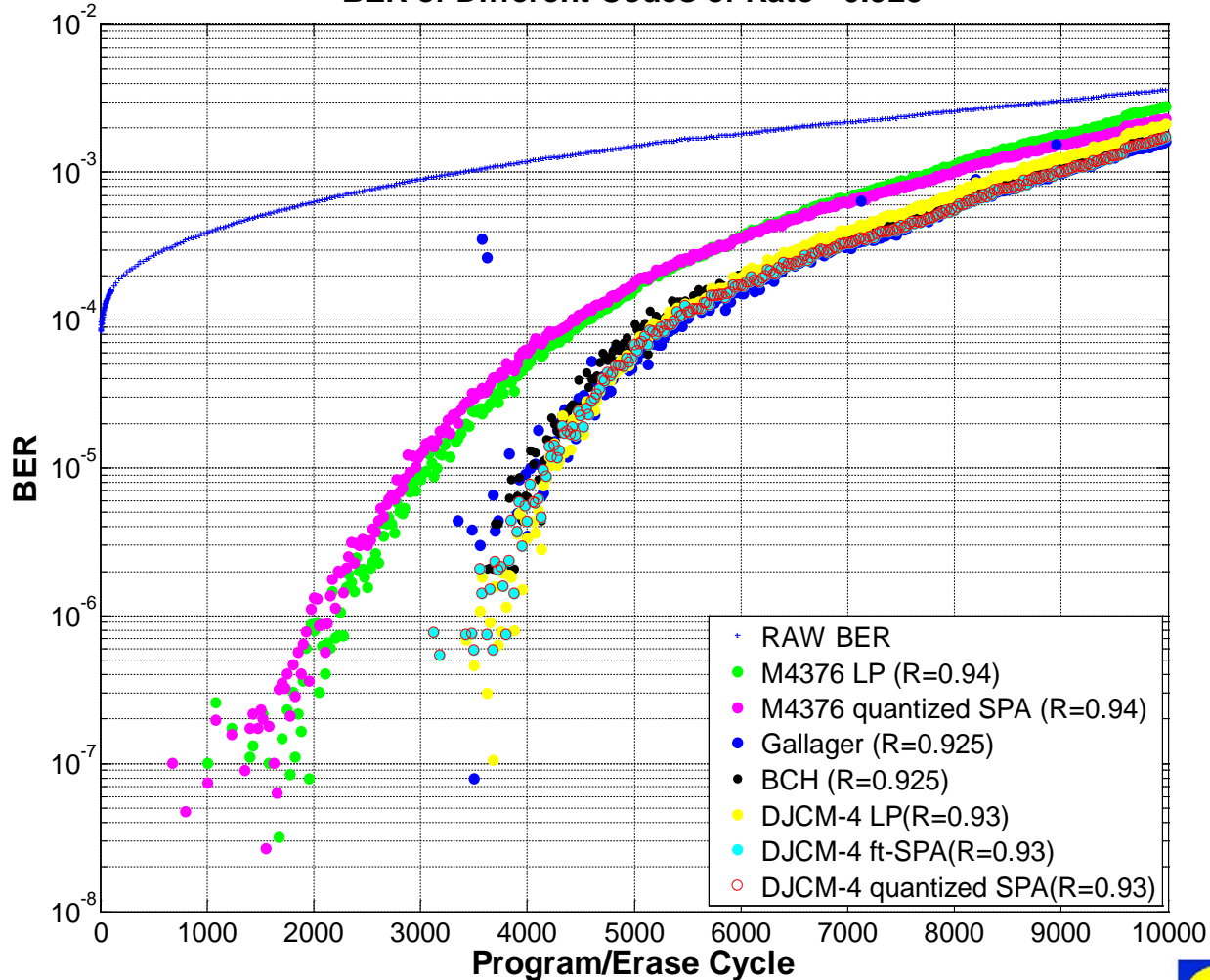


# Legend Notation

- **M4376**: MacKay code, length 4376 and rate 0.9356
- **DJCM-4**: MacKay code, length 3200 and rate 0.93
- **LP**: ADMM-based LP decoder, max iterations 200
- **ft-SPA**: floating-point SPA
- **Quantized SPA**: (5+1)-bit quasi-uniform quantized SPA

# Rate $\approx 0.925$ LP vs. SPA Decoding on TLC

BER of Different Codes of Rate  $\sim 0.925$



# Summary of Observations

- Best LDPC performance surpasses BCH at all code rates  $R \approx 0.8, 0.9, 0.925$ .
- $R \approx 0.8$  LDPC codes at 15k cycles has BER comparable to  $R \approx 0.9$  LDPC codes at 10k cycles.
- MSA was inferior to SPA decoding at  $R \approx 0.8$ .
- LP-ADMM was comparable to SPA decoding at  $R \approx 0.925$ , with slightly steeper slope.
- (5+1)-bit quasi-uniform quantized SPA (not optimized) matches floating-point SPA.

# Polar Codes

- Based on the phenomenon of channel polarization
- Achieve the capacity of symmetric binary input discrete memoryless channels under successive cancellation (SC) decoding \*
- CRC concatenated Polar codes with SC-List decoding can beat LDPC code performance (Tal and Vardy, 2011)

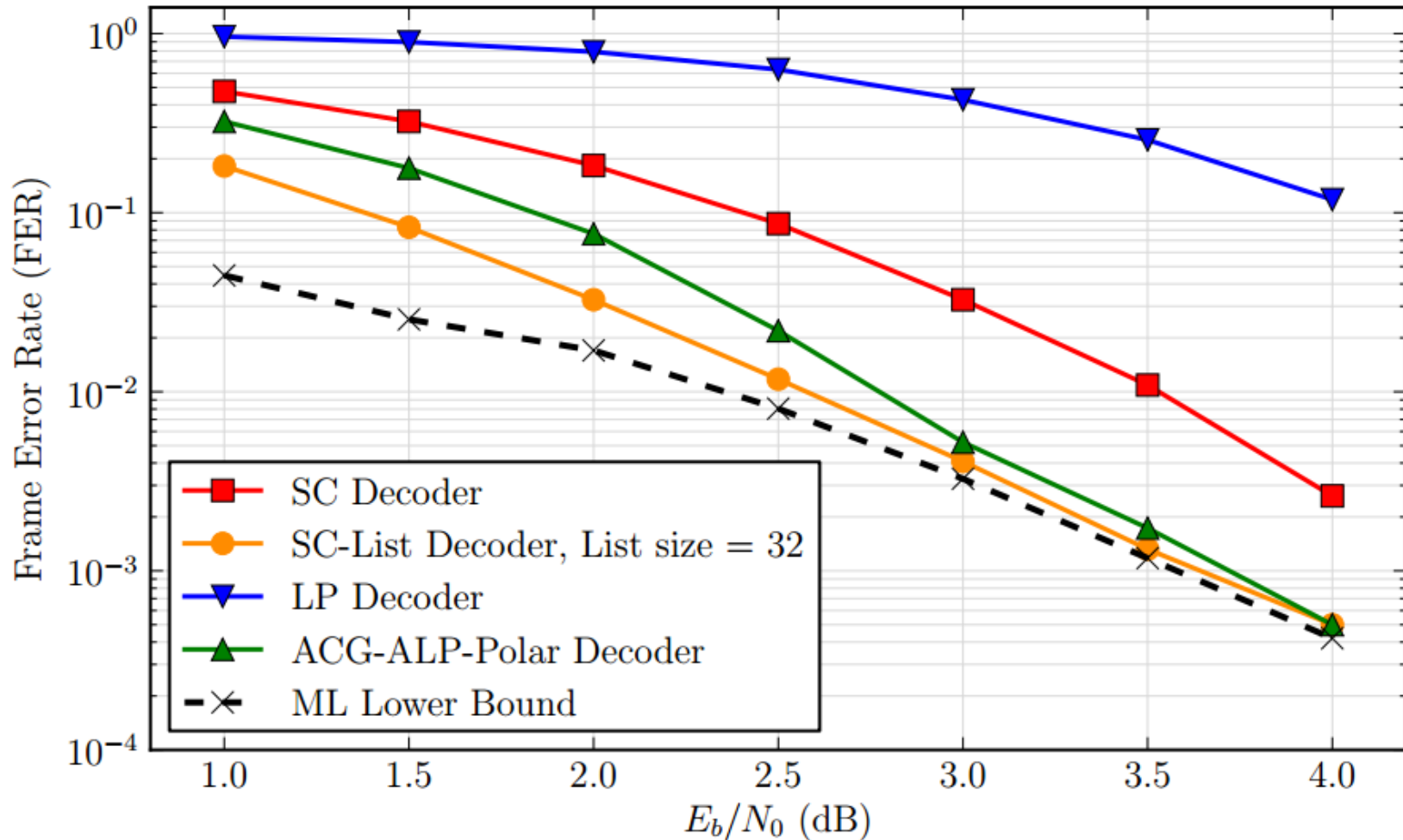
\*E. Arikan, *IEEE Trans. on Info. Theory*, July. 2009.

# LP Decoding of Polar Codes

- High density parity check codes
- Goela et al. in 2010 proposed a sparse LP polytope representation which works for a binary erasure channel but doesn't work well for a binary AWGN channel.
- We present results using a modified adaptive LP decoder for polar codes and a lower complexity polytope representation based on reduction of the polar code sparse factor graph.\*

\*V. Taranalli and P. H. Siegel, *Proc. Int. Symp. on Info. Theory (ISIT)*, June-July. 2014.

# (128, 64) Polar Code over a BAWGN channel



# Future Directions

- Characterization of inter-cell interference (ICI) and design of codes to combat it, e.g., ECC + constrained codes.
- Optimization of ECC schemes for better flash memory channel models e.g., asymmetric channels, non-binary channels, time-varying channels.
- Adaptation of new ECC techniques (polar codes, spatially-coupled LDPC codes) to flash memory applications.



Thank You!