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Designing a Configurable NVM Express Controller/Subsystem

Ravi Thummarukudy

"The IP enabled solutions provider"

AGENDA

- Company Overview
- NVMe SSDC Subsystem
- NVMe Features & Configurability
- Configurable IP Components
- Summary

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The Mobiveil Team

- **Leadership**
  - Management with 25+ years experience in Semiconductor/Silicon IP/Systems/software
  - 100+ member development team with previous experience in high speed interfaces located in US & India
  - Previously founded GDA Technologies, Inc and grew to strong IP and Services group , 500+ engineers strong.

Key differentiators

Developed several highly configurable key high speed IP blocks in the last 10+ years (PCI Express, Hyper Transport, Serial RapidIO, SPI4.2, DDR4/3,Flash Controllers etc)

Locations

Headquarters in Milpitas, CA
India design centers: Chennai & Bangalore
Sales: Offices/Reps worldwide

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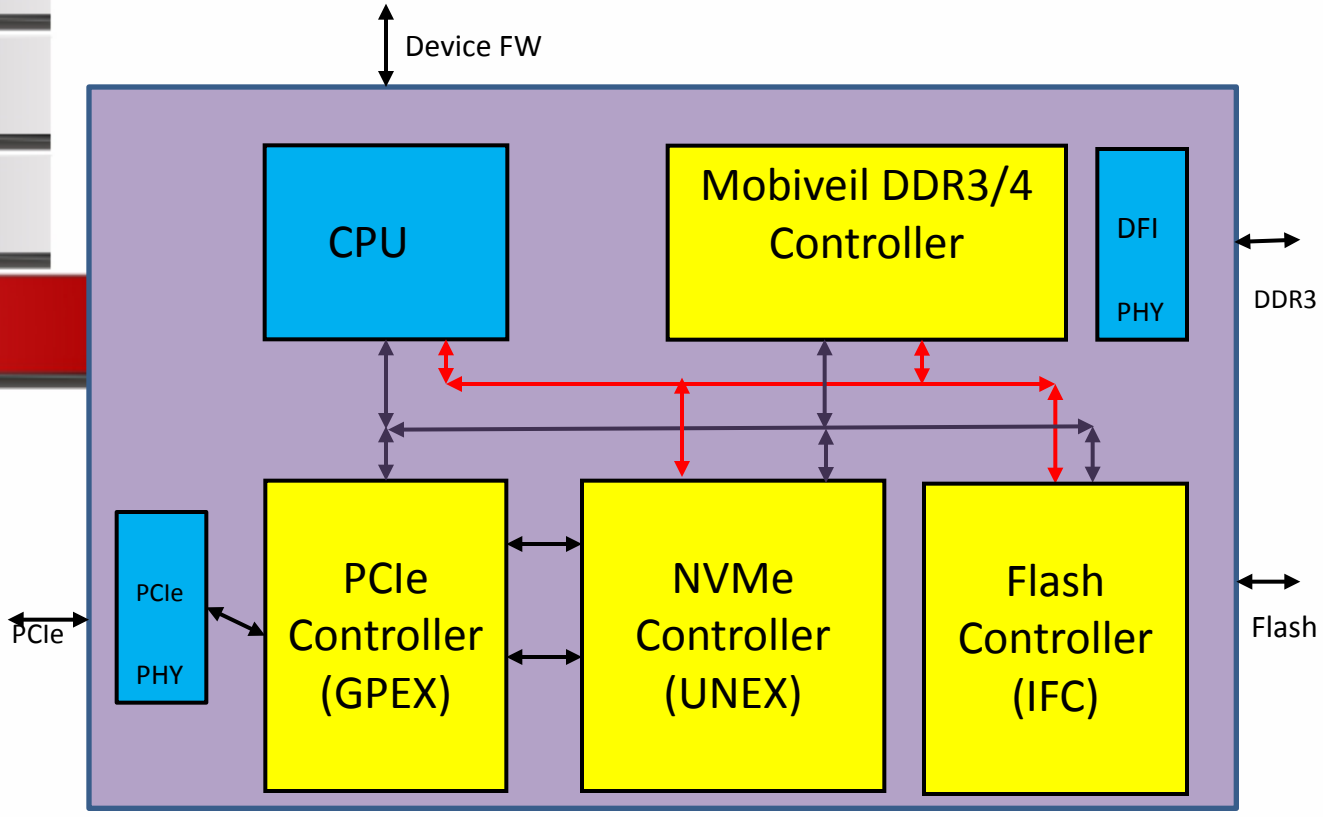
NVMe SSDC Subsystem

Company Overview
NVMe SSDC Subsystem
NVMe Features & Configurability
IFC
Summary

Mobiveil NVMe SSDC Subsystem



PCI EXPRESS™

nvm EXPRESS

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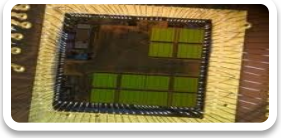
Mobiveil Subsystem IP Advantages

- Company Overview
- NVMe SSDC Subsystem
- NVMe Feature & Configurability
- Configurable IP Components
- Summary



Superior Technical Solution: *Most Feature rich IP, Complete Customization and delivery Solution*

Market leading & most exhaustively proven cores in the market: *Industry leaders are using these cores*

Consortium Participation : NVM Express- Member, *RIO – Member, PCISIG – Member, HMC - Member*

Support: *Clear IP Focus & Worldwide Support*

3rd Party Partnerships for complete Solution:
(VIP PHY IP,s, FPGA, eASIC and SOC Partners)

Standard Body Certified Cores: *All Mobiveil IPs are validated and certified: PCI Plug fest, UNH, RTA*

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Company Overview
NVMe SSDC Subsystem
NVMe - Features
Configurable IP Components
Summary

NVMe - Features

- A Register level interface that allows host software to communicate with a non-volatile memory subsystem
- Defines a standard command set for use with the NVM subsystem
- Optimized for Enterprise and Client solid state drives, typically attached to the PCI Express interface
- Defines Pair of Submission and Completion IO Queues
- Defines parallel operation by supporting up to 64K I/O Queues with up to 64K commands per I/O Queue.
- Defines many Enterprise capabilities like end-to-end data protection, enhanced error reporting, and virtualization
- Supports differentiated services, i.e., different qualities of service (QoS)Targets
- Supports Multi-Path IO and Namespace Sharing capabilities
- Supports Reservations
- Supports multiple name spaces

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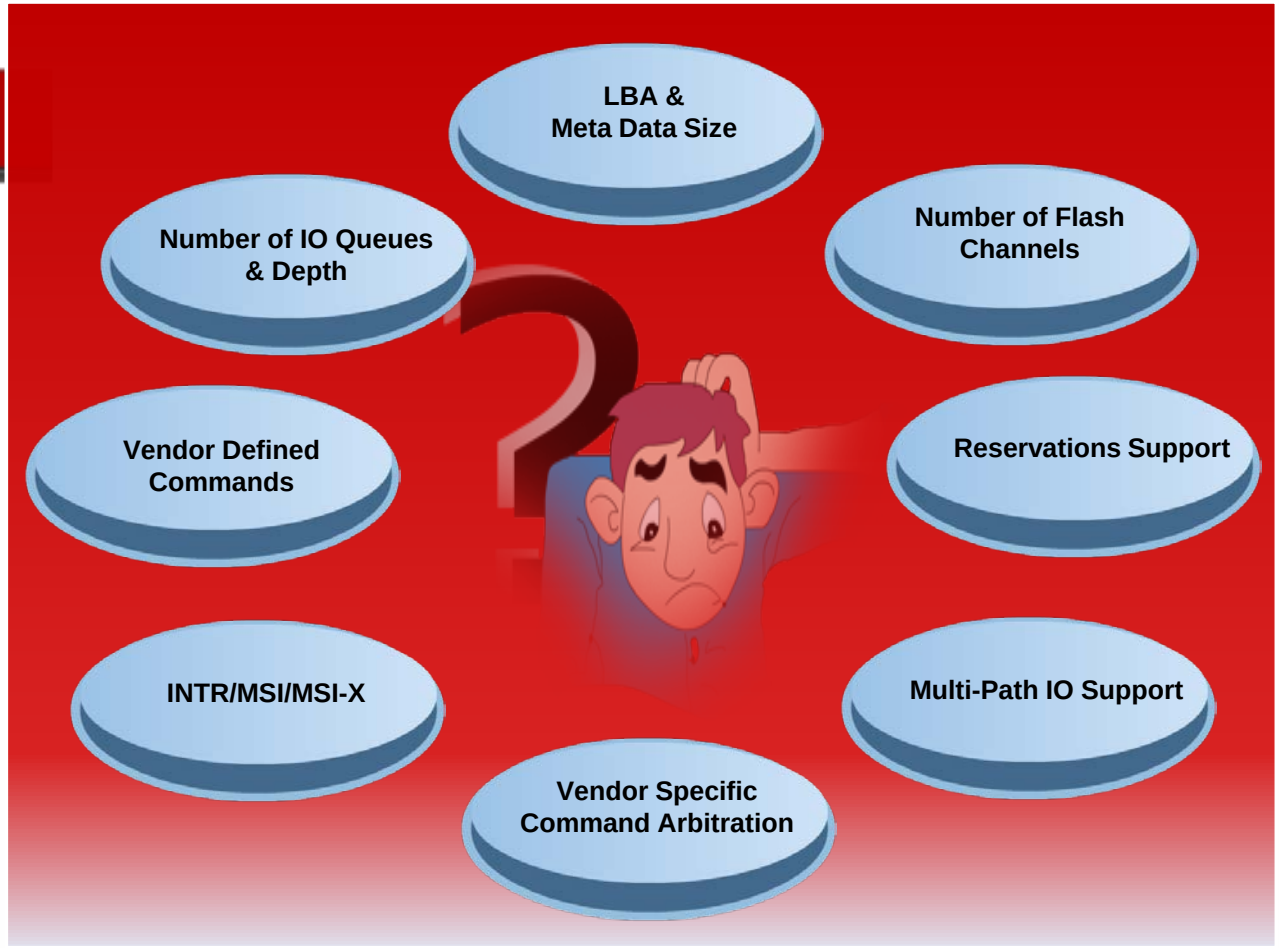
Company Overview
NVMe SSDC Subsystem
NVMe Configurability
Configurable IP Components
Summary

NVMe Configurability



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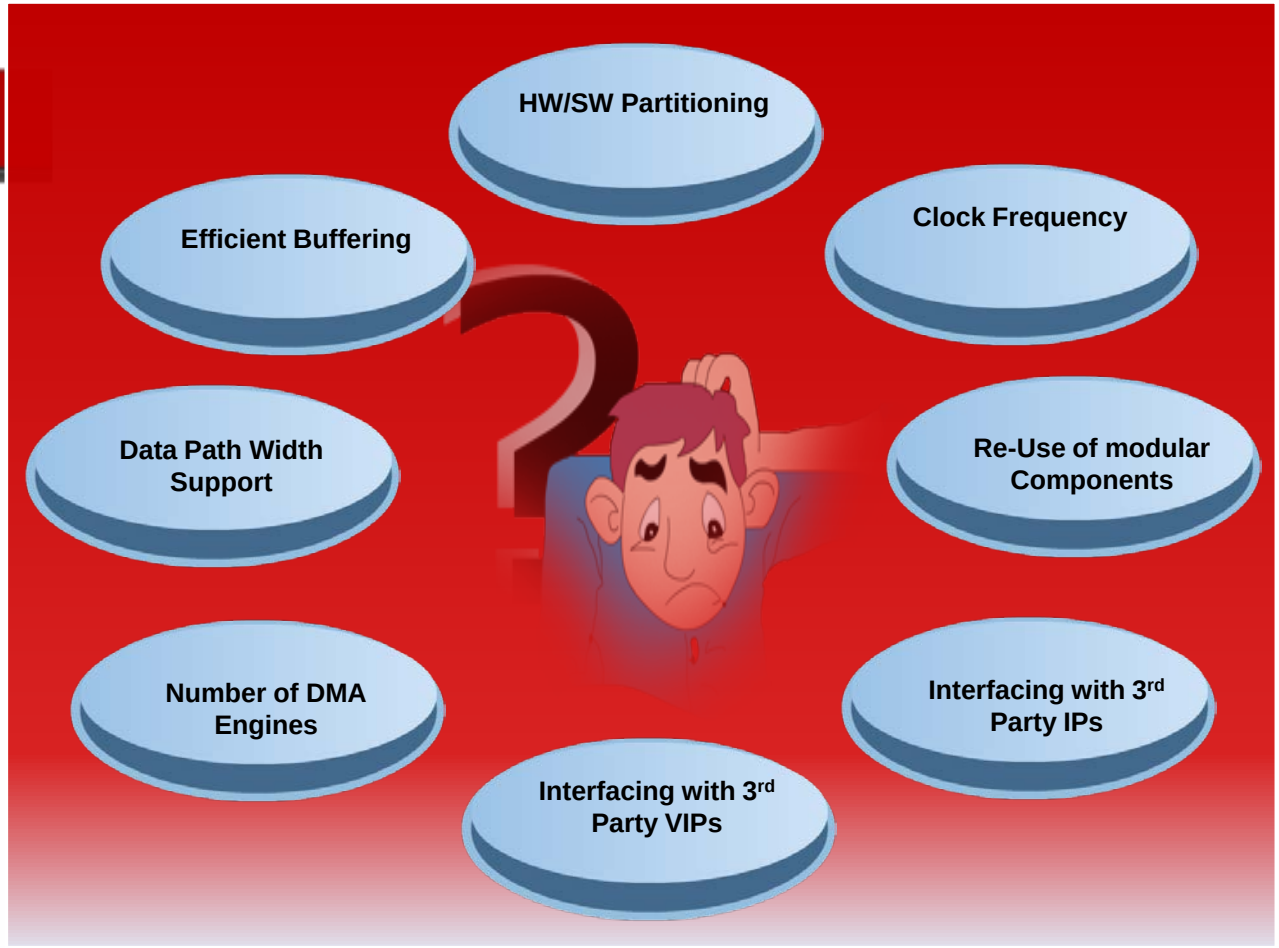
Company Overview
NVMe SSDC Subsystem
NVMe Configurability
Configurable IP Components
Summary

NVMe Configurability



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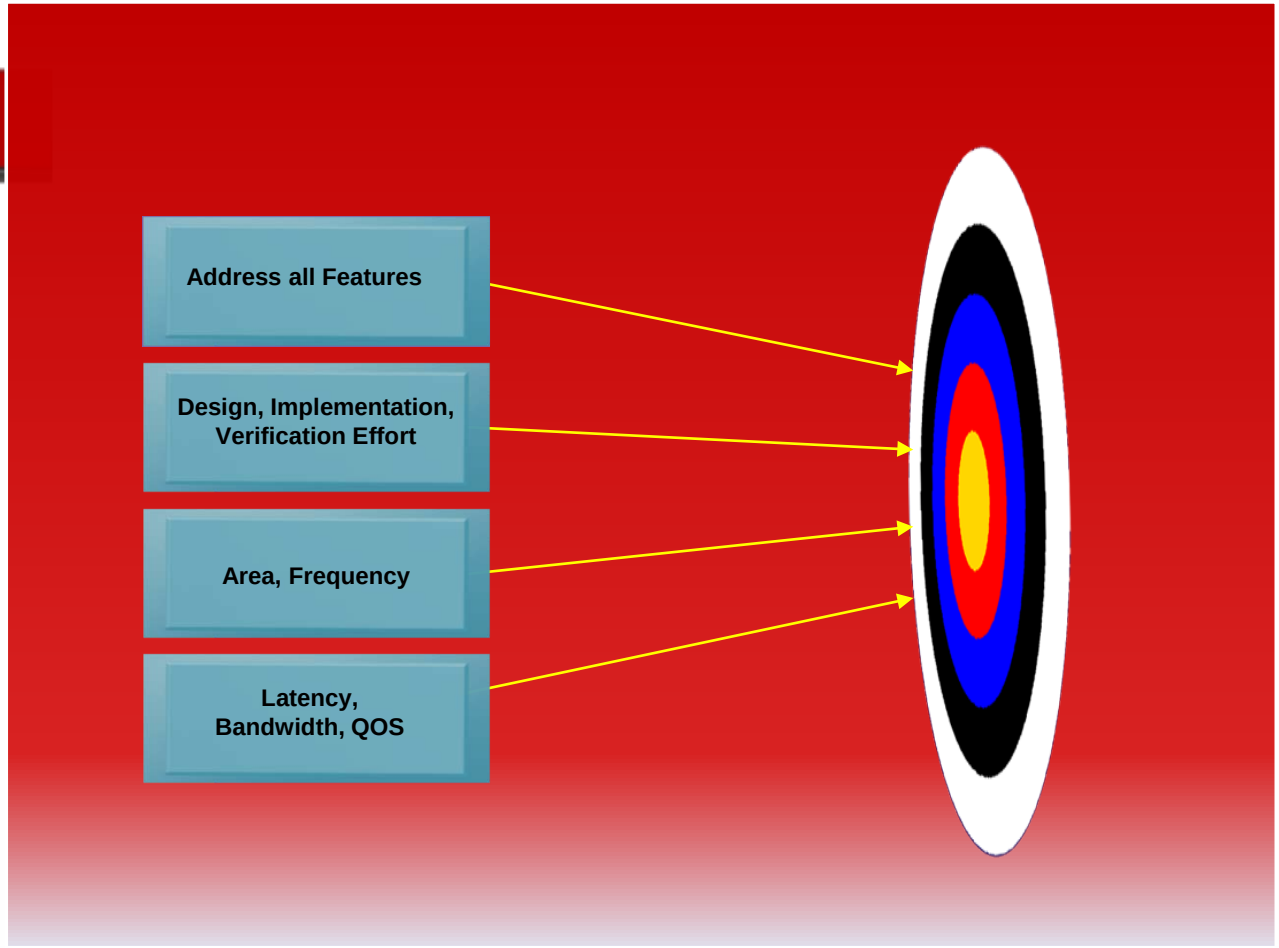
Company Overview
NVMe SSDC Subsystem
NVMe Controller
Configurable IP Components
Summary

Configurable NVMe Controller



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Configurable IP Components

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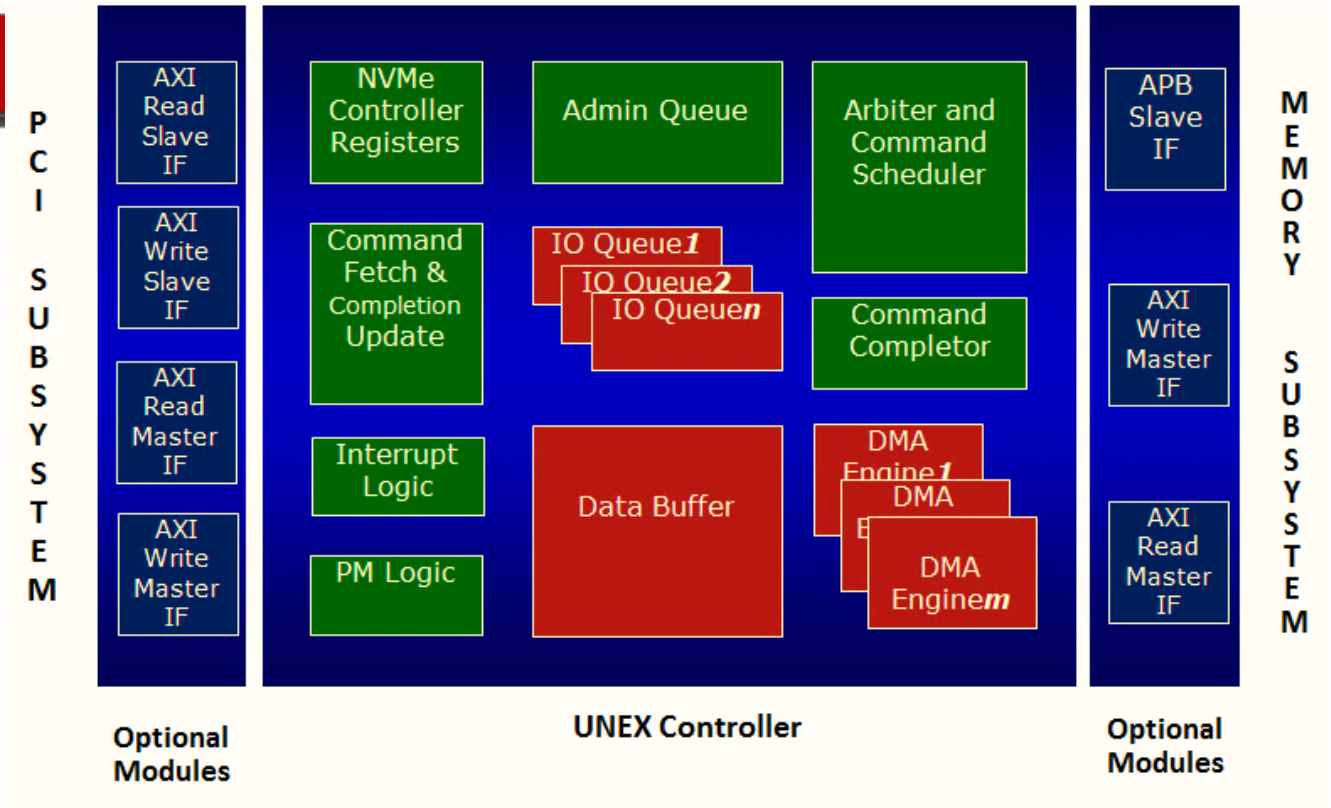
NVM Express Controller (UNEX)

Industry's First IP to Pass UNH –IOL Certification

Company Overview
NVMe SSDC Subsystem
NVMe Features & Configurability
UNEX
Summary

NVM Express (UNEX) Controller

- ✓ **Highly Configurable**
- ✓ **Technology Independent**



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Company Overview
NVMe SSDC Subsystem
NVMe Features & Configurability
UNEX
Summary

UNEX Features

- Compliant to NVM Express 1.1 specification
- Supports configurable number of IO Queues
- Supports configurable Queue depth
- Supports Round Robin or Weighted Round Robin with Urgent Priority arbitration mechanism
- Host memory page size support of 128MB
- Efficient and Streamlined Command handling
- Supports Fused Operations
- Supports All Optional Admin Commands
- Supports All Optional NVM Commands
- Supports Multi-Path IO and Namespace Sharing capabilities
- Supports Reservations
- Supports multiple name spaces
- Optional AXI interfaces for NVMe implementation in SoC
- Well defined Command Interface for local CPU to perform subsystem initialization and to handle all non-hardware accelerated commands
- Targets FPGA, Structured ASIC and Standard Cell technologies

✓ **Highly Configurable**
✓ **Technology Independent**

nvm EXPRESS
UNH Certified

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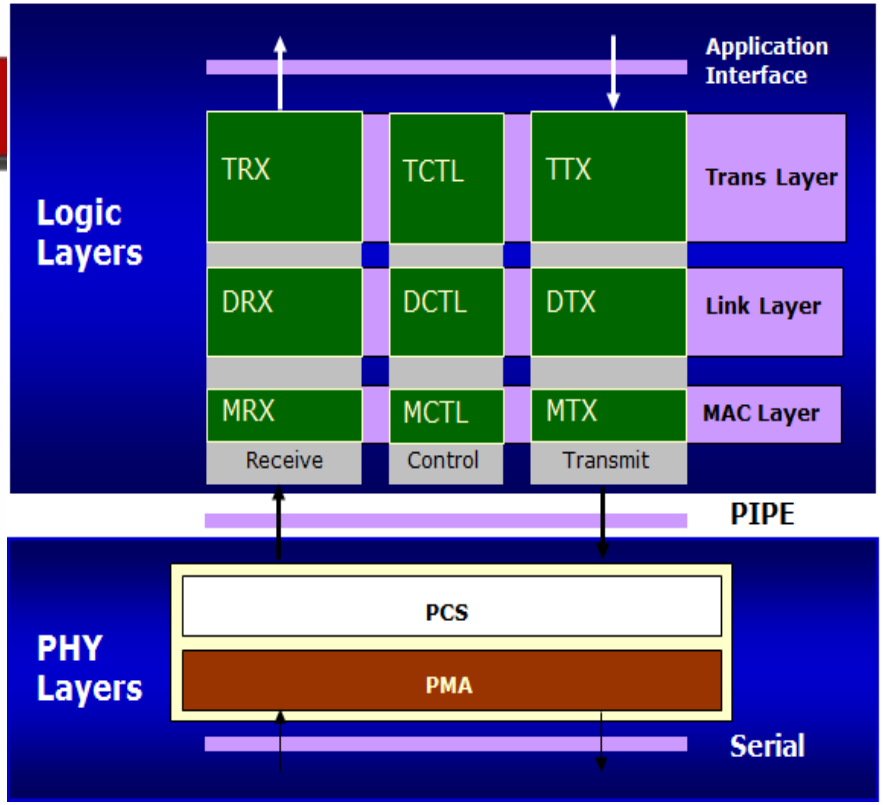
PCI Express Controller (GPEX)

Company Overview
NVMe SSDC Subsystem
NVMe Features & Configurability
GPEX
Summary

PCI Express (GPEX)

- ✓ **Highly Configurable**
- ✓ **Technology Independent**
- ✓ **System Validated**



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Gen1, Gen2 & Gen3
Endpoint
Root Complex
Dual mode
Switch port
Switch
OCB Solution

x1 to x32
180nm to 28nm

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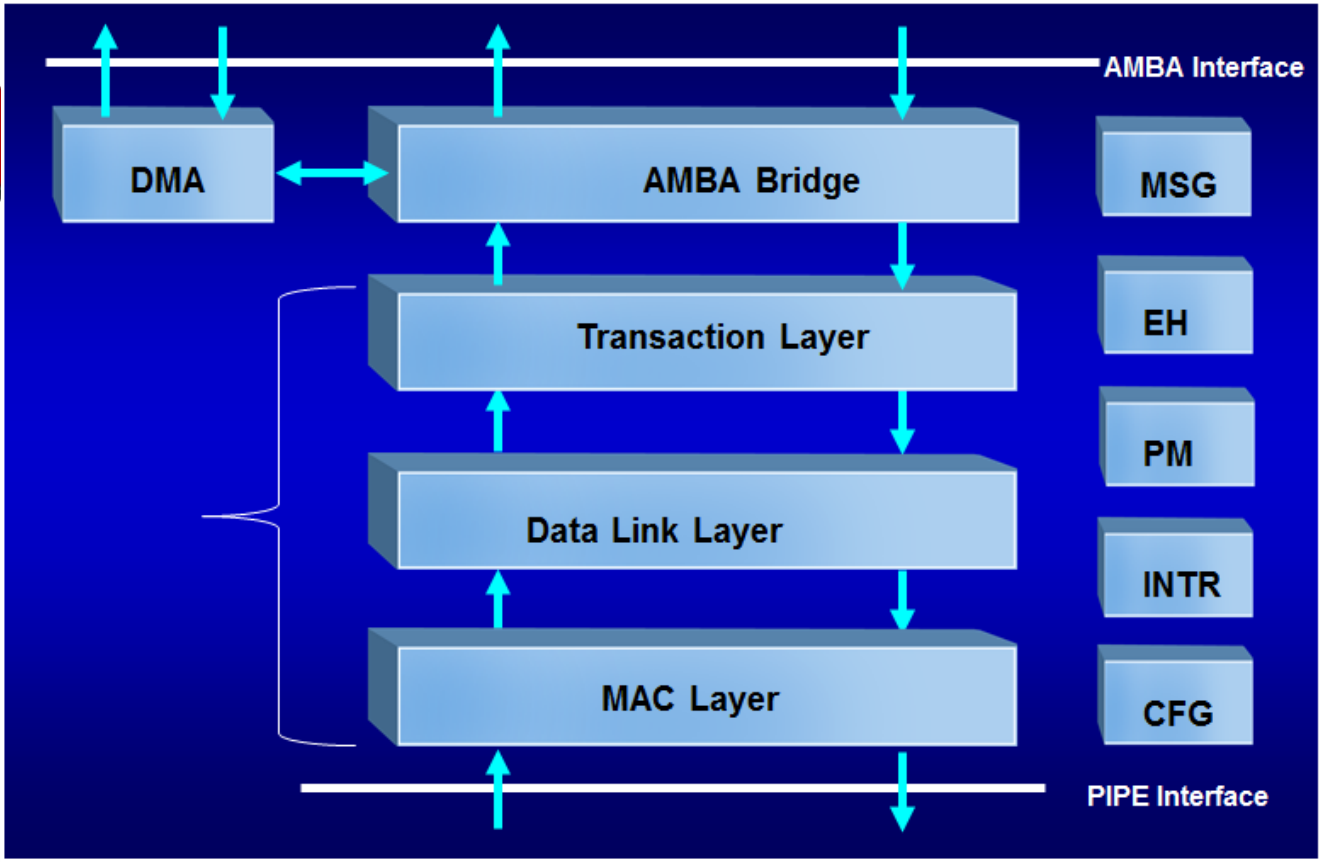
Company Overview
NVMe SSDC Subsystem
NVMe Features & Configurability
GPEX
Summary

PCIe-AMBA Bridge

- ✓ Highly Configurable
- ✓ Technology Independent
- ✓ System Validated

PCI EXPRESS™



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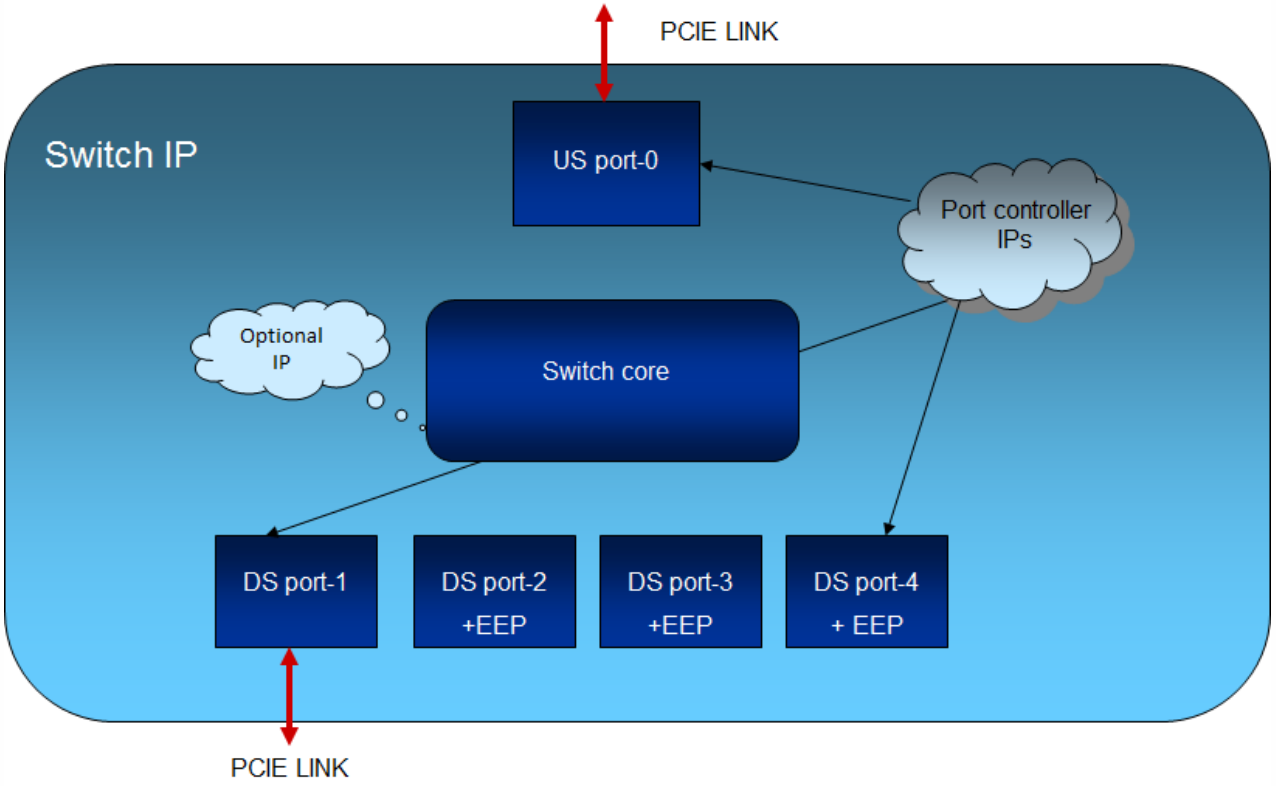
Transparent PCIe Switch

- ✓ Highly Configurable
- ✓ Technology Independent
- ✓ System Validated



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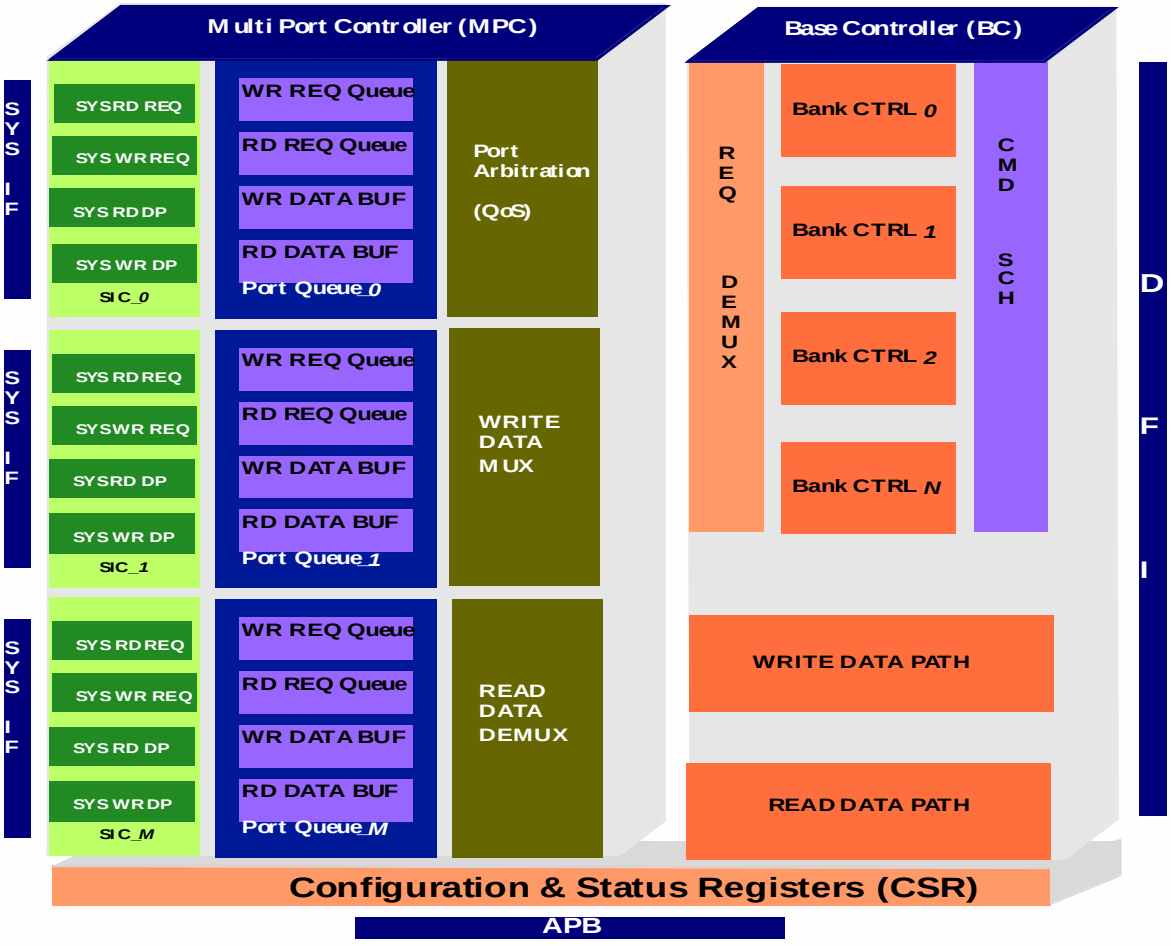
DDR3/4 Memory Controller

Company Overview
NVMe SSDC Subsystem
NVMe Features & Configurability
DDR3/4 Controller
Summary

DDR3/4 Memory Controller

- ✓ Highly Configurable
- ✓ Technology Independent



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Company Overview
NVMe SSDC Subsystem
NVMe Features & Configurability
DDR3/4 Controller
Summary

- ✓ **Highly Configurable**
- ✓ **Technology Independent**

DDR3/4 Controller Features

- Compliant with AMBA 3
- Compliant with DFI 2.1 Interface
- Supports QoS through various arbitration schemes
- Configurable and programmable address mapping
- Supports up to 4 ranks
- Supports following BC Clock to PHY Clock ratio
  - 1:1 (Full-rate Mode)
  - 1:2 (Half-rate Mode)
  - 1:4 (Quarter rate Mode)
- Supports Burst Length 4, 8, 16
- Supports Active/Precharge Power down
- Supports software and hardware driven Self Refresh entry and exit
- Supports Auto-refresh and per-bank refresh
- Supports ECC Checking and Correction (optional)
- Supports automated memory initialization
- Supports ZQ Calibration
- Targets FPGA, Structured ASIC and Standard Cell technologies

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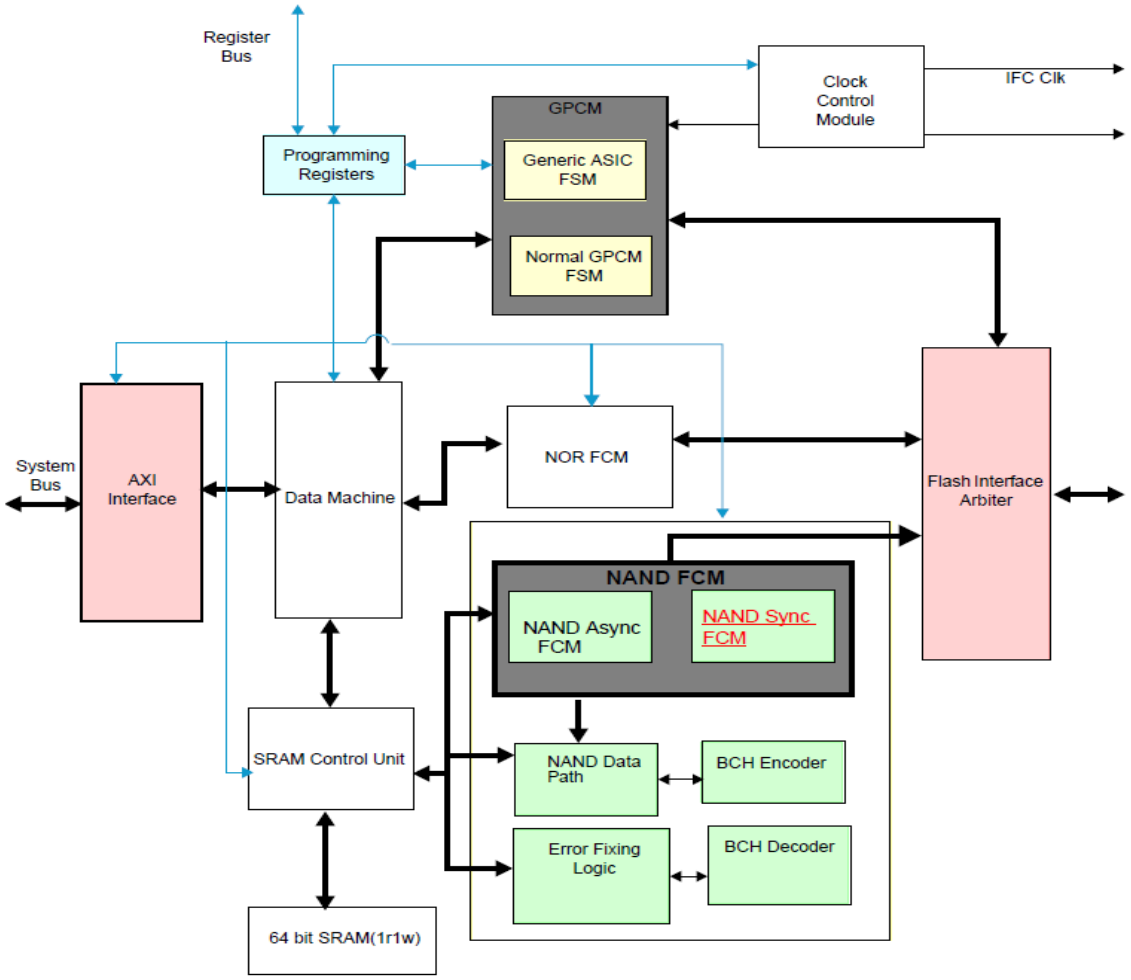
Integrated Flash Controller

Company Overview
NVMe SSDC Subsystem
NVMe Features & Configurability
IFC
Summary

Integrated Flash Controller

- ✓ **Highly Configurable**
- ✓ **Technology Independent**

Silicon Proven



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Company Overview
NVMe SSDC Subsystem
NVMe Features & Configurability
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Summary

Integrated Flash Controller Features

- Flash Controller with eight chip selects
- AXI V1.0 Slave Interface
- Separate Bus Interface for register access
- Support for error and debug registers
- Supports NAND, NOR and GPCM (SRAM and ROM) devices
- Support memory banks of size 64KByte to 4 GBytes
- Write protection capability (only for NAND and NOR)
- Provision of Software Reset
- NAND Flash Features
  - x8/ x16 NAND Flash Interface
  - Support for ONFI-2.2 Asynchronous interface (8/16 Bit)/Source Synchronous interface (8 bit) and mandatory commands.
  - BCH code for 4 bit & 8 bit Error correction per sector of 512 bytes (Using GF-2^13 Galois field) and 24 & 40 bit ECC per sector of 1K bytes (Using GF- 2^14 Galois field)
  - Optional ECC generation and checking
  - Flexible timing control to allow interfacing with proprietary NAND devices
  - SLC and MLC Flash devices support with configurable page sizes of up to 8KB

✓ Highly Configurable
✓ Technology Independent

Silicon Proven

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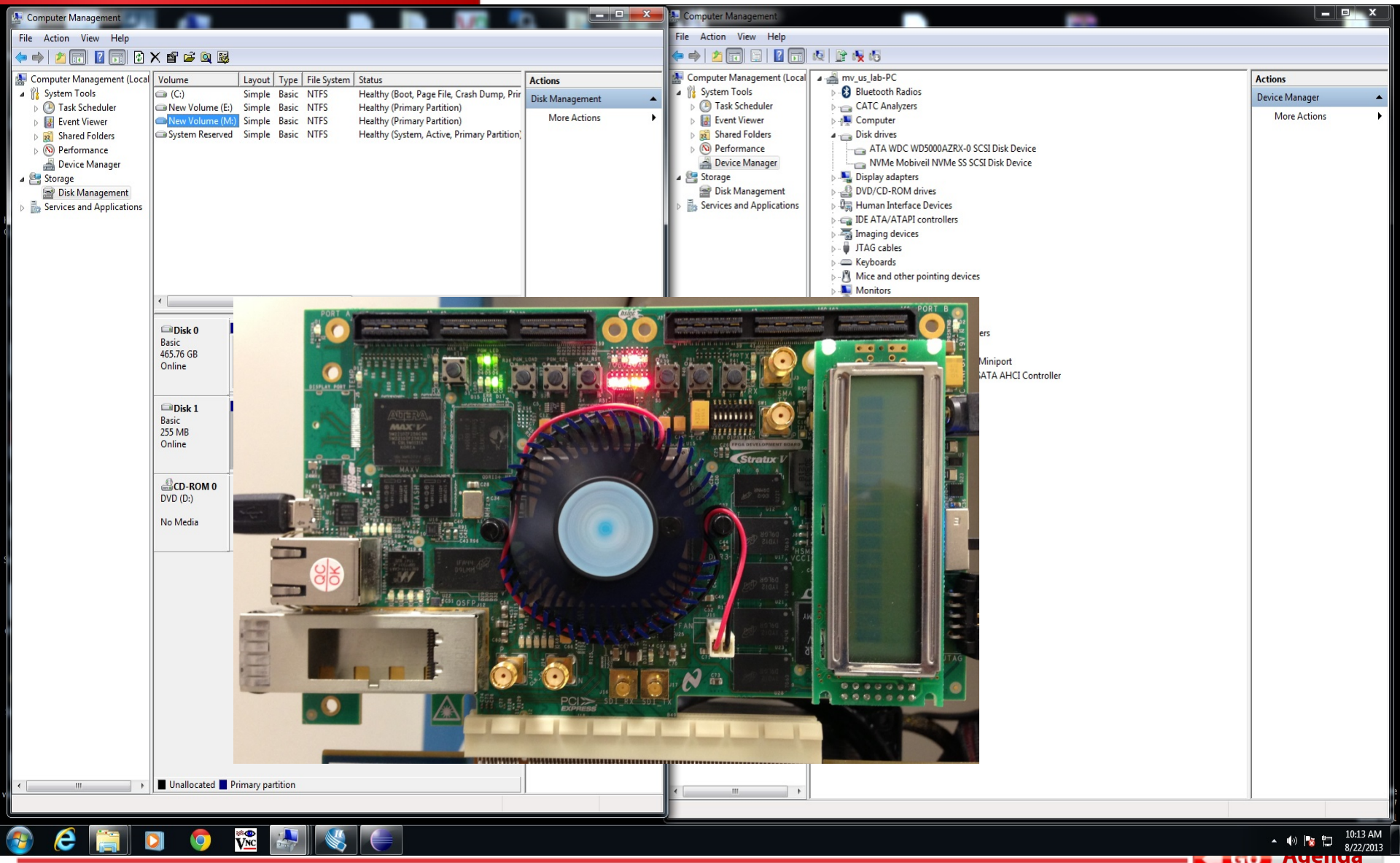
PCIe NVMe SSDC Platform



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Company Overview
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Mobiveil NVMe SSDC Platform

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Company Overview
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Summary

Mobiveil at FMS 2014

- Bronze sponsor at FMS 2014- Booth # 721
- Announcement with Altera and Everspin on MRAM based solution
- Announcement with eASIC on making Mobiveil NVM Express IP available in their devices.
- To know more about Mobiveil NVM Express IP and SSDC Platform
  - You can visit Mobiveil booth (#721) for additional information
  - Visit Altera or Mobiveil booth for additional information on Everspin MRAM based solution
  - Speak to Silicon Motion booth to understand how they are accelerating their SOC design using Mobiveil NVM Express IP
  - Visit Mobiveil or Xilinx booth to know more about implementing UNEX in Xilinx platform

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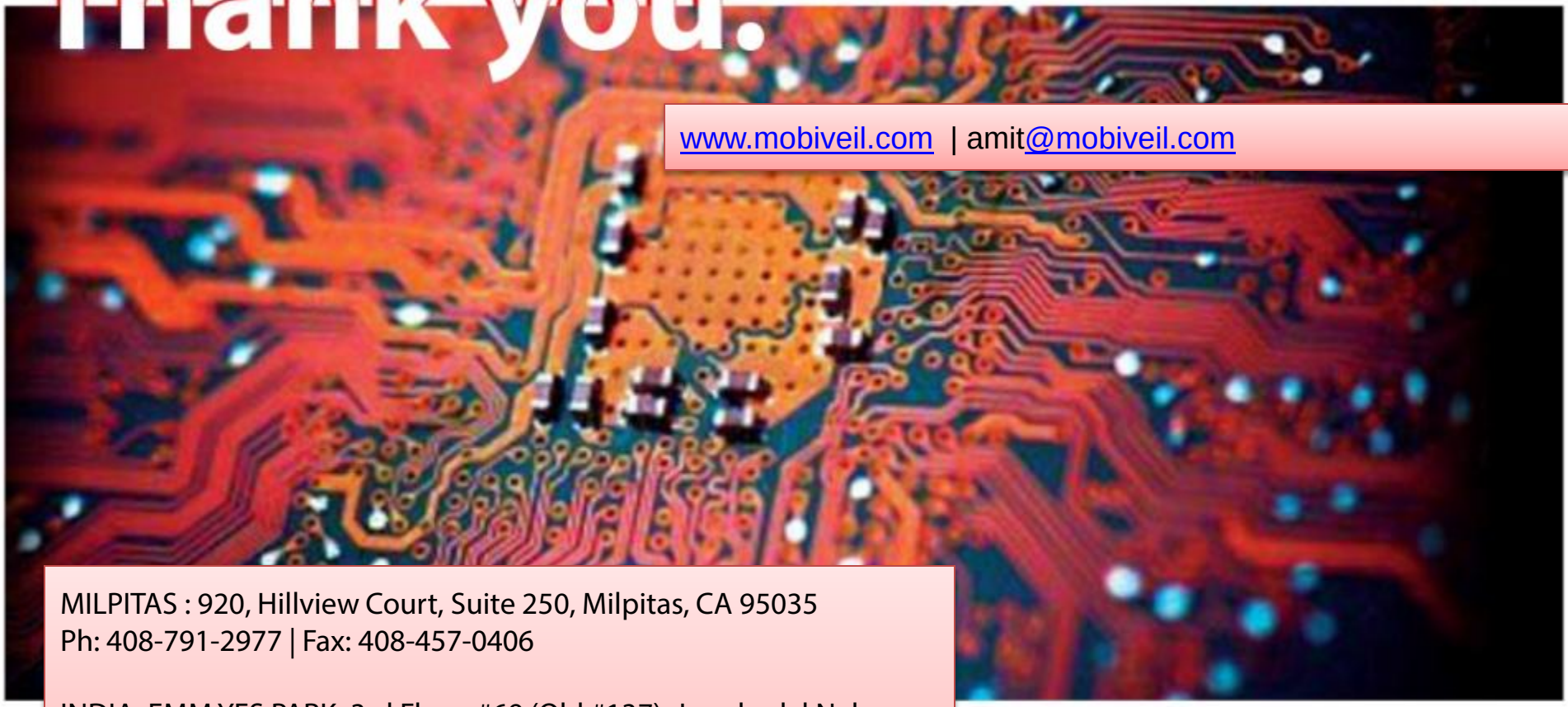
Thank you.



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