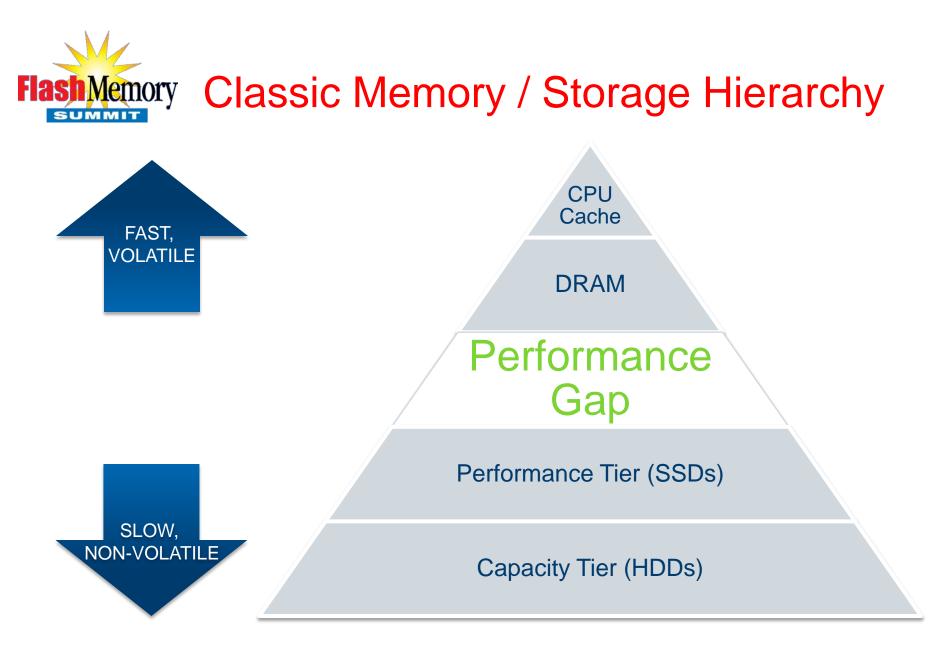


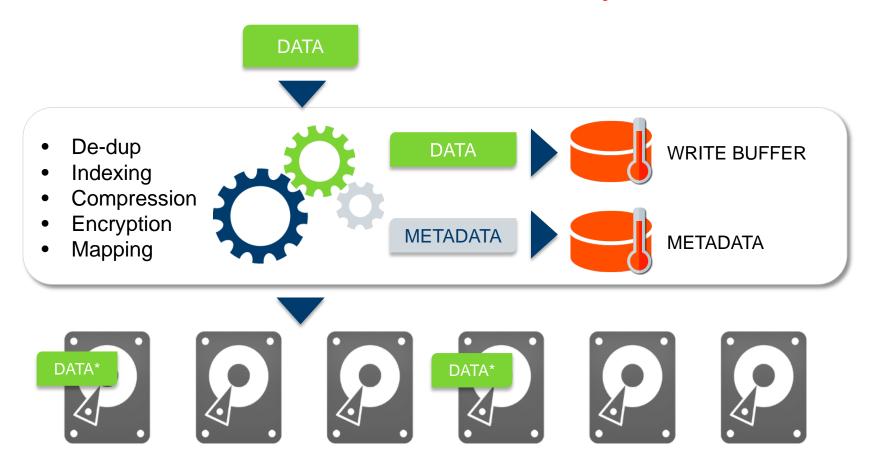
PCIe Storage Beyond SSDs

Fabian Trumper NVM Solutions Group PMC-Sierra

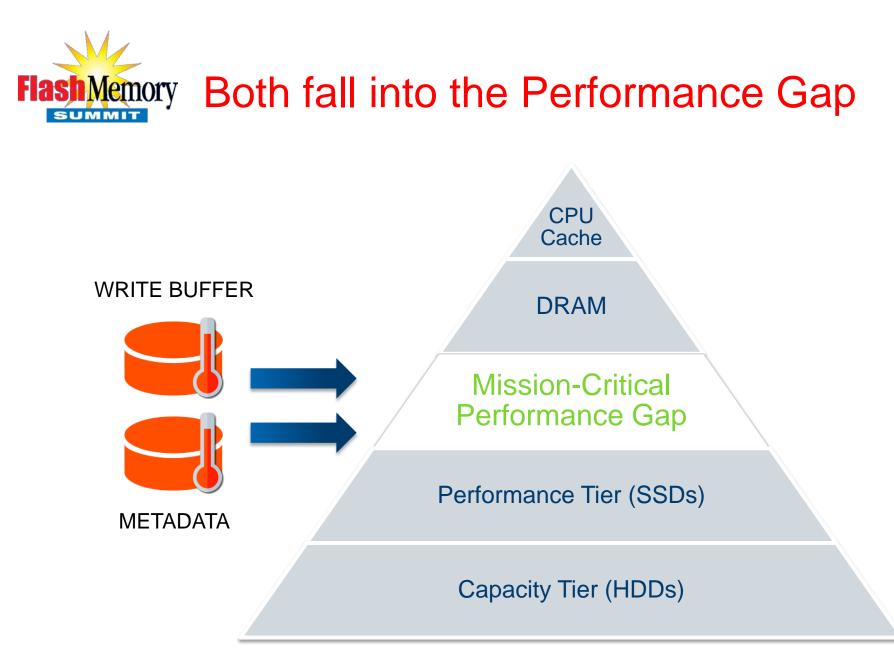




Some system hot spots don't fit well within that hierarchy



Hot Spot I/Os >= \sum (all I/O in the System)

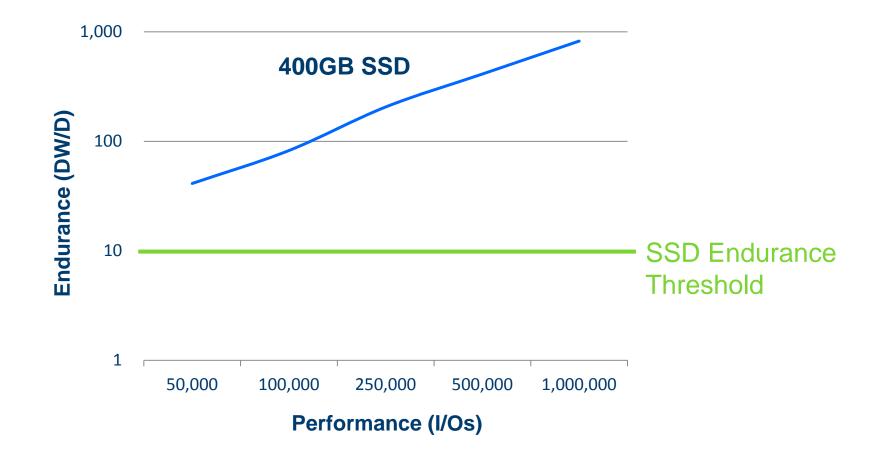


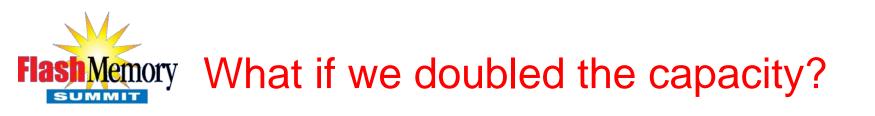


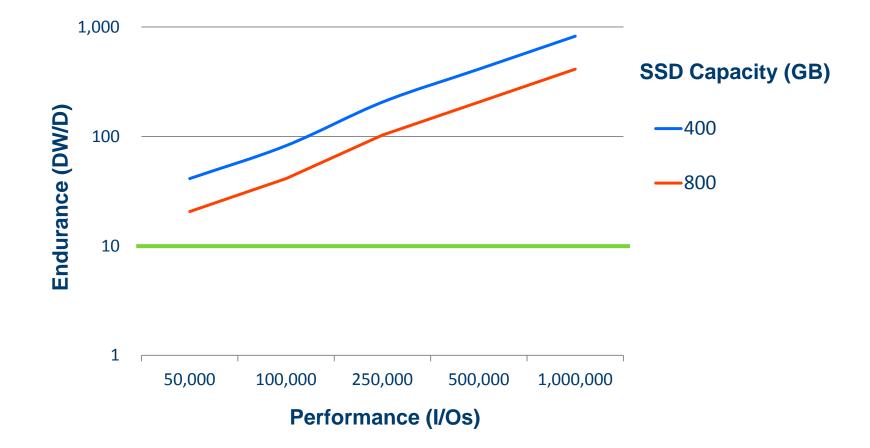
Flash Memory Two Mission Critical Data Sets

Requirements	WRITE BUFFER	METADATA 🔴
Transaction Size	Variable / Small	Fixed
Bandwidth	Low/Moderate	Very High
Response Time	Very Low	Very Low
Non Volatile	Yes	Yes
Write Endurance	Very High	Very High
Multi-Port Access	Preferably	Preferably
Mission Critical (Fail Safe)	Yes	Yes

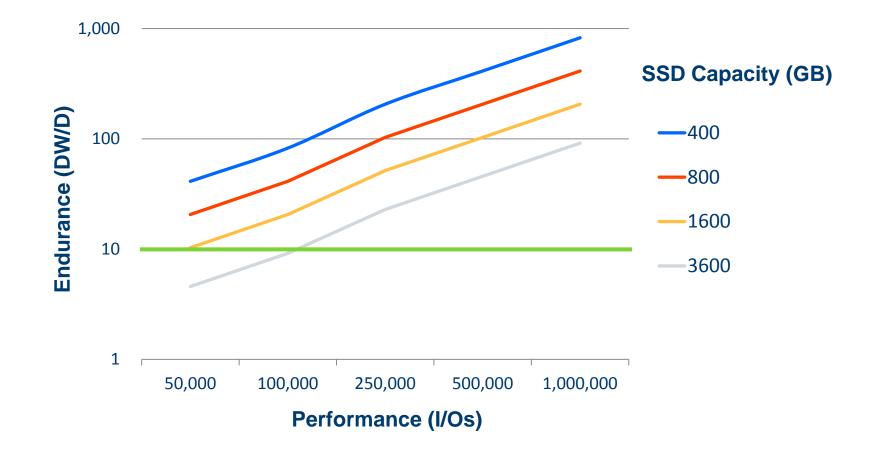


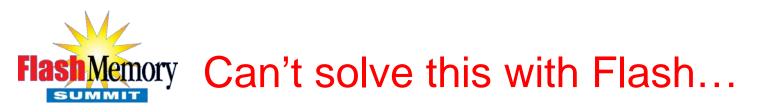


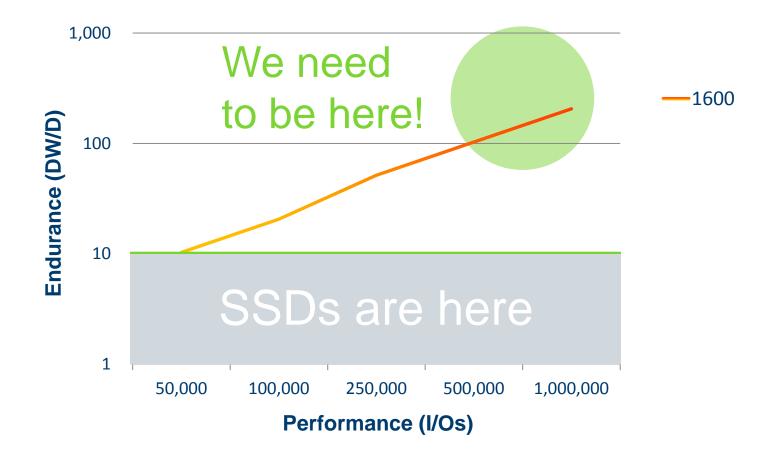














- DRAM is susceptible to power failures
- To protect mission critical information,

either -

Use UPS or BBU ► maintenance nightmare

Closed due to Power Outage!

Log everything to Storage
 Complexity,

Performance and Endurance trade-offs



What about PCM? RRAM? MRAM? We've been waiting for years...







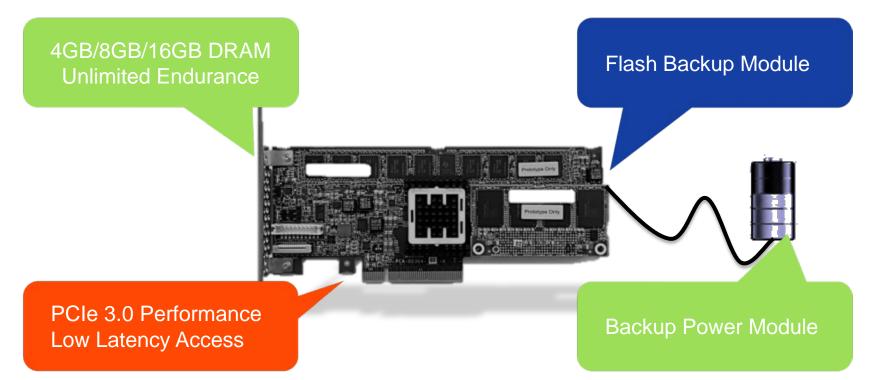


Requirements		Solid State Drive	PCI-Express Memory Mapped Storage
DMA Initiator	Νο	Νο	Yes
Memory Addressable	Yes	Νο	Yes
Variable Size Objects	Yes	Νο	Yes
Write Endurance	Yes	Νο	Yes
Multi-Port Access	Νο	Yes	Yes
Persistent	Νο	Yes	Yes

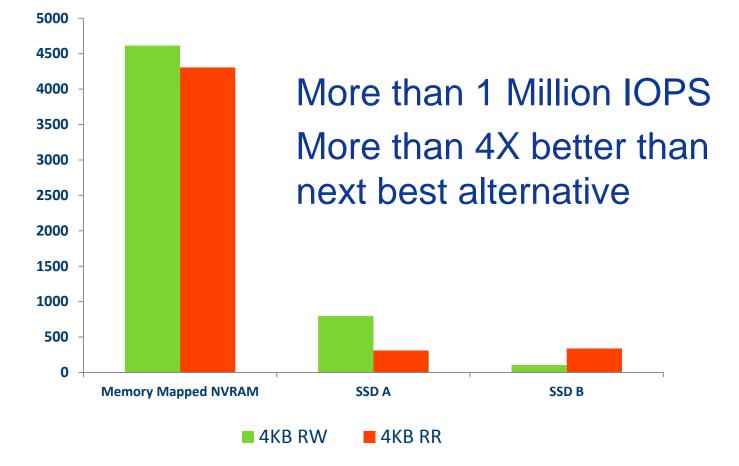


Mt Ramon Project – Hybrid Memory Card

- So we went ahead and built it ③
- 16GB NV-RAM
- NVMe and Direct Memory Interface Access Modes





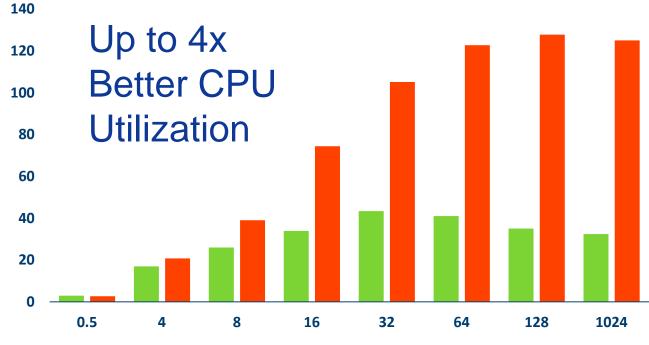


Sustained and Symmetrical Performance



Memory And what about CPU utilization?

MB/s per 1% Utilization

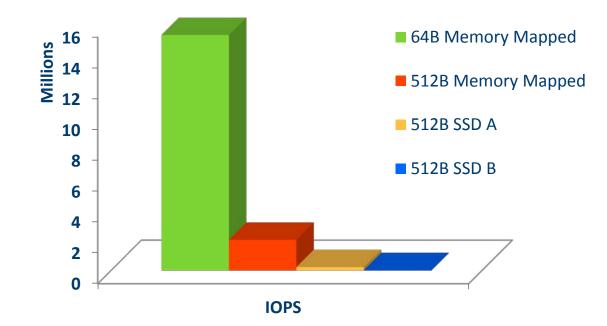


CPU Load/Store PCIe DMA

	HW	Details	
	CPU	15-3470	
	DDR	1333MHz	
	Frq	3.2Ghz	
	PCI	X8 Gen3	
	# of cores	4	
N			



15 Million Random Write IOPS for 64B Transactions



- Memory Mapped Interfaces provides higher IOPS for small write transactions
- Ideal for in-place updates of metadata and database records



- Enable the Industry to support Memory-Mapped Storage by working through standards bodies:
 - NVMexpress



- SNIA NVM Programming TWG
- Enable Applications and Operating Systems ISV
 - Adopt methods and APIs to recognize and take advantage of memory-mapped devices



Thank You! PMC

See us in booth # 416 for a live demo

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