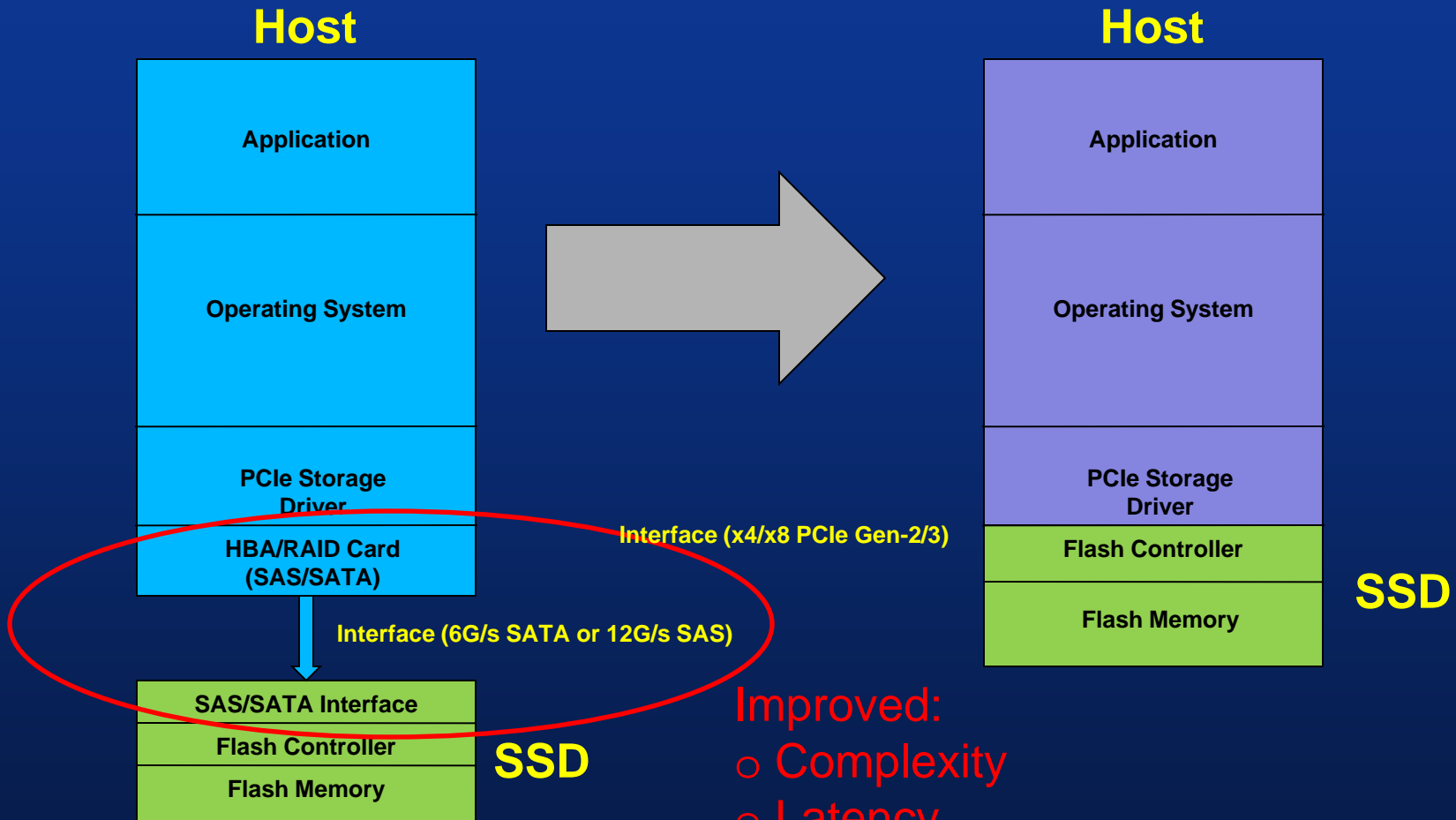




Power Management PCIe/NVMe Flash Cards

Presenter: Bob Weisickle
CEO/Founder: OakGate Technology, Inc.

NVMe Premise/Challenge



- Improved:
- Complexity
 - Latency
 - Performance
 - Reliability

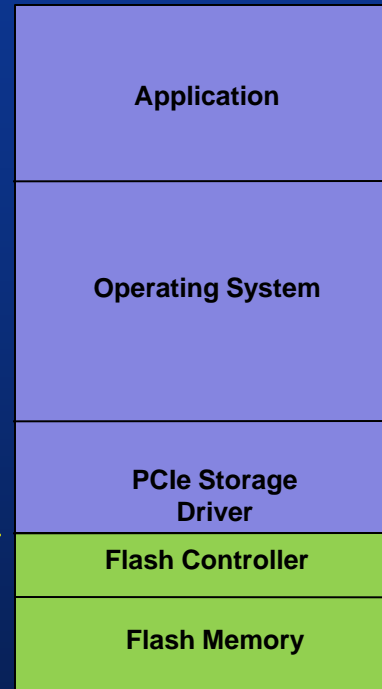
Performance/Validation Challenge

Requirements

- Access to PCIe Registers
- Queue Configuration
- Hot Discovery
- Error/Fault Injection
- Power Loss/Recovery
- PCIe Resets
- NVMe Performance/Power



Host



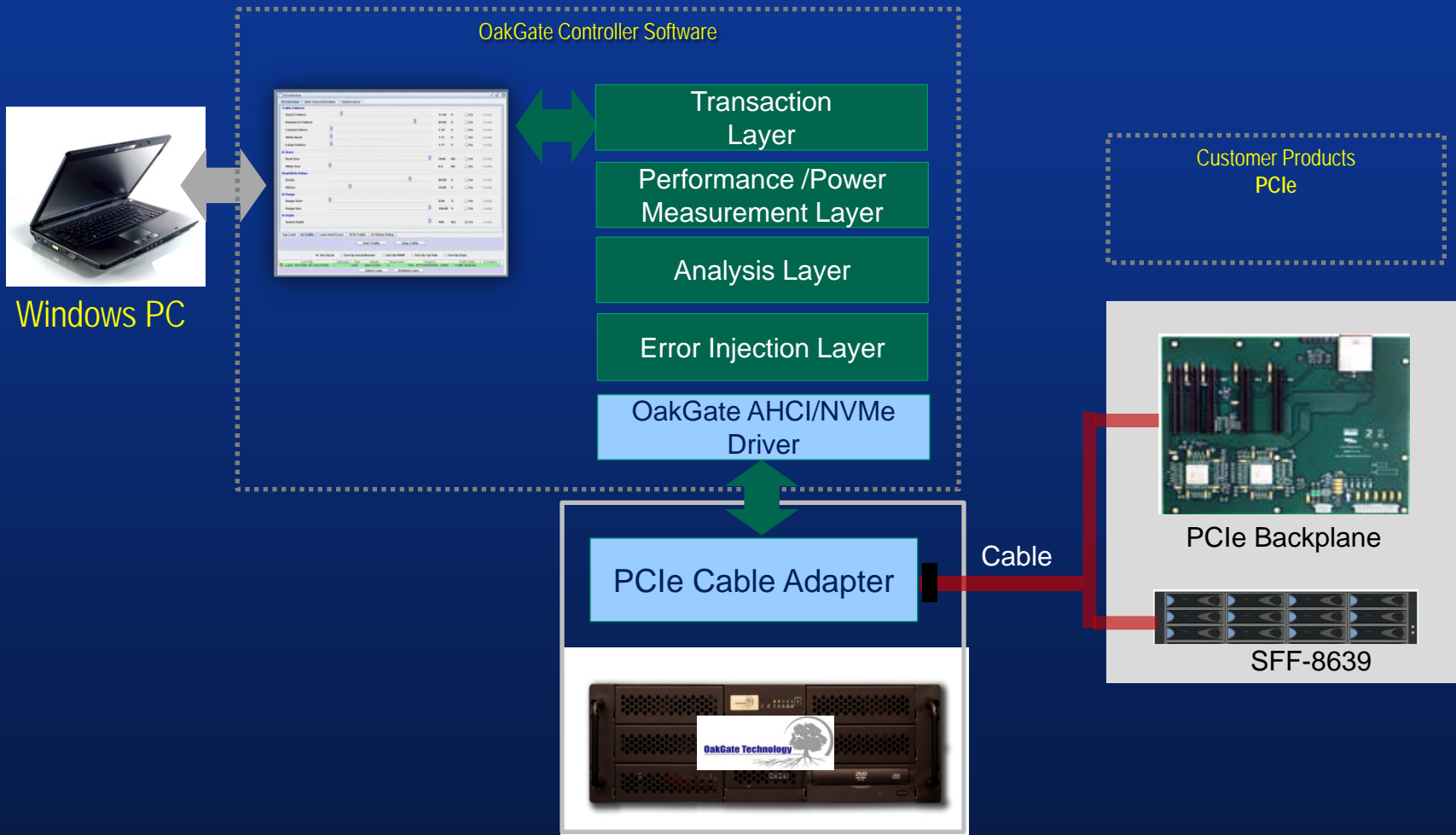
Challenges

- Closely coupled to host
- Access via host driver
- Shared environment
- Limited Hot Plug/Discovery
- Power Measurement

PCIe Interface

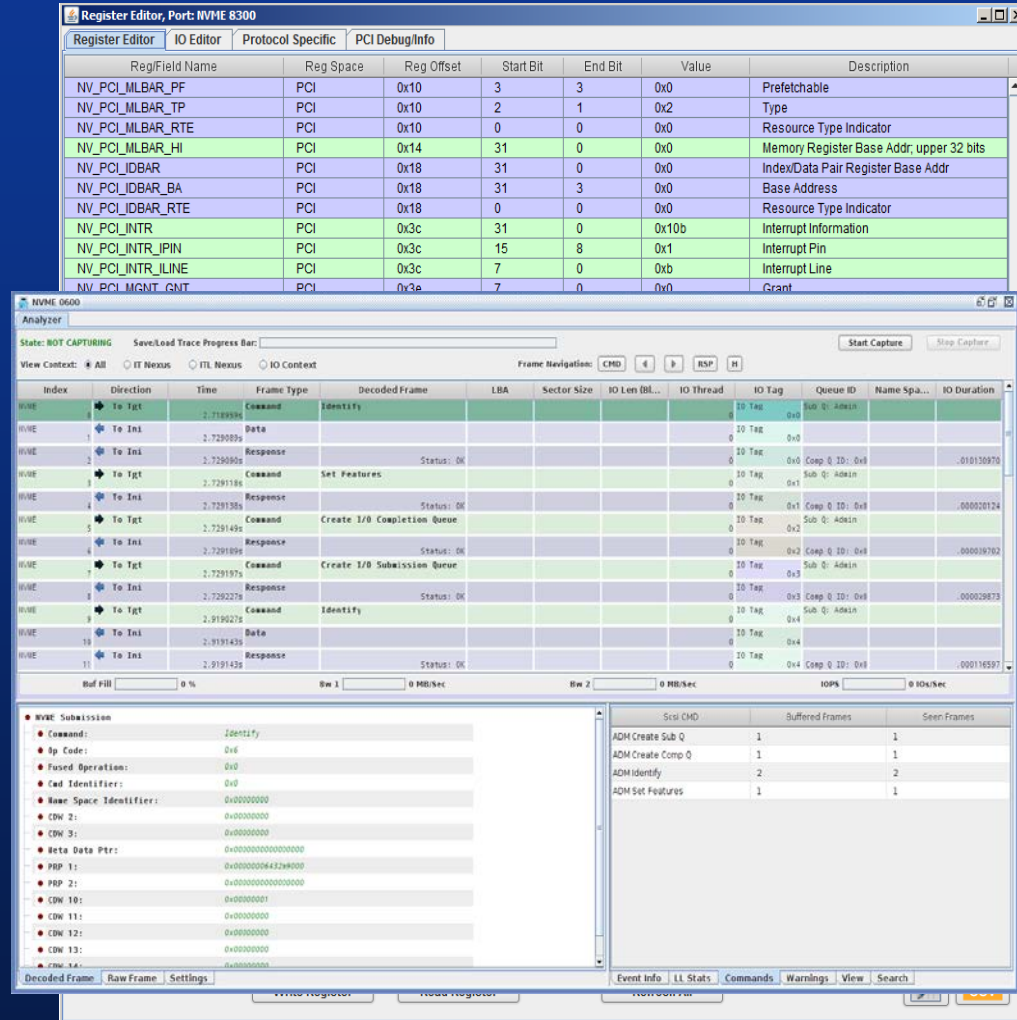
SSD

Performance/Validation Environment



Base Level PCIe Validation

- Register Access
 - Bit Level verification
 - Error Injection (Bit/Register Level)
 - Base Address Visibility
 - Get/Set Features
- Command Analyzer
 - Posted commands w/ responses
 - Visibility to errors



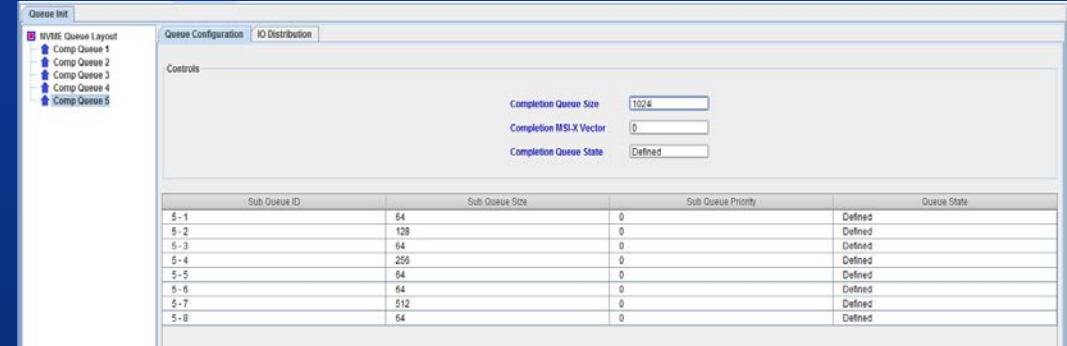
The image shows two software windows. The top window is the 'Register Editor, Port: NVME 8300'. It displays a table of registers with columns for Reg/Field Name, Reg Space, Reg Offset, Start Bit, End Bit, Value, and Description.

Reg/Field Name	Reg Space	Reg Offset	Start Bit	End Bit	Value	Description
NV_PCI_MLBAR_PF	PCI	0x10	3	3	0x0	Prefetchable
NV_PCI_MLBAR_TP	PCI	0x10	2	1	0x2	Type
NV_PCI_MLBAR_RTE	PCI	0x10	0	0	0x0	Resource Type Indicator
NV_PCI_MLBAR_HI	PCI	0x14	31	0	0x0	Memory Register Base Addr: upper 32 bits
NV_PCI_IDBAR	PCI	0x18	31	0	0x0	Index/Data Pair Register Base Addr
NV_PCI_IDBAR_BA	PCI	0x18	31	3	0x0	Base Address
NV_PCI_IDBAR_RTE	PCI	0x18	0	0	0x0	Resource Type Indicator
NV_PCI_INTR	PCI	0x3c	31	0	0x10b	Interrupt Information
NV_PCI_INTR_IPIN	PCI	0x3c	15	8	0x1	Interrupt Pin
NV_PCI_INTR_ILINE	PCI	0x3c	7	0	0xb	Interrupt Line
NV_PCI_MGMT_GNT	PCI	0x3e	7	0	0x0	Grant

The bottom window is the 'NVM Express Analyzer'. It shows a capture of NVMe commands and responses. The main table lists frames with columns for Index, Direction, Time, Frame Type, Decoded Frame, LBA, Sector Size, IO Len (B/L), IO Thread, IO Tag, Queue ID, Name Spac..., and IO Duration. Below the table, there are performance metrics like Buf Fill, BW 1, BW 2, and IOPS. A detailed view of an NVMe Submission command is shown at the bottom, including fields like Command, Op Code, Fused Operation, Cid Identifier, Name Space Identifier, and various Cdw fields.

Queue Configuration

- Multiple Sub/Comp Queues
- Definable Sub/Comp Queue Size
- Sub Queue IO Loading
- Multi-CPU Queue Distribution
- Definable Interrupt Support
 - MSI-X
 - MSI
 - Line

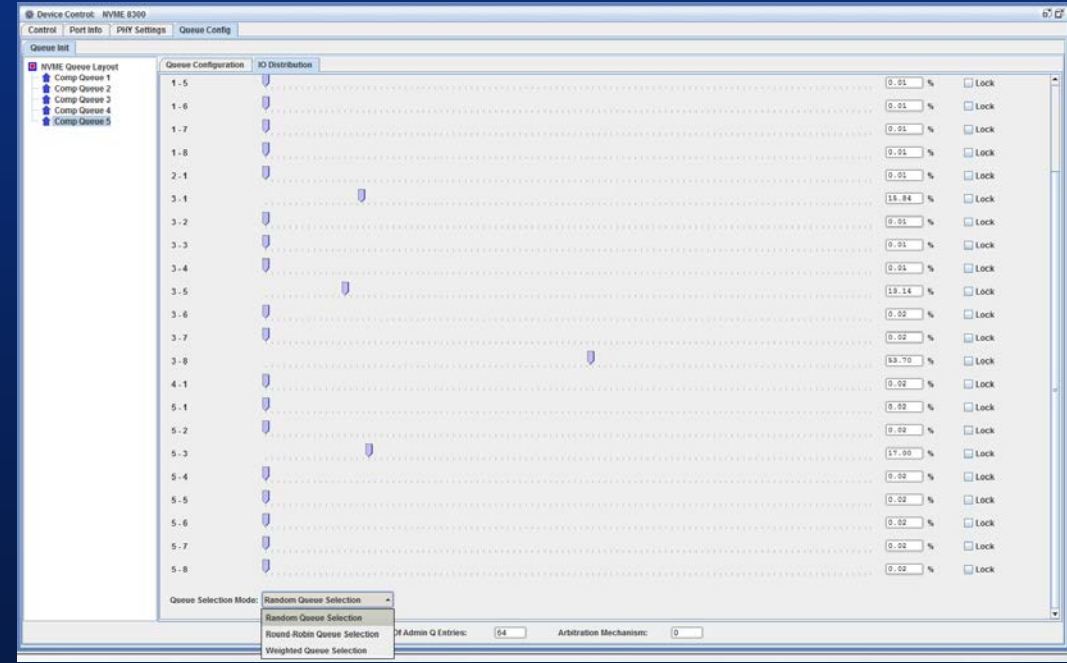


Queue Configuration - IO Distribution

Controls

Completion Queue Size: 1024
 Completion MSI-X Vector: 0
 Completion Queue State: Defined

Sub Queue ID	Sub Queue Size	Sub Queue Priority	Queue State
5-1	64	0	Defined
5-2	128	0	Defined
5-3	64	0	Defined
5-4	256	0	Defined
5-5	64	0	Defined
5-6	64	0	Defined
5-7	512	0	Defined
5-8	64	0	Defined



Device Control - NVME 8200 Queue Config

Queue Configuration - IO Distribution

Sub Queue ID	Sub Queue Size	Sub Queue Priority	Queue State	Completion Rate	Lock
1-5	64	0	Defined	0.01 %	<input type="checkbox"/>
1-6	128	0	Defined	0.01 %	<input type="checkbox"/>
1-7	64	0	Defined	0.01 %	<input type="checkbox"/>
1-8	256	0	Defined	0.01 %	<input type="checkbox"/>
2-1	64	0	Defined	0.01 %	<input type="checkbox"/>
3-1	64	0	Defined	15.84 %	<input type="checkbox"/>
3-2	128	0	Defined	0.01 %	<input type="checkbox"/>
3-3	64	0	Defined	0.01 %	<input type="checkbox"/>
3-4	256	0	Defined	0.01 %	<input type="checkbox"/>
3-5	64	0	Defined	15.14 %	<input type="checkbox"/>
3-6	64	0	Defined	0.02 %	<input type="checkbox"/>
3-7	64	0	Defined	0.02 %	<input type="checkbox"/>
3-8	64	0	Defined	53.70 %	<input type="checkbox"/>
4-1	64	0	Defined	0.02 %	<input type="checkbox"/>
5-1	64	0	Defined	0.02 %	<input type="checkbox"/>
5-2	128	0	Defined	0.02 %	<input type="checkbox"/>
5-3	64	0	Defined	17.00 %	<input type="checkbox"/>
5-4	64	0	Defined	0.02 %	<input type="checkbox"/>
5-5	64	0	Defined	0.02 %	<input type="checkbox"/>
5-6	64	0	Defined	0.02 %	<input type="checkbox"/>
5-7	64	0	Defined	0.02 %	<input type="checkbox"/>
5-8	64	0	Defined	0.02 %	<input type="checkbox"/>

Queue Selection Mode: Random Queue Selection

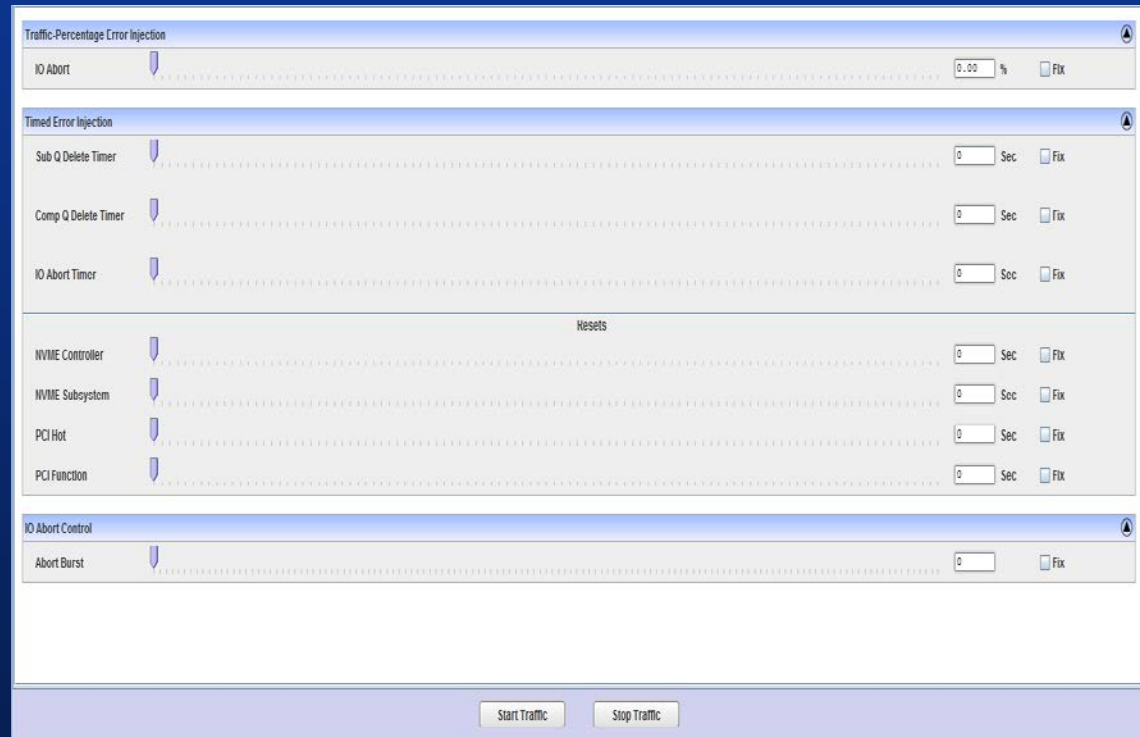
Admin Q Entries: 04 Arbitration Mechanism: 0

Hot Power Loss/Recovery

- Host Independent Power Control
 - Ability to control power to each device
 - Measure power of each device
- Surprise Power Loss/Recovery
 - Detection of device being powered off
 - Auto re-discovery and drive state verification
 - No Host reboot required
- Auto Queue Management
 - Re-instantiate all Queues
 - Clean up of outstanding commands
- Auto Traffic Control
 - Continue with traffic workload
 - Check for data corruption

Resets/Queues/Abort

- IO Aborts
- PCIe Resets
 - Function Resets
 - Hot Resets
 - Controller
 - Subsystem
- Auto Re-Discovery
- Queue Management & Recovery



Data Retention/Corruption

- Validate Pre-existing Data
- Validate 'Acknowledged' Writes
- Evaluate 'Outstanding' Writes
 - Verify Atomic Write Functionality
 - Single LBA corruption
 - Visibility to Partial Writes

Validate Data Integrity

Validate Data Integrity

Validate Written Data On Link Up

Validate LBA Atomicity

Validate Outstanding IOs

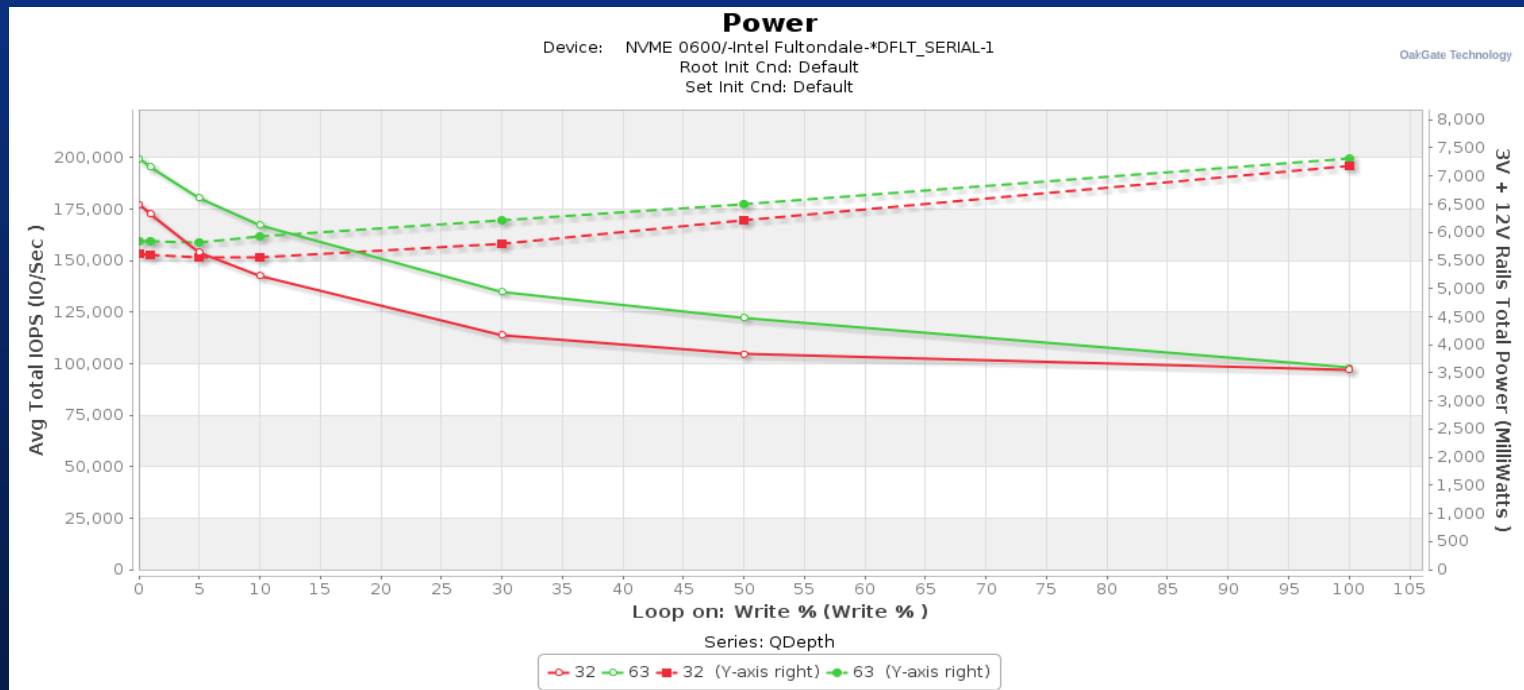
Clear All Data Validation Tables in System

Nr Of Last Writes To Validate:

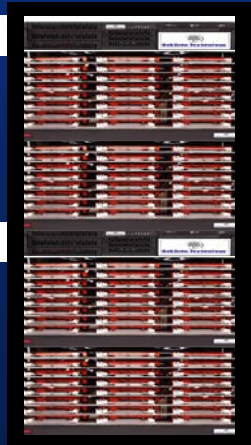
Warning: "Validate LBA Atomicity" and "Validate Outstanding IOs" should only be enabled to check IO's that have NOT been acknowledged. Enabling them could generate errors that may be proper behavior for the target.

Power Assessment

- Real-time Power Measurement
 - Power vs Performance
 - Power vs Workload



- Improved Space Utilization
- Better Power/DUT
- Enhanced Management



SAS/SATA
44U Rack
96 SATA/SFF-8639 SSDs
OakGate



PCIe
44U Rack
256 PCIe SSDs
OakGate



Thermal
10.5x5.5 Box
1024 SATA SSDs
512 PCIe x4 SSDs
OakGate/Tanisys

- NVMe has momentum in the Market
 - Products exists from a several major suppliers
- Test/Validation Tools exist
 - With Power Control and Power Measurement
 - Detailed PCIe Register/Queue access
- PCIe Ecosystem is evolving
 - SFF-8639, M.2 etc becoming available
 - Dual Port Support
- NVMe Spec is evolving rapidly
 - Requires Validation Tools that stay current



Thank You

Questions/Follow-up:
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www.oakgatetech.com