Taking Full Advantage of Ultra High Speed SD Cards

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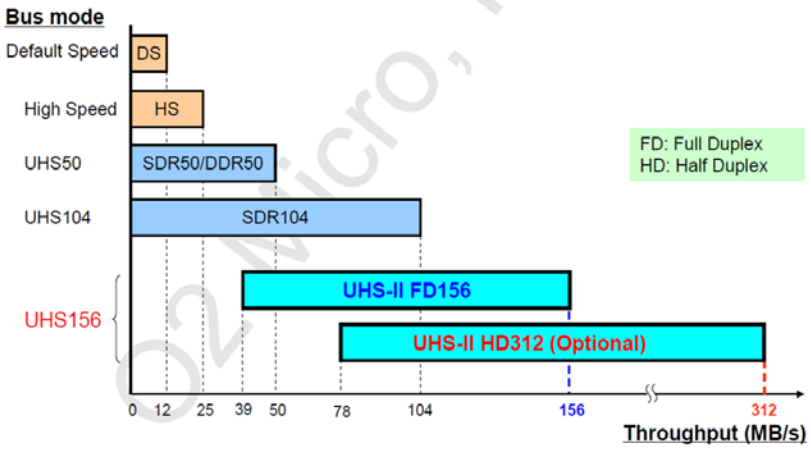
What is The Advantage of UHS-II?

- Faster Data Transfer
  - Up to 312MB/s
- Easy Implementation
  - Only 3 Differential Pairs
- Low EMI
  - Differential Interface
- Low Power
  - Low-Swing Signaling
  - Low Power Mode

What is The Advantage of UHS-II?

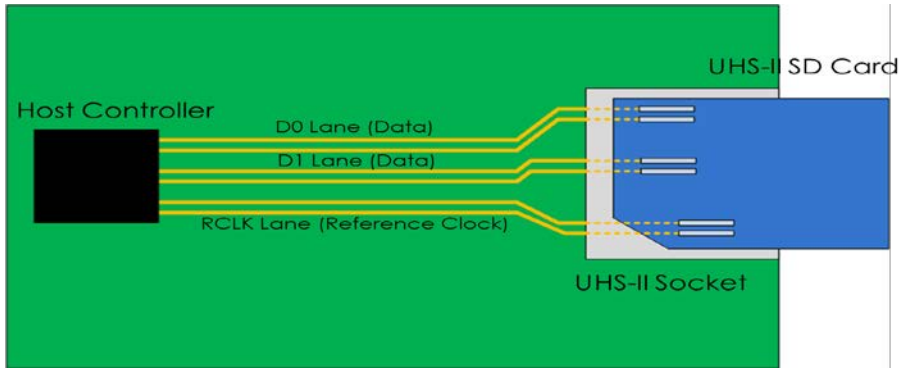
	UHS-I	UHS-II
Interface Data Rate	208MHz (4bits Data and Clock)	1.56Gbps (2 lanes Bi-Directional Data and Low Frequency RCLK)
Clock Scheme	Source Synchronous parallel Interface	CDR Based Serial Interface
Termination	No	Yes
Signal Swing	1.8V (3.3V Legacy Mode)	400mV Differential Pk-Pk
Electrical Spec	Setup/Hold, Tr/Tf etc	Jitter Spec, Eye Mask
Connector	Treat as Mechanical Parts	Treat as Electrical Part (impedance, return loss)
Operational Mode	Various Data Rates and DDR mode Supported	Various Data Rates, Half Duplex Mode, Low Power Mode supported

Bus Speed Mode		Maximum Frequency	Signal Voltage	Bus Maximum Performance	Spec. Version
Default Speed (DS)		25MHz	3.3V	12.5MB/sec	1.01
High Speed (HS)		50MHz	3.3V	25MB/sec	1.10
UHS-I	SDR12	25MHz	1.8V	12.5MB/sec	3.01
	SDR25	50MHz	1.8V	25MB/sec	
	SDR50	100MHz	1.8V	50MB/sec	
	SDR104	208MHz	1.8V	104MB/sec	
	DDR50	50MHz	1.8V	50MB/sec	
UHS-II	FD156	52MHz x30	LVDS	156MB/sec	4.00 4.20
	HD312	52MHz x30	LVDS	312MB/sec	

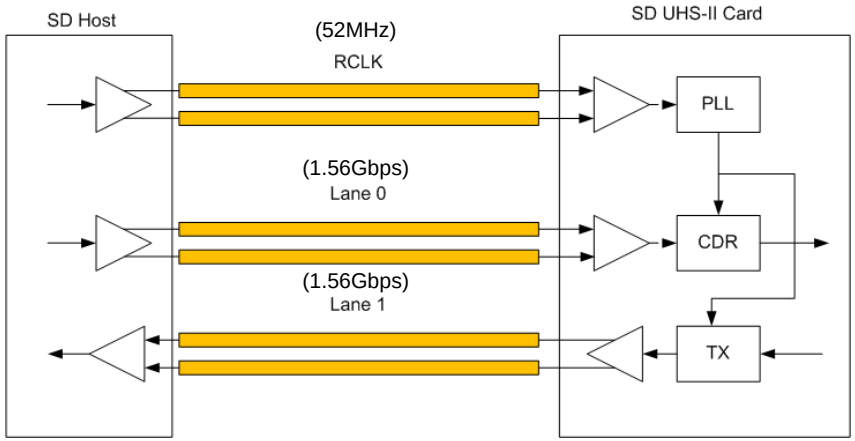


UHS-II Interface Overview

UHS-II Platform

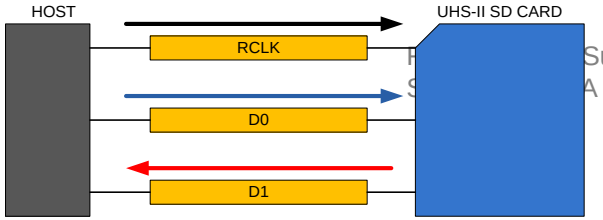


Clocking and Data Transfer

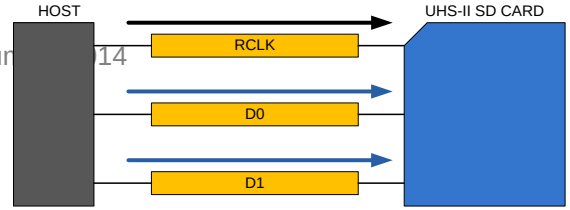


UHS-II Full and Half Duplex

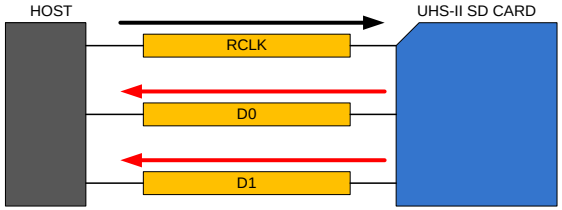
Full Duplex Mode (Upto 156MB/s)



Half Duplex Write Mode (Upto 312MB/s)



Half Duplex Read Mode (Upto 312MB/s)



UHS-II Implementation/Validation

- Key Factors in Successful Design

Channel Design

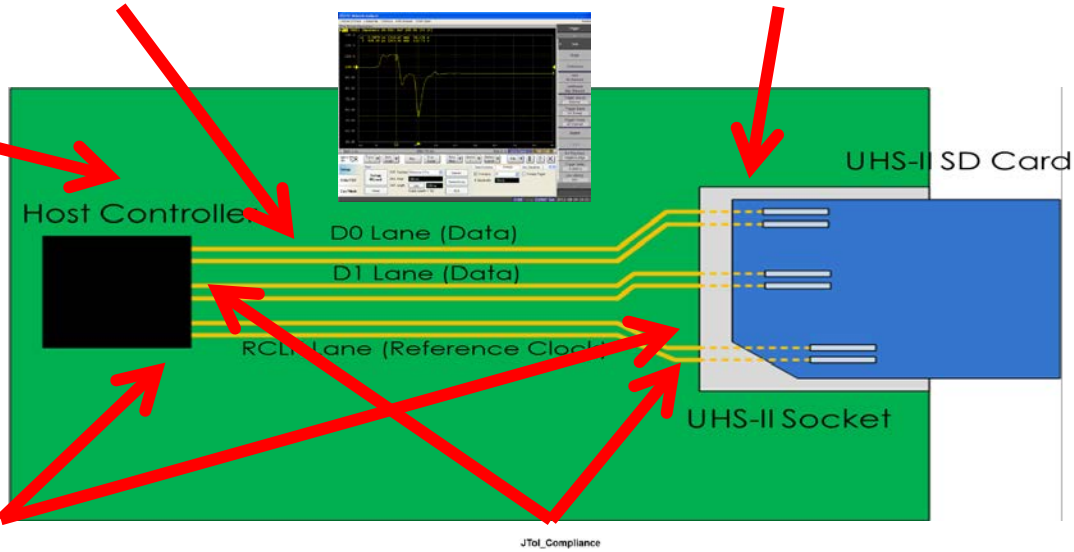
-Loss, Impedance Control, Impedance Discontinuity etc

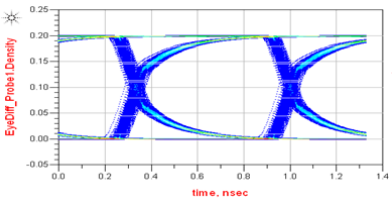
Socket Characteristics

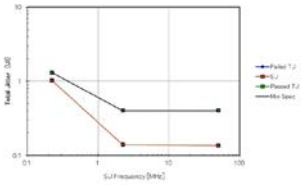
-Loss, Impedance Etc.

Power Supply

-Supply Noise







Transmitter/RCLK Characteristics

-Jitter, Eye Pattern, Return Loss Etc

Receiver Characteristics

-Jitter Tolerance, Return Loss Etc

UHS-II Implementation/Validation

- "UHS-II Test Guidelines" are Released from SDA.
  -Electrical Test Guidelines
  -Protocol Test Guidelines
- "UHS-II Test Tools" are Available from Test Equipment Vendors.

Examples of Test Items

Electrical Test

TG1-5	**3.2.2**	**Host RCLK Tx Specifications (@TP2)** Fill out the results in Table List - 5		
TG1-5-1	3.2.2.1	RCLK Frequency and Data Rate		x
TG1-5-2	3.2.2.2	Differential voltage (+/- Vdiffmin)		x
TG1-5-3	3.2.2.3	Rise/fall time (Tr/Tf)		x
TG1-5-4	3.2.2.4	Common mode voltage (Vcm)		x
TG1-5-5	3.2.2.5	Total jitter (Tj)		x
TG1-5-6	3.2.2.6	Duty cycle (Tckh)		x
TG1-6	**3.2.3**	**Host D0/D1 Tx Specs (@TP2)** Fill out the results in Table List - 6		
TG1-6-1	3.2.3.1	Differential voltage (+/- Vdiffmin)		x
TG1-6-2	3.2.3.2	Eye- pattern and Total Jitter		x
TG1-6-3	3.2.3.3	Rise/fall time (Tr/Tf)		x
TG1-6-4	3.2.3.4	Common mode voltage (Vcm)		x
TG1-6-5	3.2.3.5	EIDL state differential voltage (Vdiff_pd)		x
TG1-6-6	3.2.3.6	EIDL state common mode voltage (Vcm_pd)		x
TG1-6-7	3.2.3.7	Lane 0/1 skew (Skinter)		x

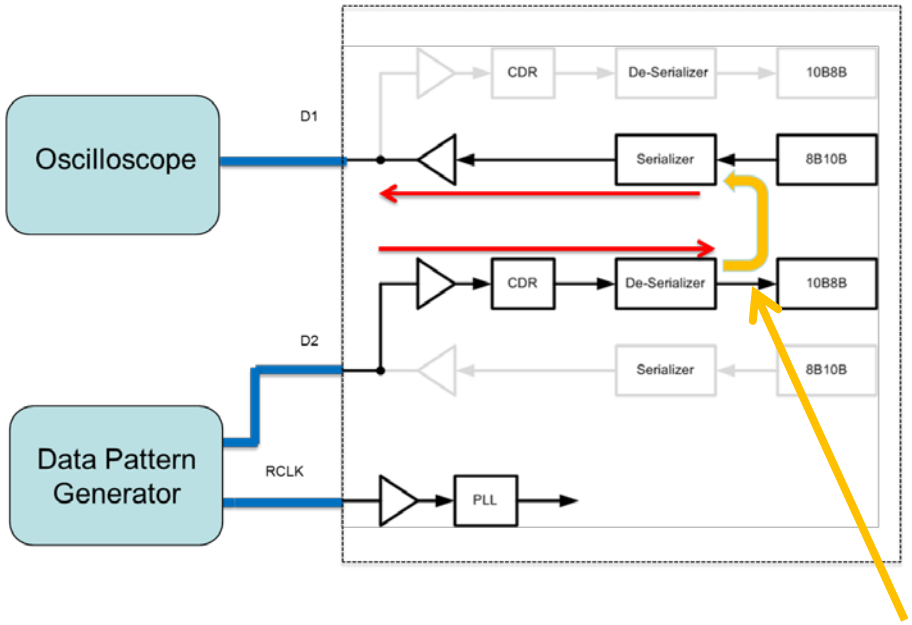
Protocol Test

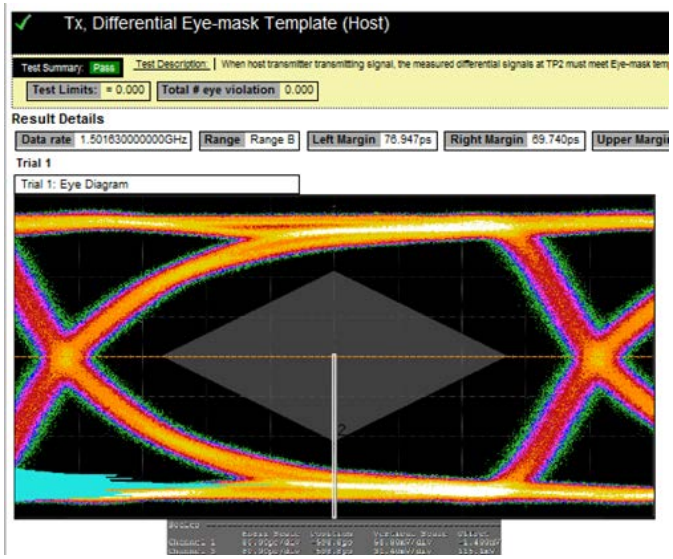
No.	Test Item	Target	
		Host	Device
1-1	**Interface Speed (FD mode):** Device shall fully support Interface speed from 39MB/sec to 156 MB/sec in FD mode.		X
1-2	**Interface Speed (FD mode):** Host shall support at least one Interface speed from 39MB/sec to 78 MB/sec in FD mode.	X	
1-3	**Interface Speed (2L-HD mode):** Device shall fully support Interface speed from 78MB/sec to 312 MB/sec in 2L-HD mode.		X
1-4	**Supporting Legacy SD I/F:** Host shall initialize Legacy SD I/F if UHS-II I/F is not detected.	X	
1-5	**Direction of D0 and D1:** As default, direction of D0 and D1 Lanes are downstream and upstream respectively.	X	X
1-6	**Direction of D0 and D1 on 2L-HD mode write:** Direction of D0 and D1 Lanes are both downstream when Host sends data to Device.	X	X
1-7	**Direction of D0 and D1 on 2L-HD mode read:** Direction of D0 and D1 Lanes are both upstream when Host receives data from Device.	X	X
1-8	**RCLK:** RCLK shall be distributed individually to removable Devices. In case of Ring connection, RCLK is distributed by either point to point method (like Figure 3-6 (a)) or multi-drop method (like Figure 3-6 (b)).	X	

UHS-II Implementation/Validation

- Transmitter Test

  - Eye Pattern and TX Parameter Test

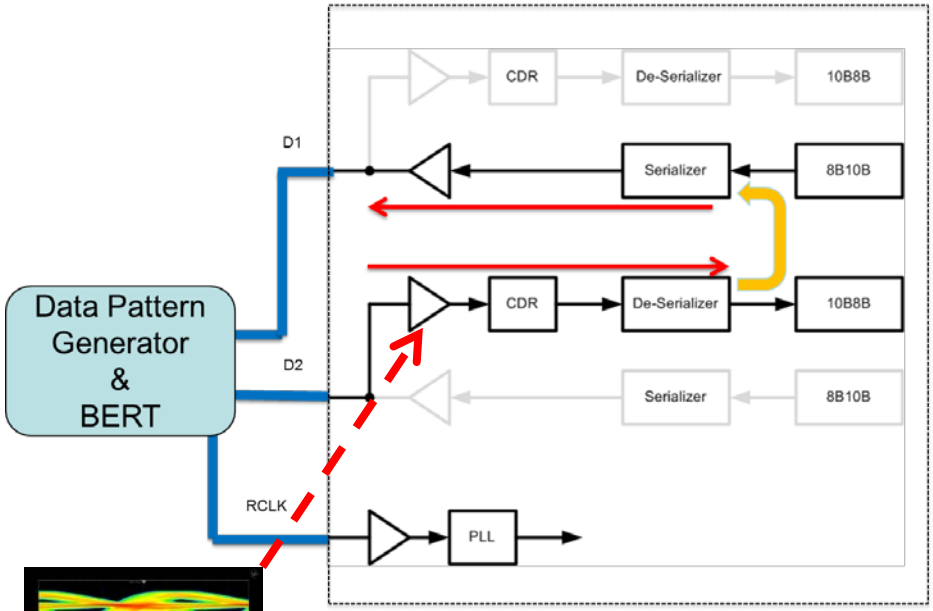


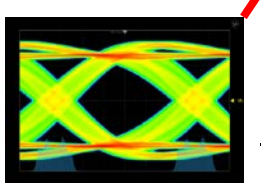


Loopback mode is defined in the spec.

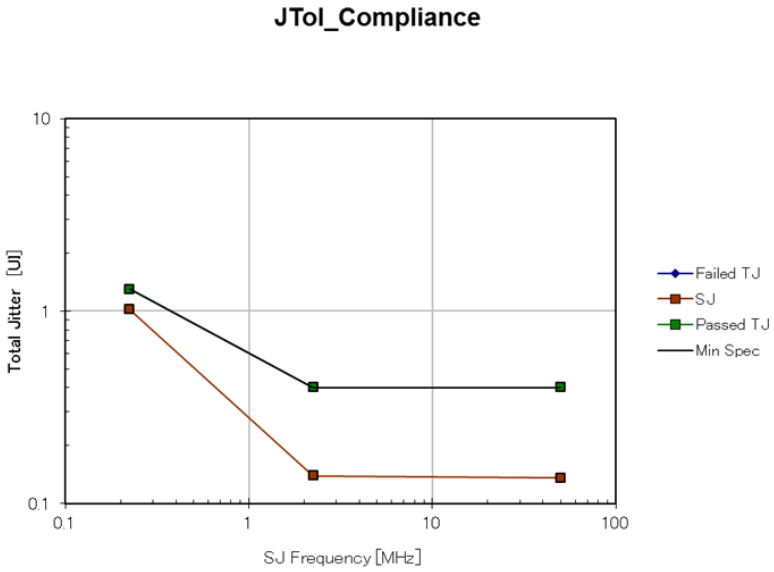
UHS-II Implementation/Validation

- Receiver Test
  - RX Jitter Tolerance Test



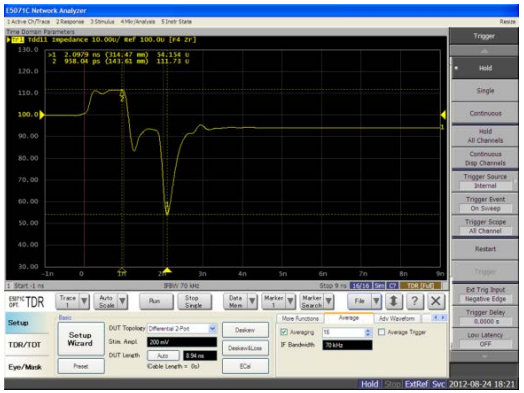


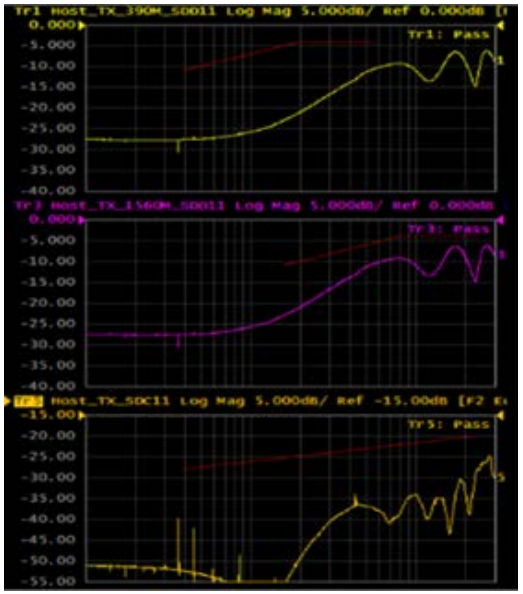
Stressed Eye

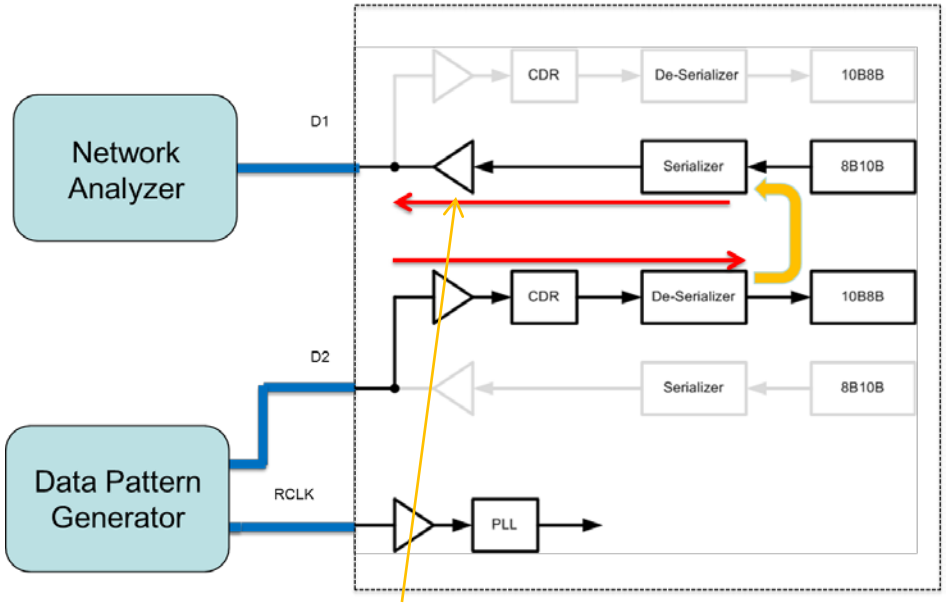


UHS-II Implementation/Validation

- Return Loss / Impedance Test
  - Hot TDR and Return Loss





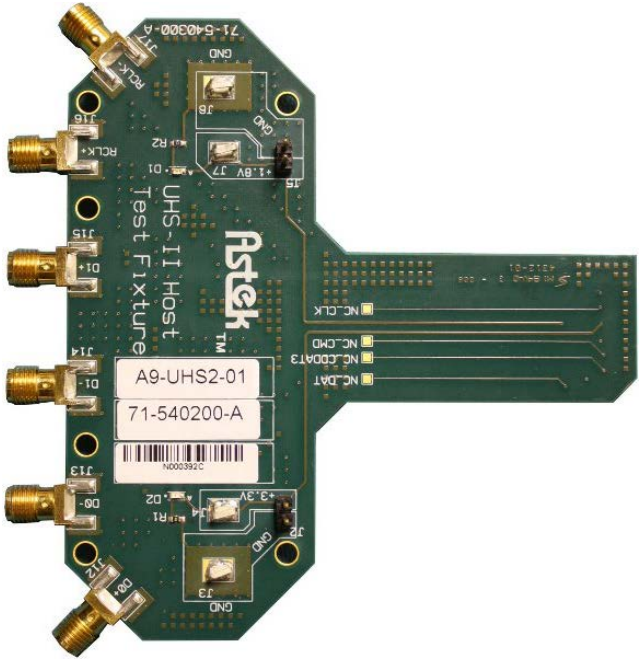


Exercise The Transmitter

UHS-II Implementation/Validation

- Test Fixtures
  - **Card Test Fixture**

  - **Host Test Fixture**



UHS-II Implementation/Validation

- Protocol Test (Test Demo at SDA Booth)
  - UHS-II Host/Card Tester