How Good Is Your Memory?

An Architect's Look Inside SSDs

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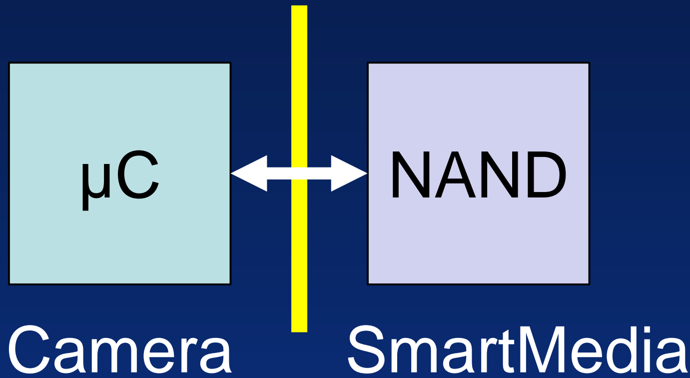
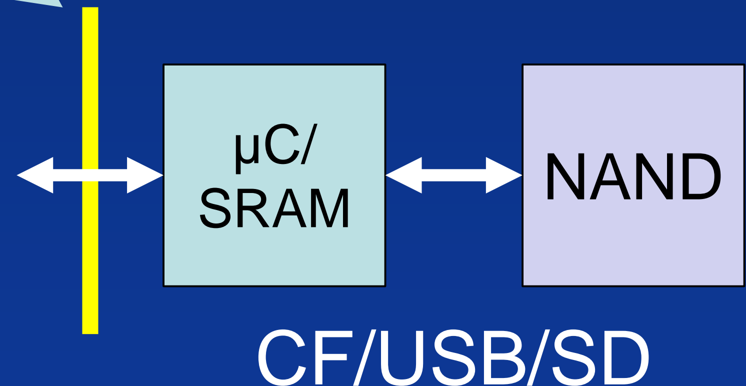
Early Storage Optimizations

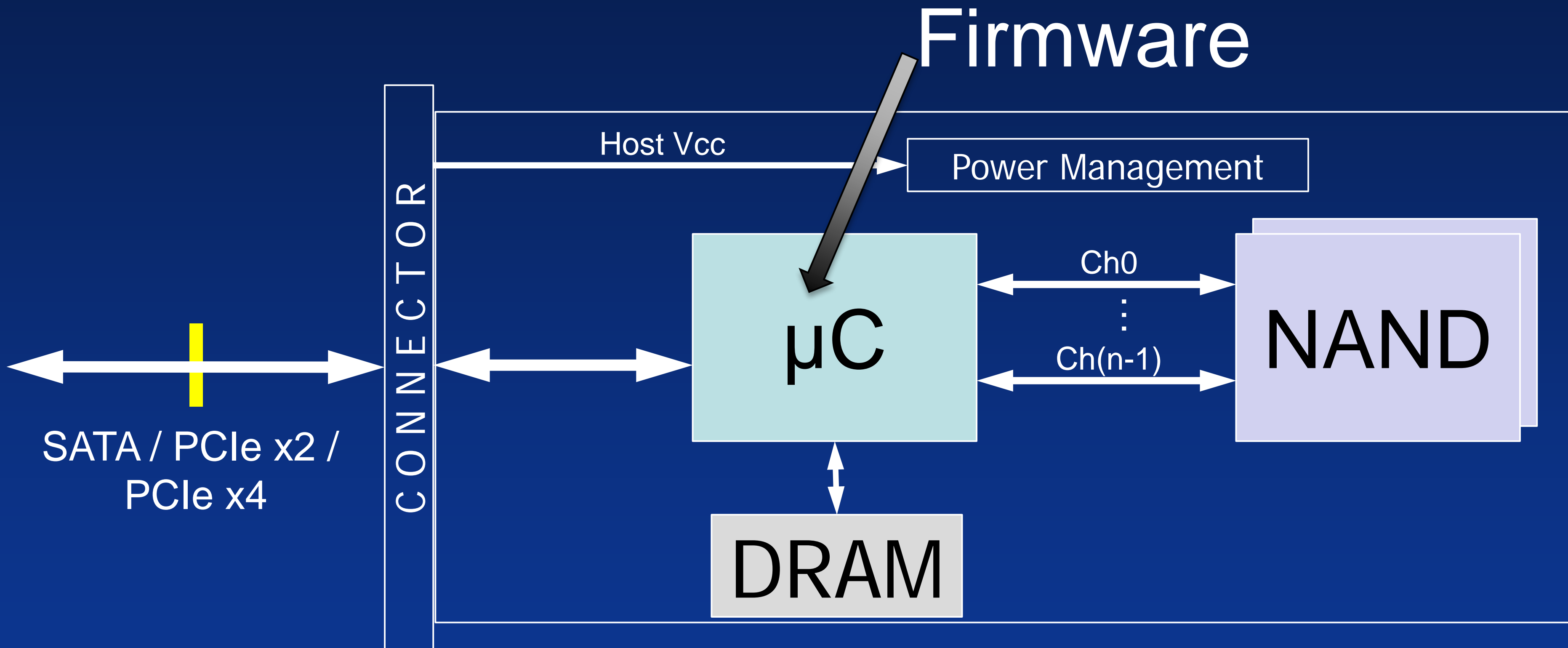


- Slow
- Early obsolescence
- Inexpensive solution

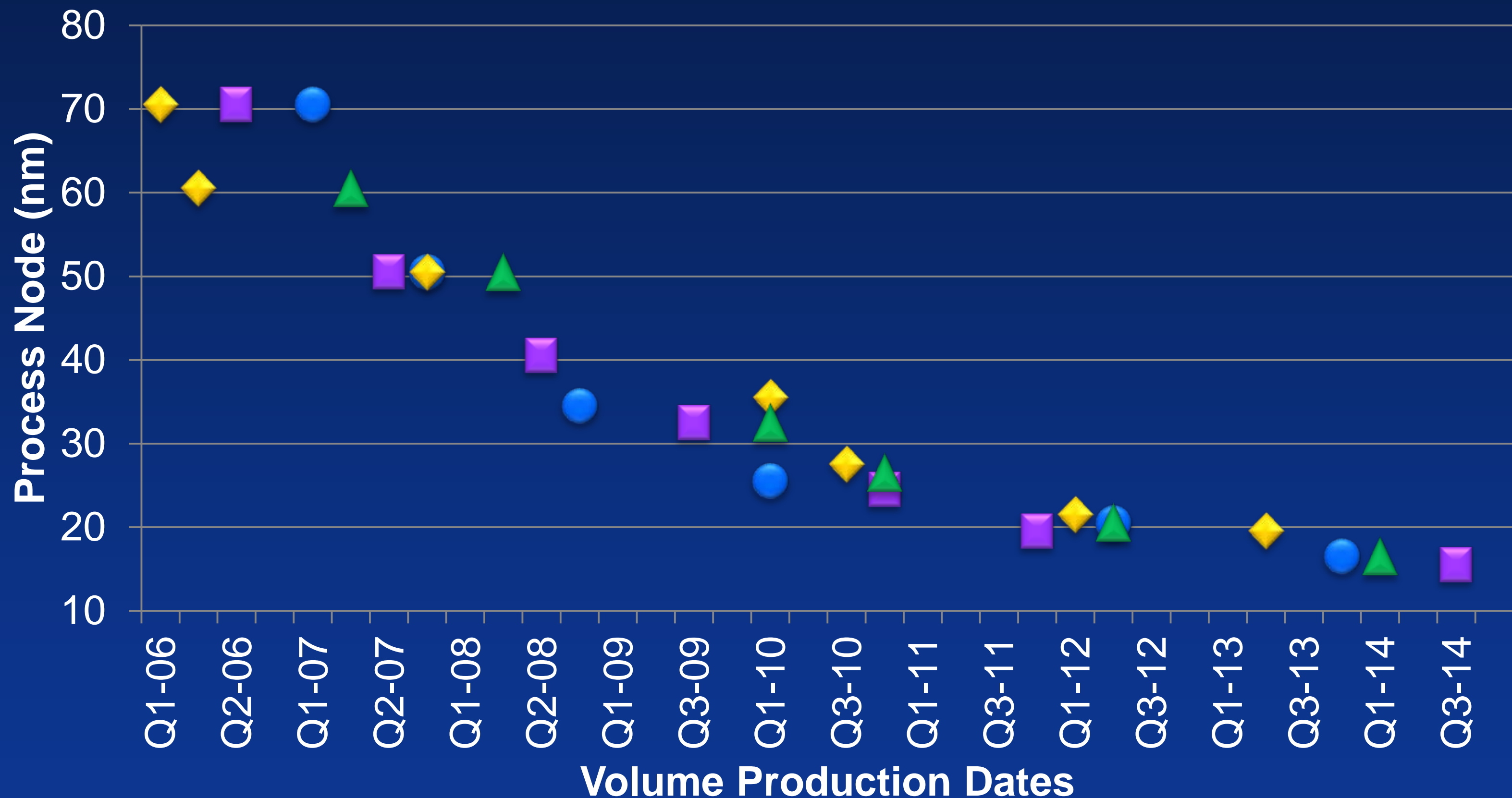
- Faster
- Upgradeable
- Slightly more expensive



High-Level SSD Architecture



The Past Decade of Planar NAND



- The industry went through 7-9 NAND lithography transitions

Data based on publicly known information.

What Happened in That Decade?

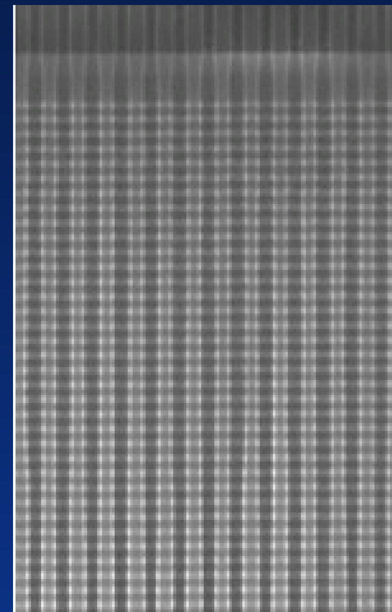
- Density: 2Gb → 128Gb per die
- Interface: 40MHz SDR → 266MHz DDR
- Bits per Cell: SLC → MLC → TLC
- Planes: 1 → 2 → 4
- Page size: 2KB → 16KB
- Block size: 128KB → 8+MB
- Packaging: 1ch TSOP-48 → 4ch BGA
- ECC: 1-bit Hamming → RS?/BCH → LDPC
- Electrons per Cell State: > 300 → 16
- Engineering skill: 1 college kid → 3+ PhDs

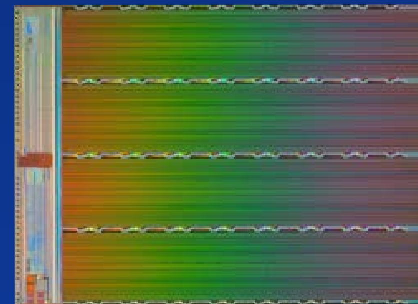
Could We Scale Planar NAND Beyond 16nm?

- Lower cost per bit
- Higher ECC
- Longer array operations
- Less data retention
- Less endurance
- More PhDs

3D NAND: Standing NAND on Its Head

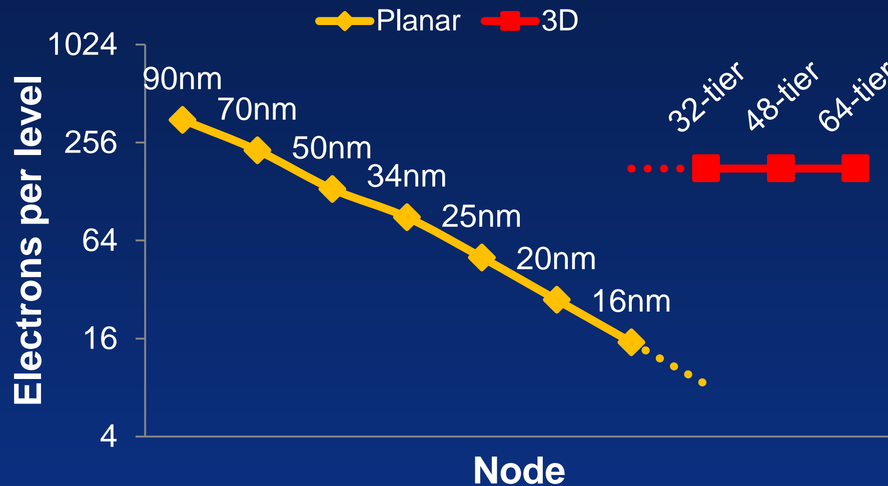
- 3D NAND cell architecture enables significant performance improvement
- 3D NAND cost improvement over planar expands with subsequent nodes

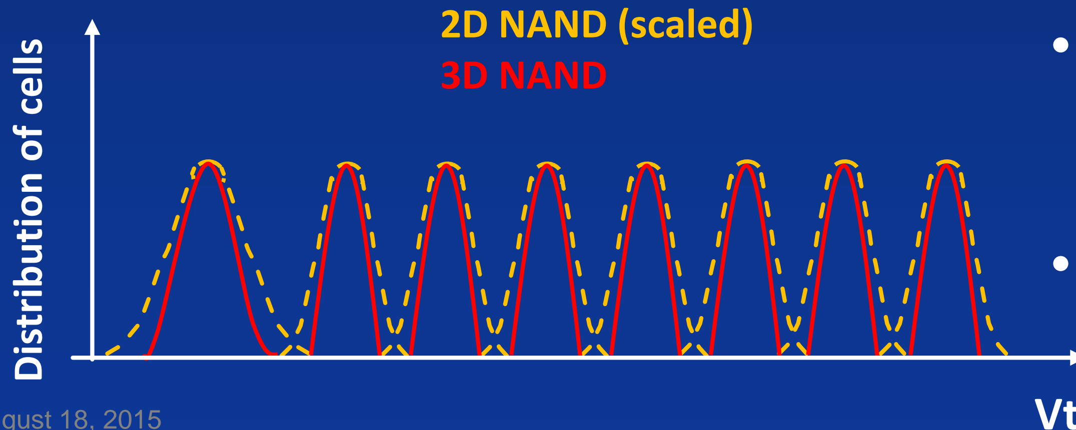




Flash Memory SUMMIT

3D NAND Reliability Relative to Planar NAND





3D NAND cell design simultaneously improves performance and reliability

- Vertical stacking allows large number of electrons per cell independent of scaling
- No longer relying on lithography to continue scaling
- Decreased interference between cells translates into higher cycling endurance
- Uses familiar memory materials – CT or FG

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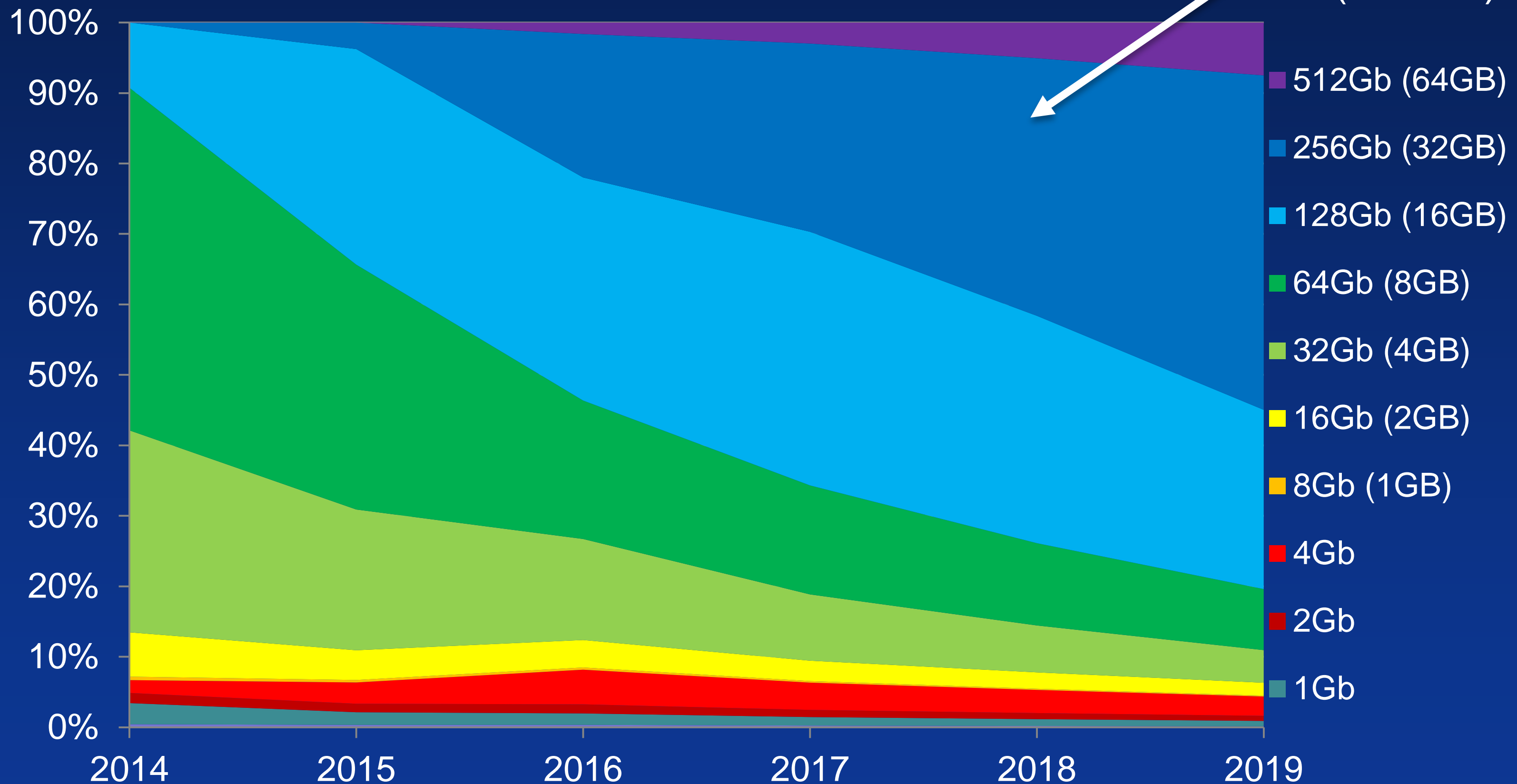
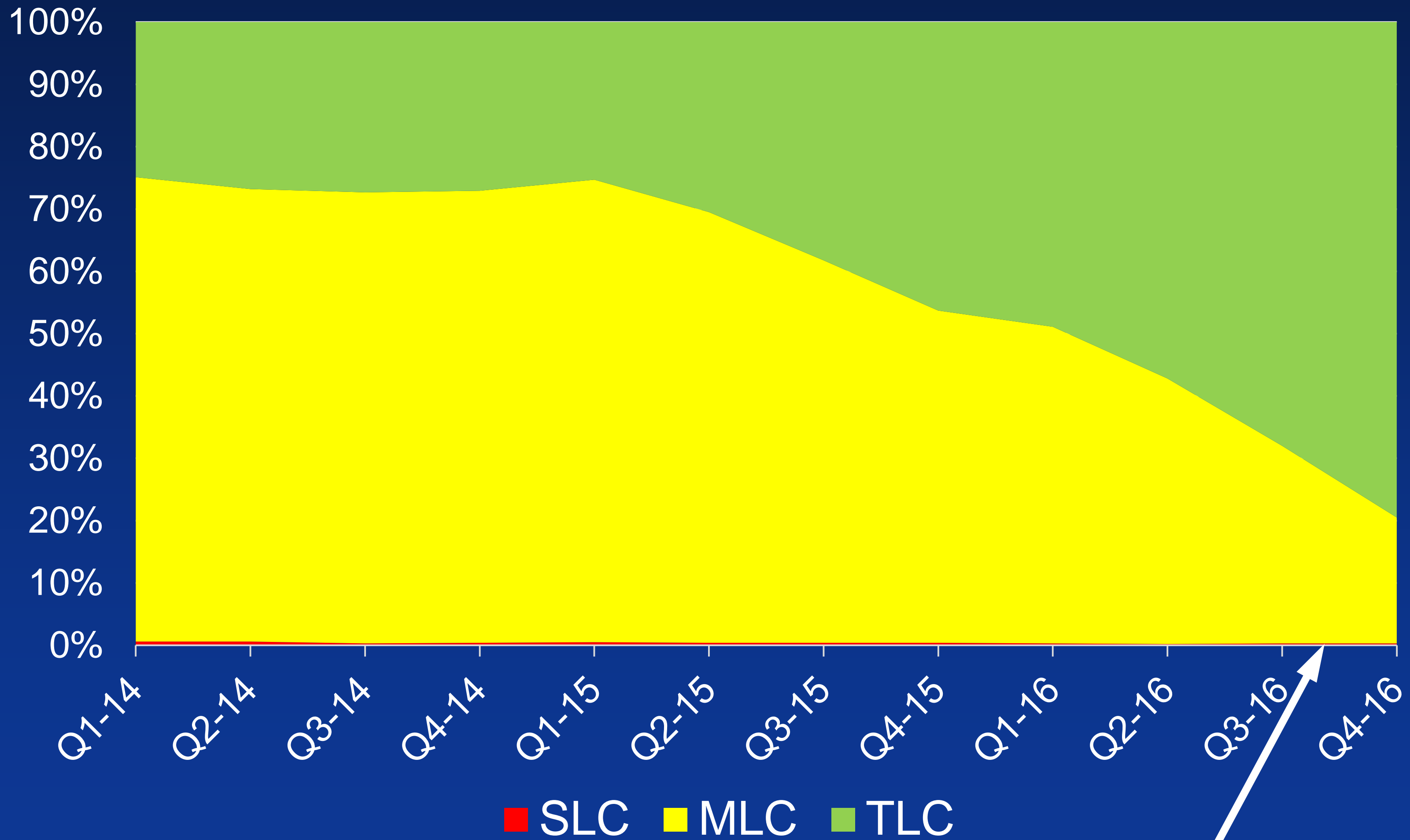
3D NAND Enables New Die Densities



Source: iSuppli 2Q15

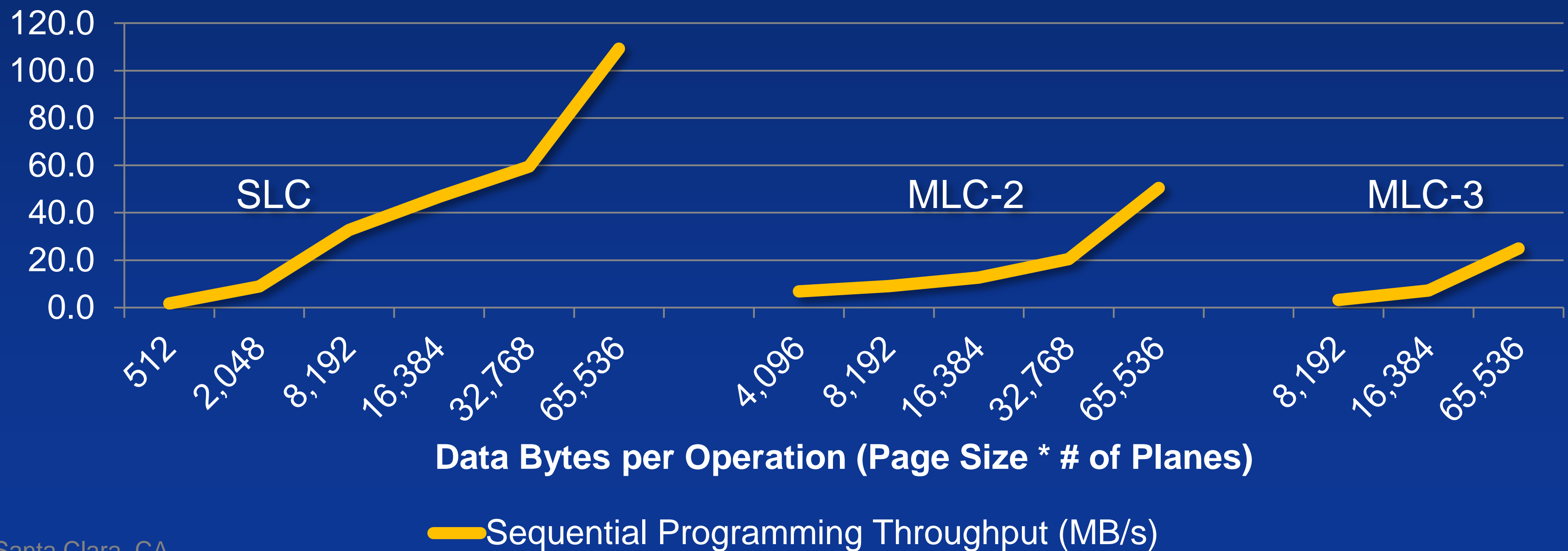
3D TLC NAND Goes Mainstream



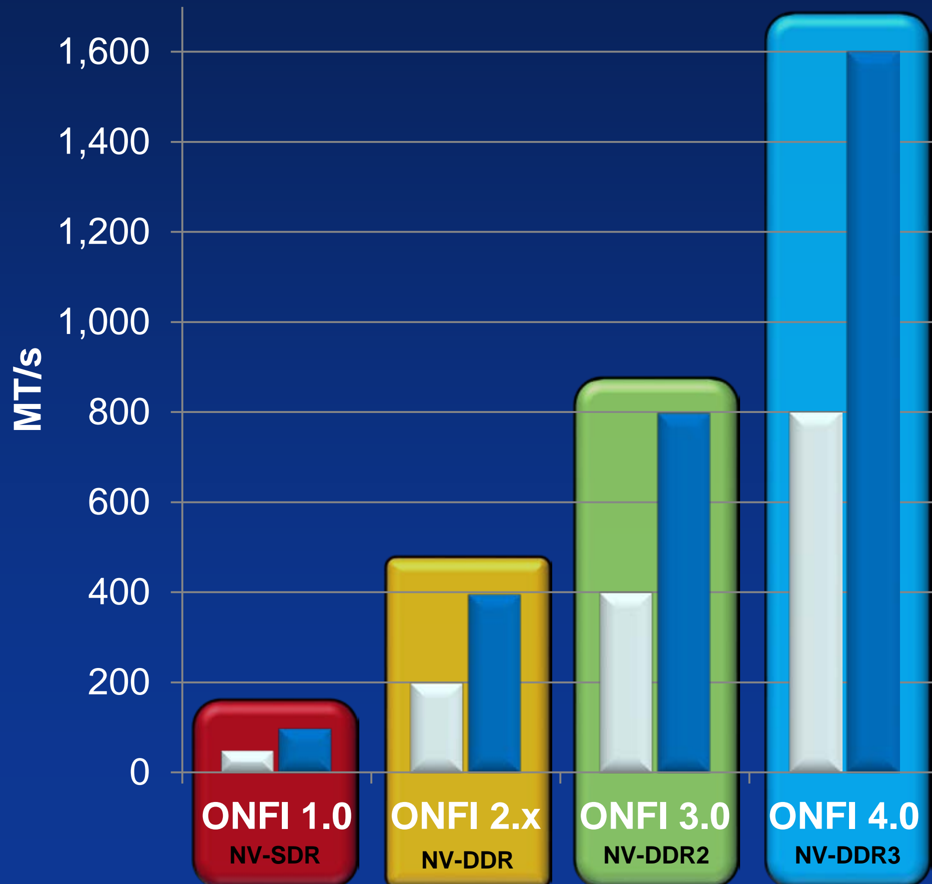
Source: iSuppli 2Q15

3D NAND Improves Array Performance

- Faster write bandwidth a result of larger number of data bytes per operation and a reduction in tPROG



ONFI 4 Results in Lower Energy

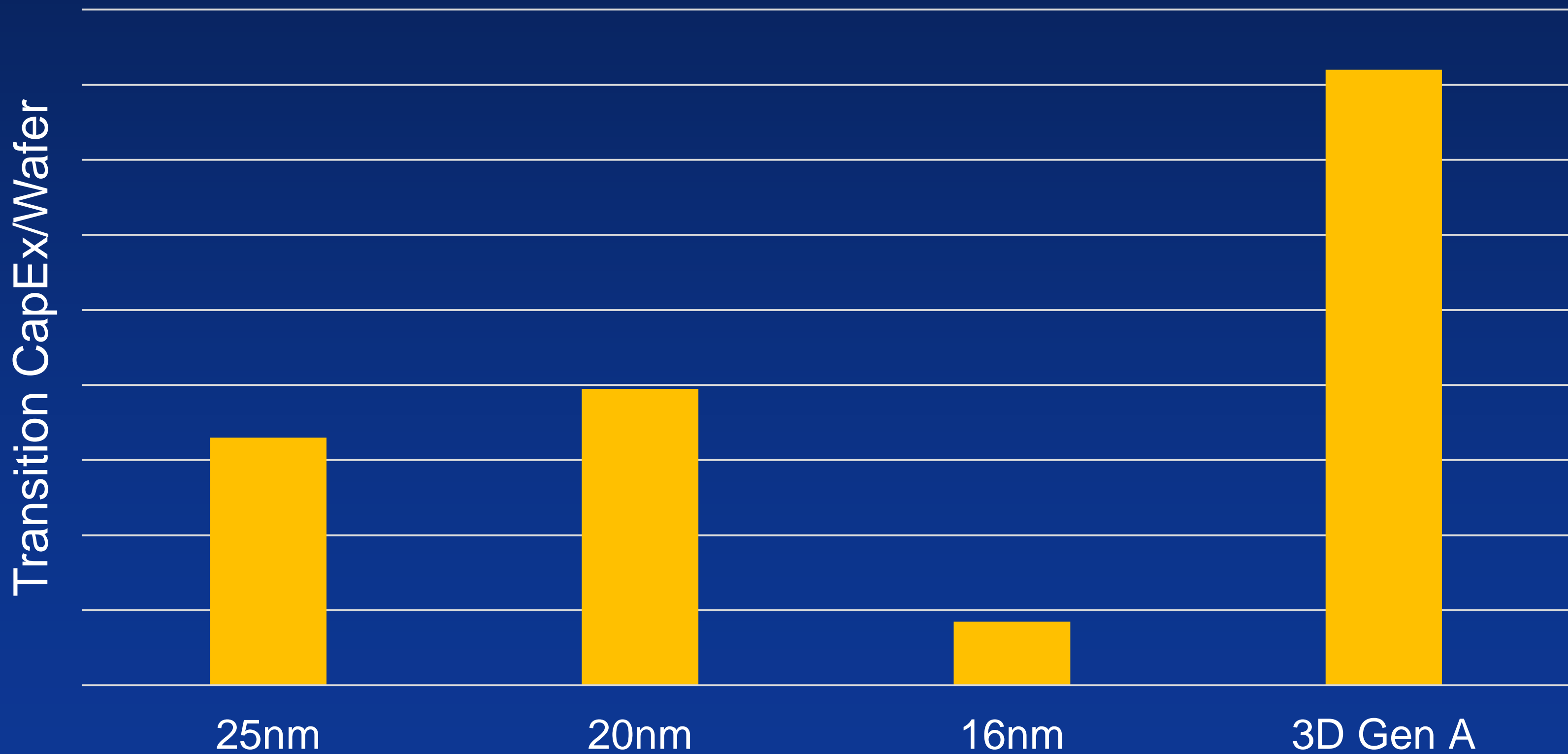


- ONFI 4.0 to be introduced with 3D NAND
- Interface up to 800MT/s throughput
- Reduces energy per bit with 1.2V interface

What's New?

- Density: Introduction of 256Gb
- Interface: ONFI 4.0, 1.2V
- Bits per Cell: MLC, TLC with SLC modes
- Electrons per Cell State: ~200
- Page/block/plane architecture follow traditional NAND scaling path
- Engineering skill: ~~1 college kid~~ 3+ PhDs

Why So Long to 3D NAND?!



Questions?

About Michael Abraham

- Business Line Manager in the Storage Business Unit at Micron
- Former NAND Architect
- Covers emerging memories and 3D XPoint™
- IEEE Senior Member
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