Comparison of 20 nm & 10 nm-class 2D Planar NAND and 3D V-NAND Architecture

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TechInsights

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  - 20 nm - class
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  - Key Technologies & Barriers
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  - Key Technologies & Barriers
- Conclusions

NAND Technology

❑ Introduction

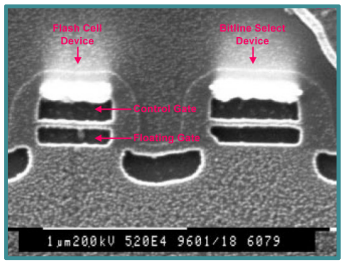
Let's think about ……

- ✓ **NAND, still needed in the future?**
- ✓ **Scaling-down, still needed?**
- ✓ **2D planar NAND, physical limitations?**
- ✓ **2D planar NAND, electrical limitations?**
- ✓ **3D V-NAND, no limitations?**
- ✓ **No devices to replace NAND?**
- ✓ **etc.**

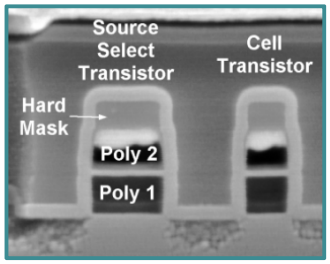
NAND Technology

❑ Introduction

Shrink, Shrink, Shrink, ……



16M (Samsung, 450 nm)
1994

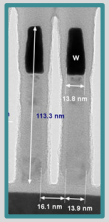


256M (Toshiba, 180 nm)
1999

4G (IMFT, 50 nm)
2005

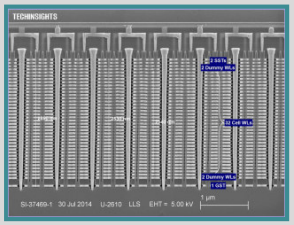
64G (IMFT, 20 nm)
2010

2D



16G (Toshiba, 15 nm)
2015

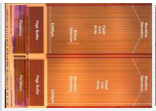
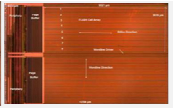
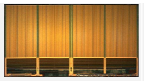
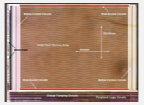
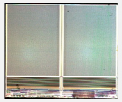
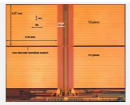
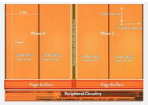
3D



128G (Samsung, 32L, MLC/TLC)
2015

NAND Technology Trend

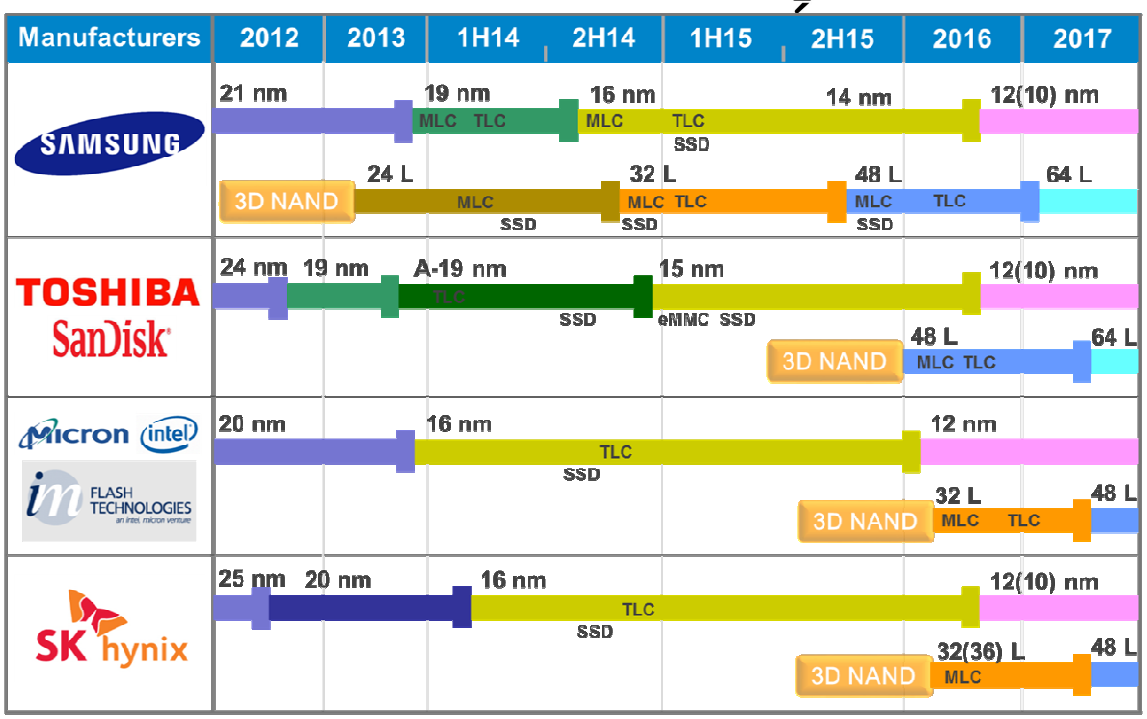
❑ Major Players & Process Node

Makers	20 nm Class (2D)	10 nm Class (2D)	3D NAND
SAMSUNG	 27nm  21nm	 19nm  16nm	 24L  32L MLC  32L TLC
TOSHIBA SanDisk	 24nm	 19nm  15nm  A-19nm	
Micron / IM FLASH TECHNOLOGIES	 25nm  20nm	 16nm	
SK hynix	 26nm	 16nm	

NAND Technology Trend

TECHINSIGHTS

❑ Technology Roadmap

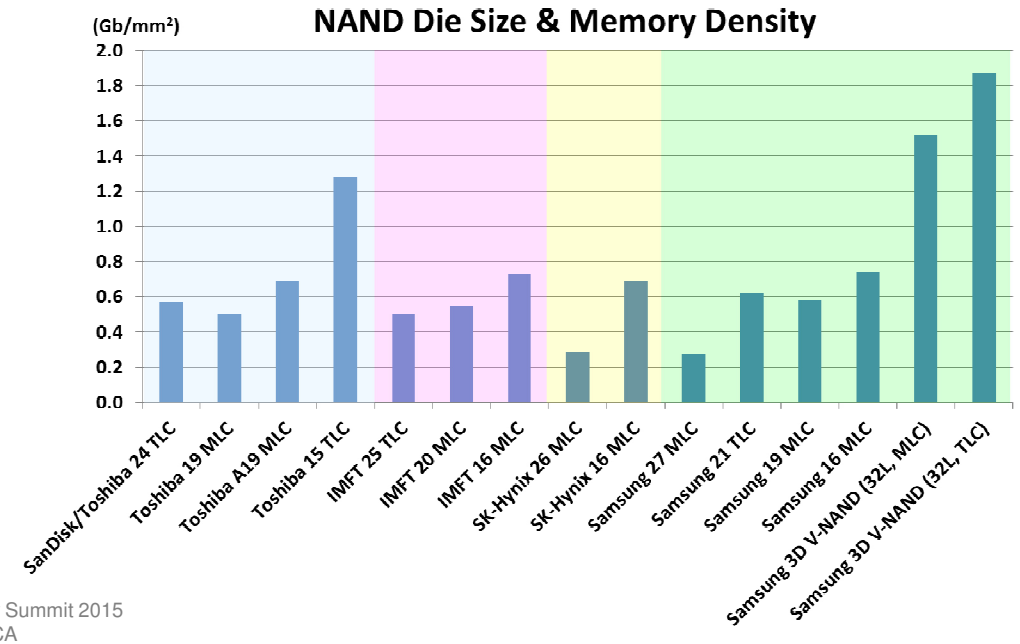


NAND Technology Trend

TECHINSIGHTS

Die Size & Memory Density

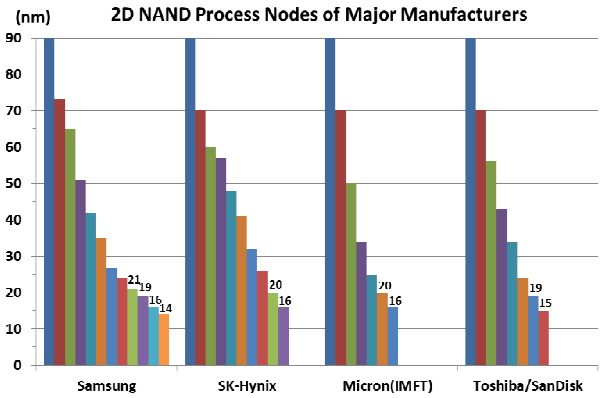
- ✓ 2D Planar: Up to 1.28 Gb/mm² (Toshiba/15 nm)
- ✓ 3D V-NAND: Up to 1.87 Gb/mm² (Samsung/32L), 2.8 Gb/mm² (48L)

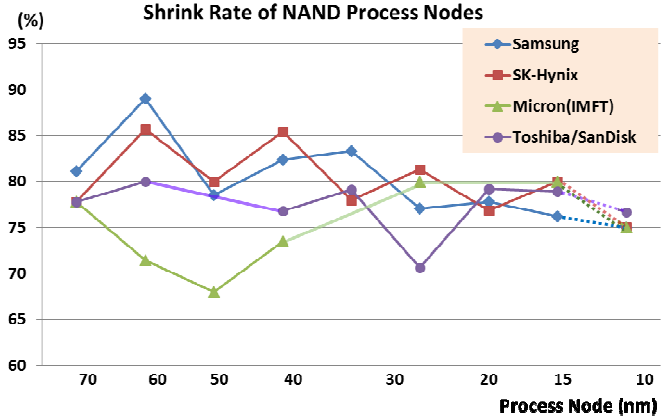


2D Planar NAND

❑ Process & Design Overview: Shrink Factor

- ✓ **Shrink Factor: 0.75 ~ 0.8**
- ✓ **20(19) nm / 2012 → 16(15) nm / 2014 → 12 nm / 2016 → 9 nm / 2018**

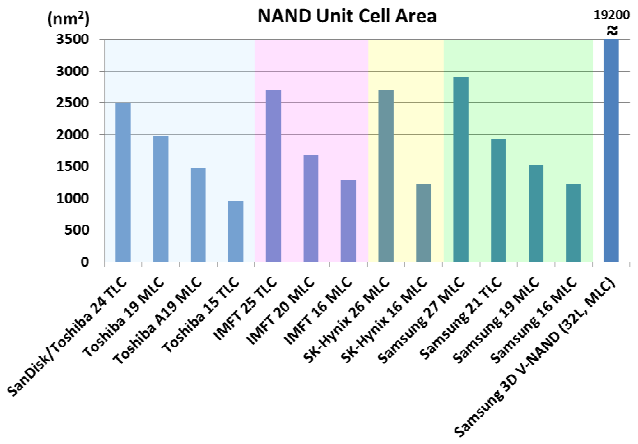


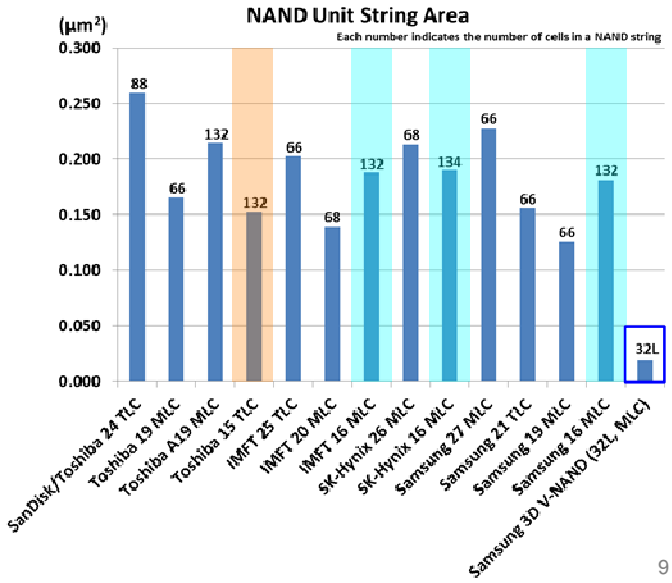


2D Planar NAND

❑ Process & Design Overview: Unit Cell/String Area

- ✓ **Unit NAND Cell Area: Scale-down to 0.00096 μm²**
- ✓ **Unit String Area (@132 WLs): Scale-down to 0.152 μm²**
- ✓ **Unit Cell Area (3D V-NAND @20 nm): 0.019 μm² (32L, 48L, 64L, 128L)**





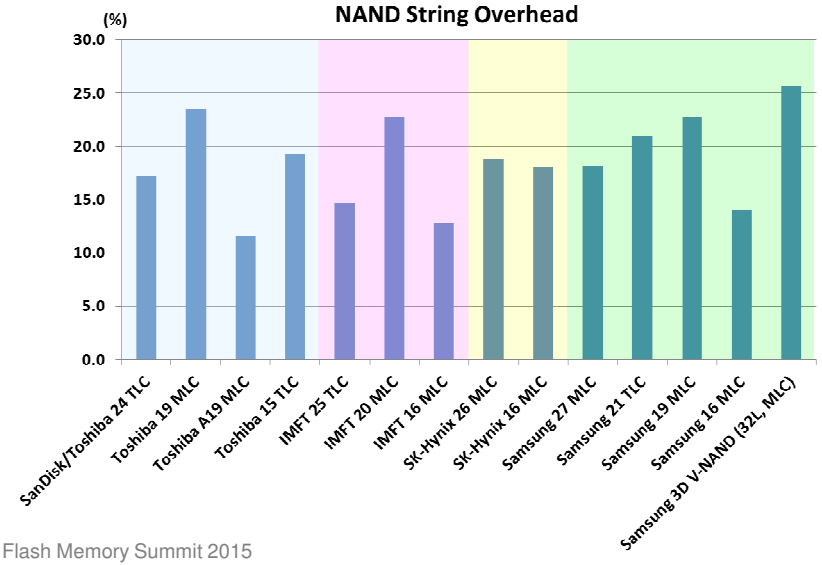
2D Planar NAND

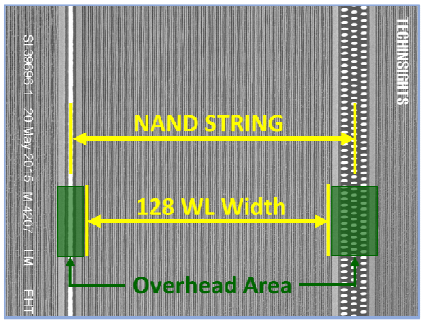
Process & Design Overview: String Overhead

- ✓ **NAND String Overhead**

  = A ratio of overhead length to the total length of NAND string

- ✓ **Overhead 13 ~ 14% for Samsung/IMFT 16 nm MLC NAND**





2D Planar NAND

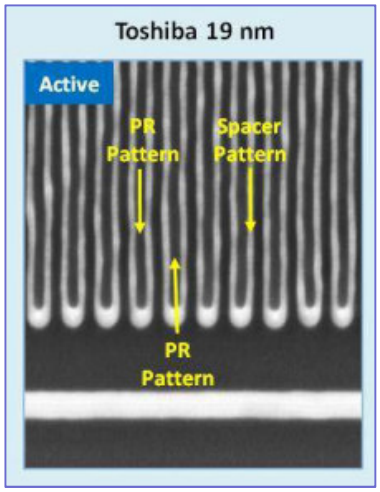
❑ Key Words to Scale-down (Process/Architecture)

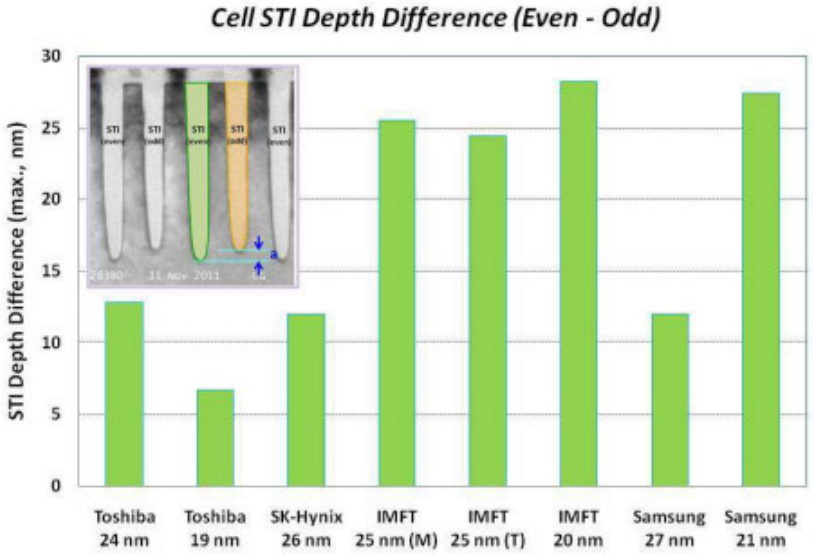
✓ **Patterning Technology**	• Three Critical Steps: Active, Gate, Bitline • DPT → (TPT) → QPT → ? • How to reduce # Masks?
✓ **Air-Gap process Technology**	• Active, Gate, Bitline Cross talk • Uniformity?
✓ **IPD Engineering**	• ONO + Nitridation
✓ **Flow-able CG Technology**	• Si + C for narrow space
✓ **Interconnection Design**	• WL Extension Region (Layout)

2D Planar NAND

❑ Patterning Technology (DPT, Active)

- ✓ **SADP, SARP and LELE Process**
- ✓ **Process optimization including depth/space difference needed**



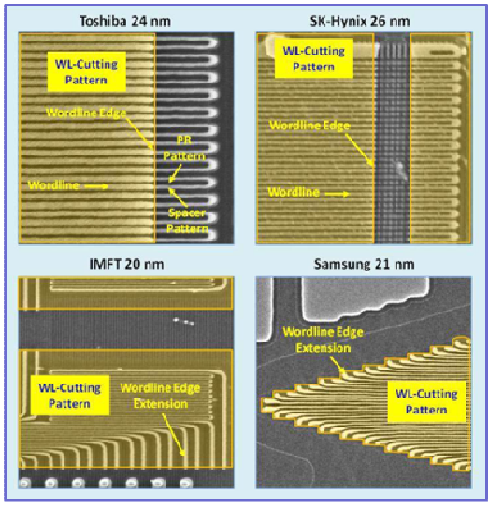


2D Planar NAND

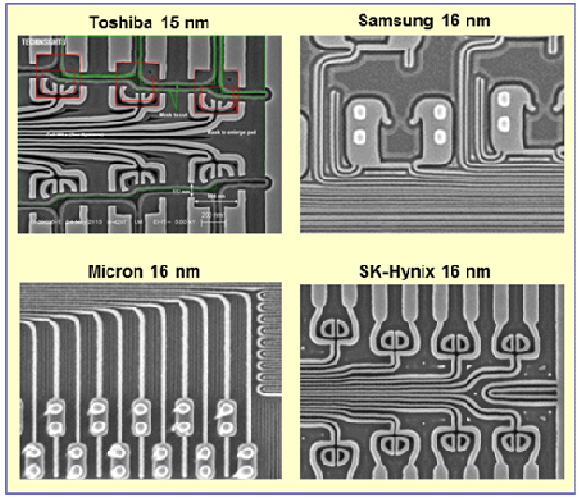
❑ Patterning Technology (DPT & QPT, Gate)

- ✓ How to reduce # masks for QPT (ex. 4 Masks)
- ✓ Cell Mask → Enlarge Mask → Pad(Peri, SSL & GSL) Mask → Cut-off Mask

Comparison DPT Patterns



Comparison QPT Patterns

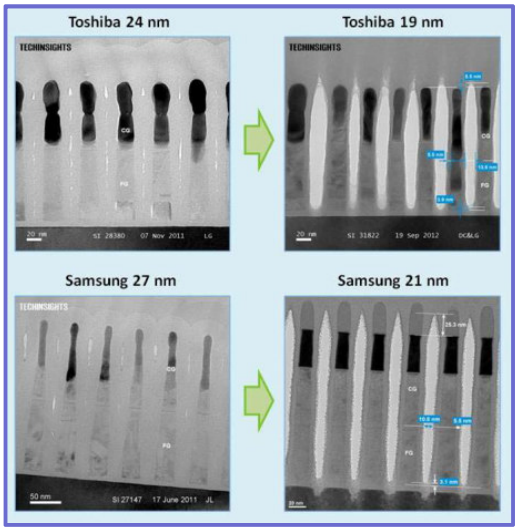


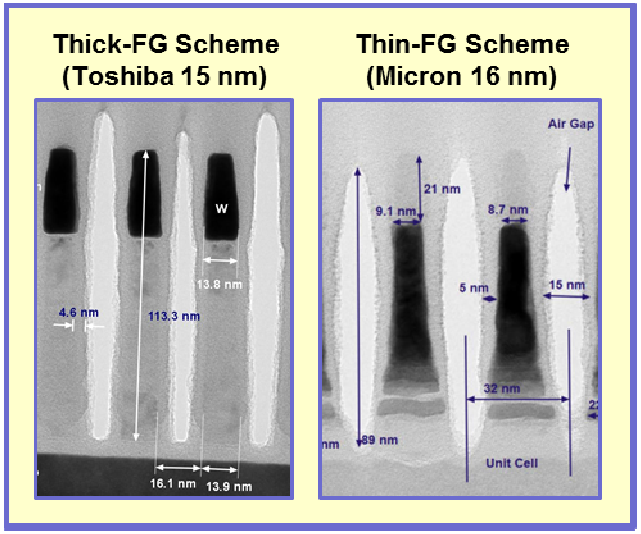
2D Planar NAND

❑ Air-Gap Technology: Gate

- ✓ Interference (cross-talk) causes V_T distribution
- ✓ Wordline Loading

→
- Low-k dielectric
- Air-Gap



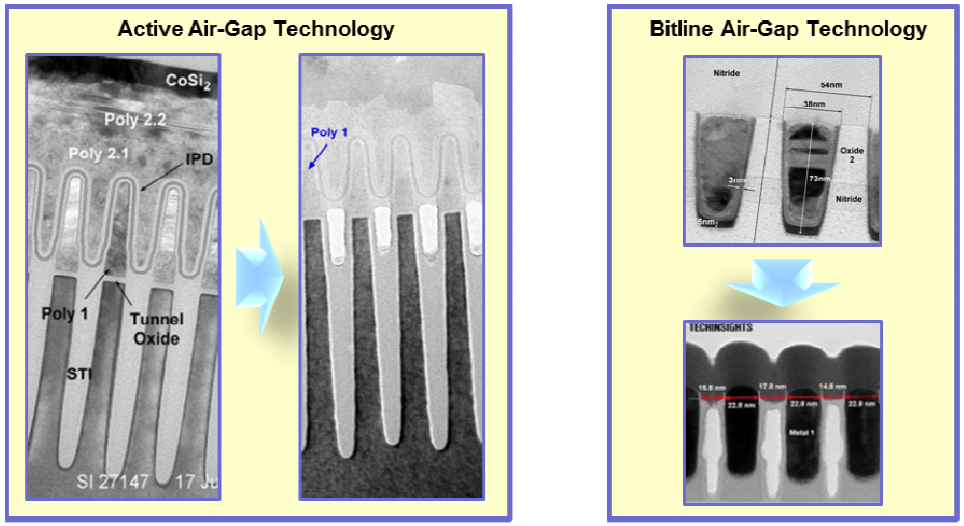


2D Planar NAND

Air-Gap Technology: Active & Bitline

- ✓ Bitline Loading causes RC delay
- ✓ Cell-to-cell interference (neighbor bitlines)

→
- Low-k dielectric
- Air-Gap



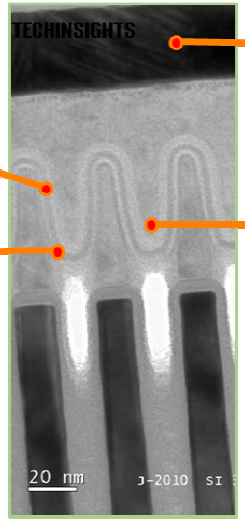
2D Planar NAND

IPD/CG Engineering

- ✓ IPD: Barrier optimization, coupling area, coupling ratio
- ✓ CG: Materials, Defect (nano-void)-free deposition

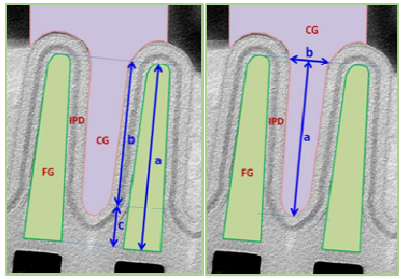
✓ IPD: Thinner barrier dielectric & nitridation (NONON)

✓ IPD/FG: Effective FG height wrapped with IPD layer to increase coupling area between FG and CG



✓ CG: Metal or metal silicide materials (CoSi, NiSi, W, etc.)

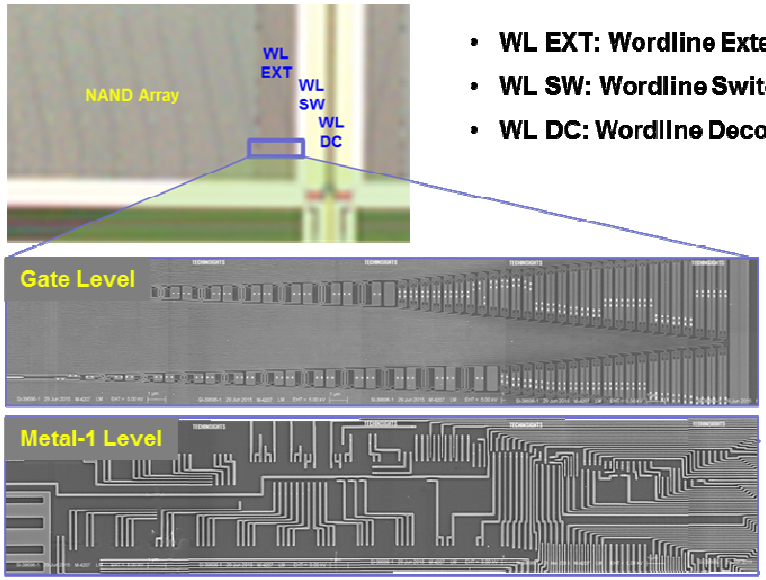
✓ CG: Deposition/Fill in narrow space (<5~7nm) (Flow-able CG poly-Si)



2D Planar NAND

Interconnection Design

- ✓ Interconnection area overhead
- ✓ Optimization QPT (Cell Gate WLs) extension patterns/layout



- WL EXT: Wordline Extension Area
- WL SW: Wordline Switching Area
- WL DC: Wordline Decoder Area

3D Vertical NAND

Major Players on Commercial Market

- ✓ Samsung: Aug. 2013 ~, 32-tier TLC (on market), 48 & 64-tier (on Dev.)
- ✓ Toshiba/SanDisk, Micron/Intel, SK-Hynix: Still on testing/sampling

84.3 mm², 1.52 Gb/mm²

Samsung 850 PRO SSD (256GB/2014)

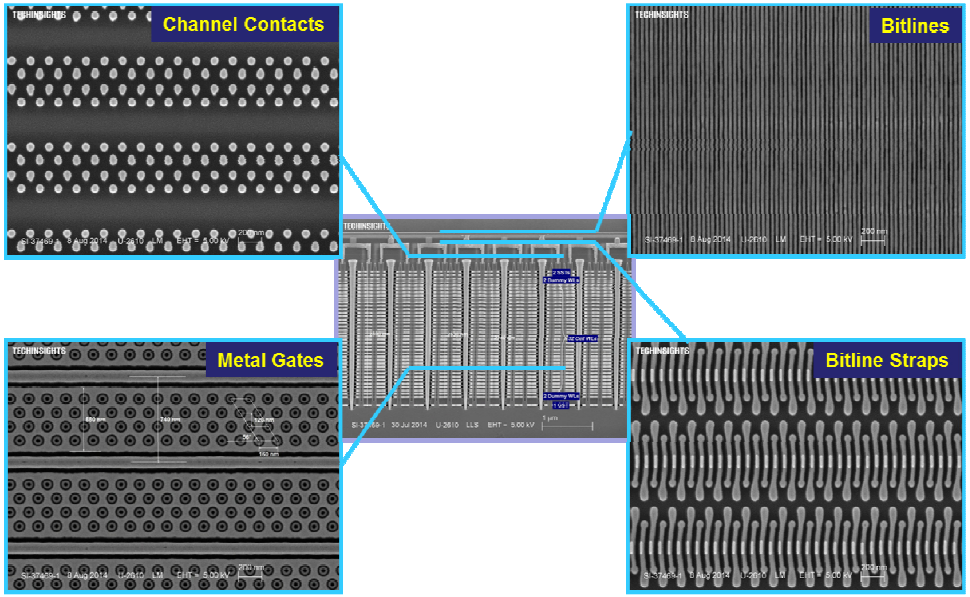
68.3 mm², 1.87 Gb/mm²

Samsung 850 EVO SSD (500GB/2015)

3D Vertical NAND

Samsung V-NAND (32 L) Overview

- ✓ 39 TR Layers: 32 NAND Cells, 4 Dummy Cells, 2 SSTs, 1 GST
- ✓ Staggered bitline contacts with wavy straps



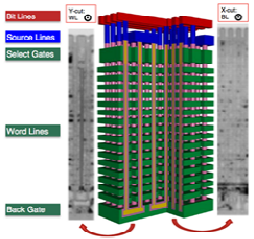
■ 3D Vertical NAND

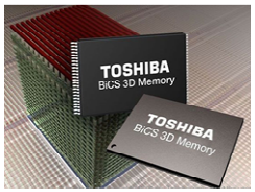
TECHINSIGHTS

❑ 3D NAND: Other Players (R&D/Sampling)

✓ **FG or CTF structure: FG may be difficult (Process Integration)**

■ Toshiba/SanDisk

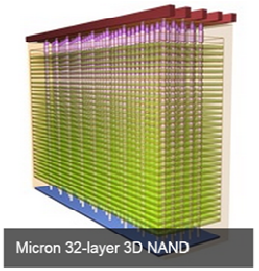


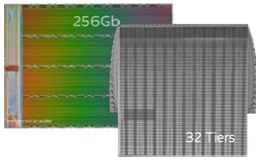


Source: Toshiba

CTF

■ Micron/Intel

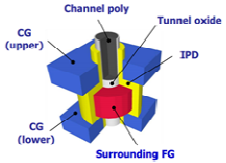




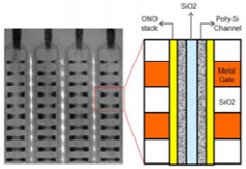
Source: Micron/Intel

FG

■ SK-Hynix



DC-SF
(Dual CG-Surrounding 3D FG)



SMArT
(Stacked Memory Array Transistor)

Source: SK-Hynix

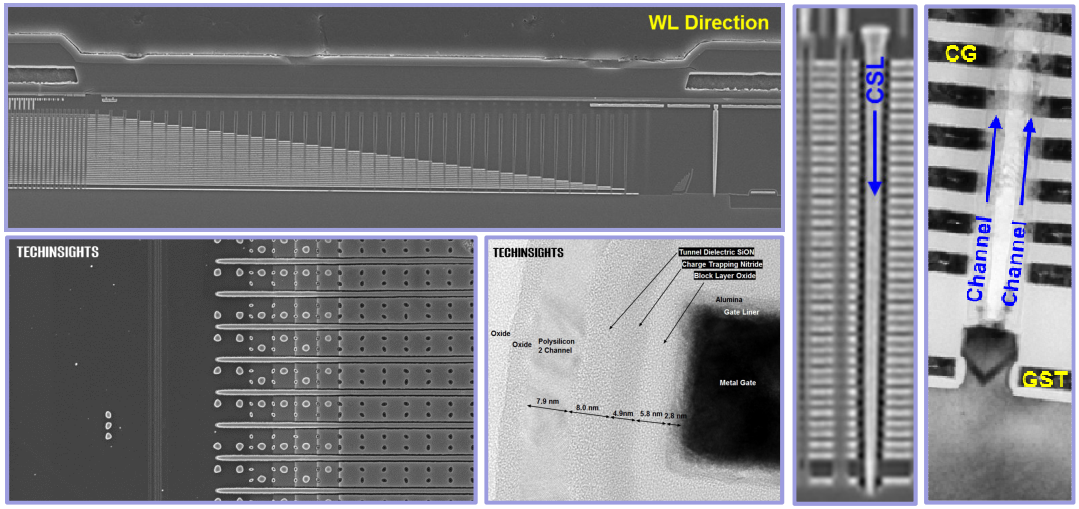
CTF

3D Vertical NAND

TECHINSIGHTS

Key words for future 3D NAND

- ✓ 48L, 64L, 96L and 128L with Higher Aspect Ratio Hole Process
- ✓ Cell WL Interconnection: # Masks, Layouts, Trimming, Uniformity
- ✓ Vertical Channel: Doping/Junction Engineering
- ✓ CTF/IPD Engineering



Summary

TECHINSIGHTS

❑ Comparison 2D and 3D NAND

- **2D Planar NAND**
  - ✓ 10 nm (or 9 nm) would be the last node (TLC)
  - ✓ Current QPT will be used on 12 nm and 10 nm
  - ✓ Challenges:
    - Flow-able CG, IPD, Tunnel Oxide, Cell Interference
    - # Electrons, Cell Uniformity → V_T distribution (ECC)
    - # Cycles (Endurance), Retention

- **3D NAND**
  - ✓ 48L and 64L would be possible. But, not the 96L or 128L
  - ✓ Current 20 nm (or 16 nm) node will be used on 48L and 64L
  - ✓ Challenges:
    - Higher number of layers → High-A/R, Process Integration
    - # Masks (# PR Trim), ALD-CVD (Dielectrics), Cell Uniformity