

Improving NAND Flash Reliability with Rank Modulation

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joint work with

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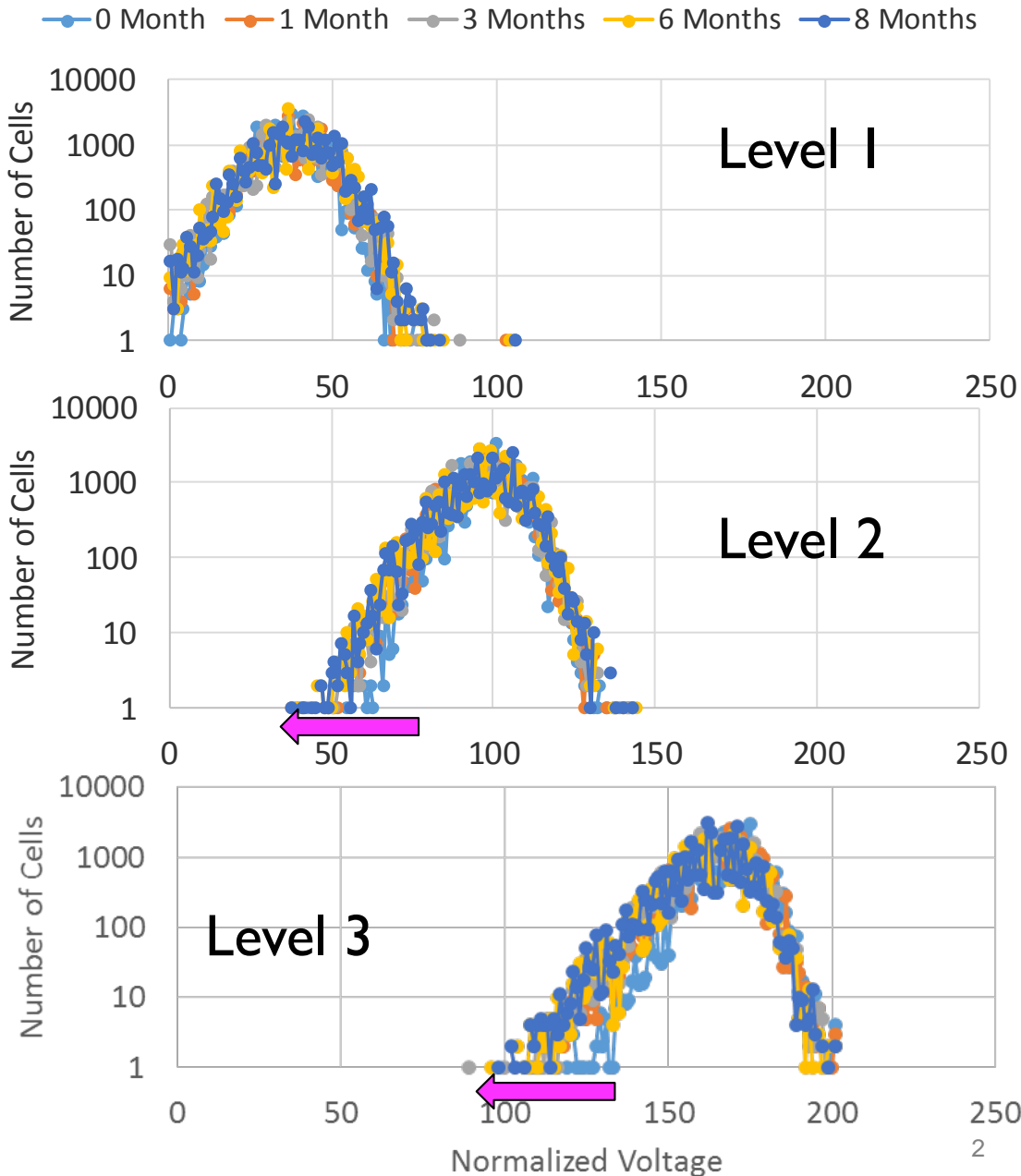
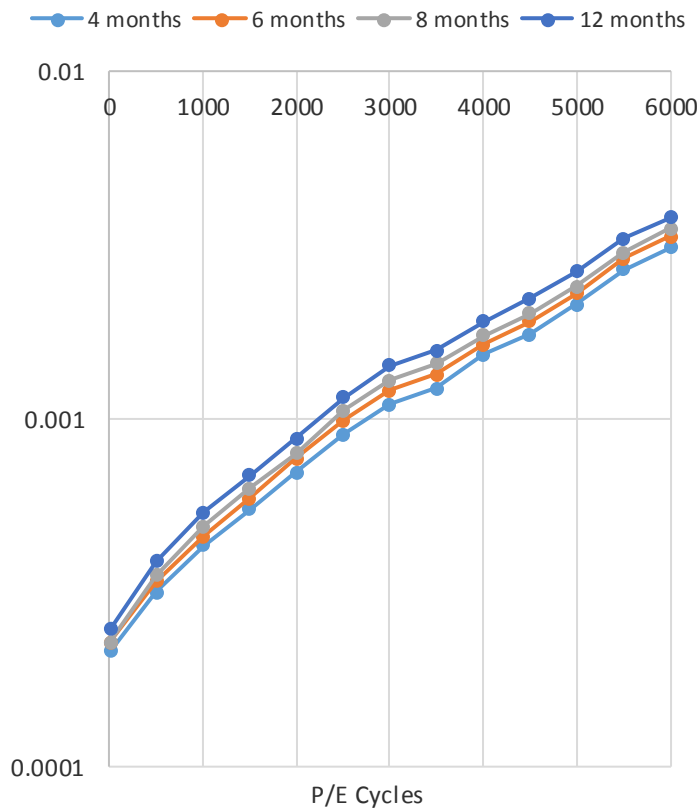
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Asymmetric Voltage Drift in 1x nm MLC NAND

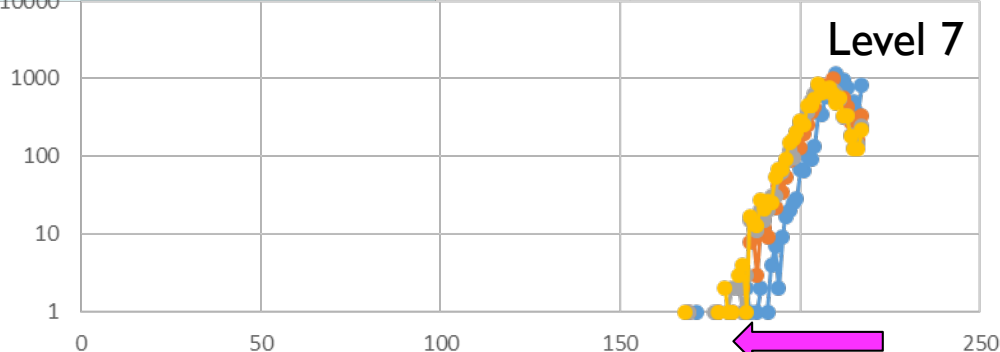
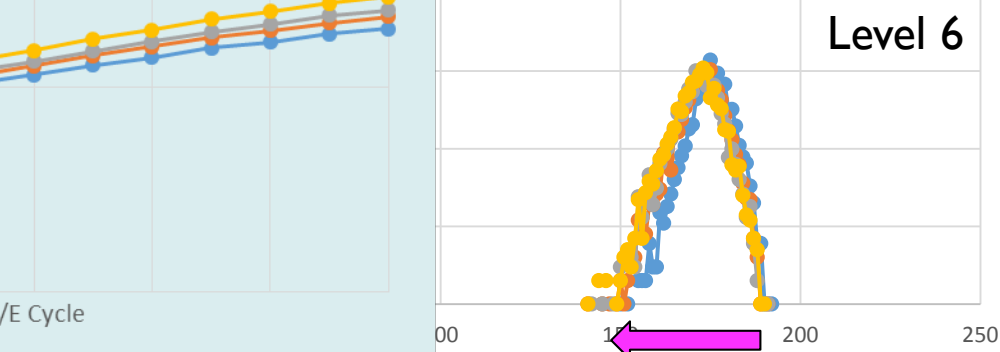
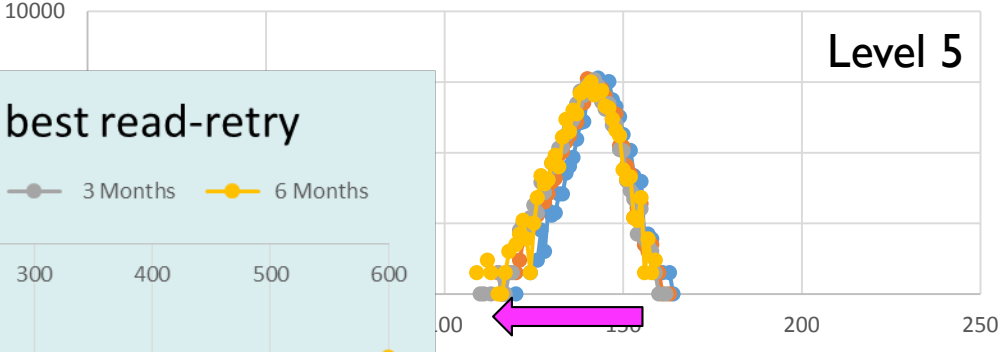
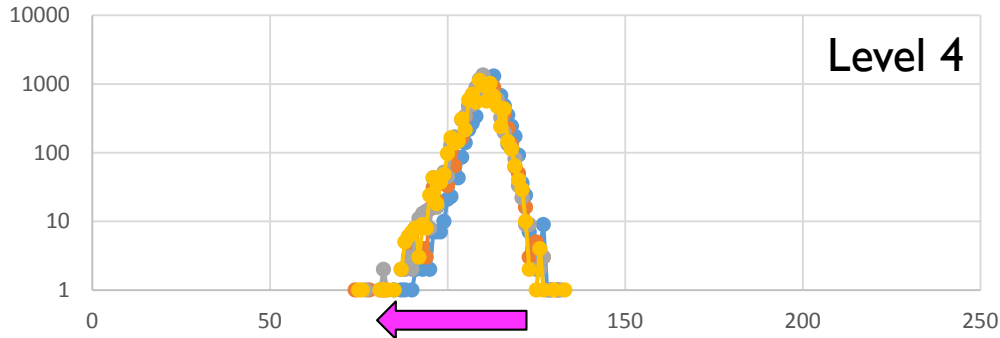
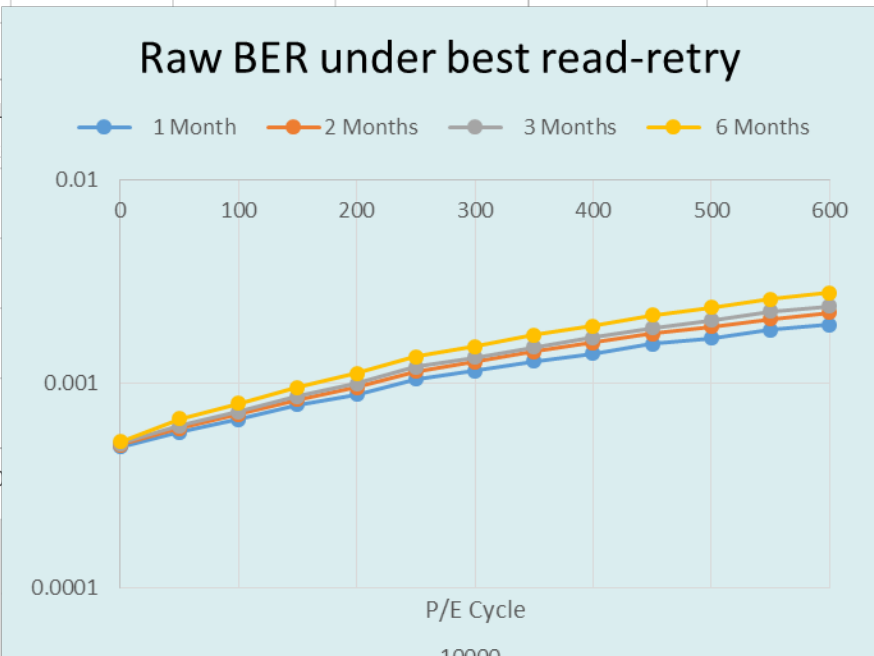
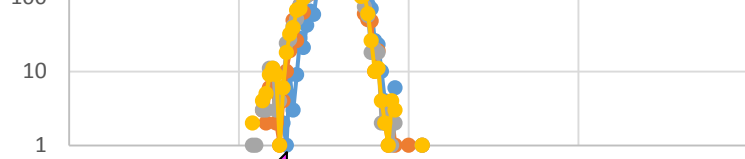
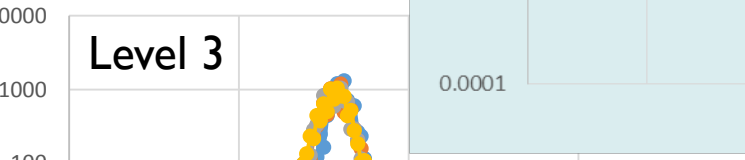
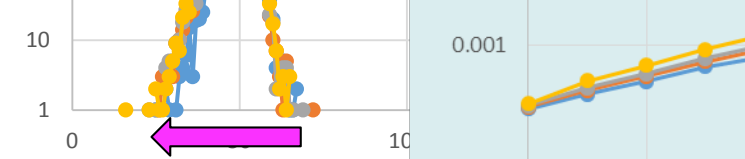
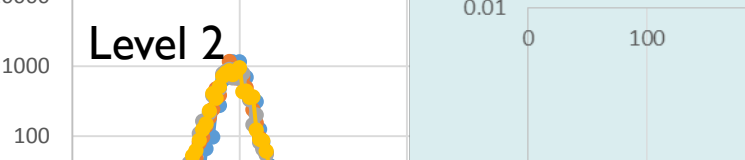
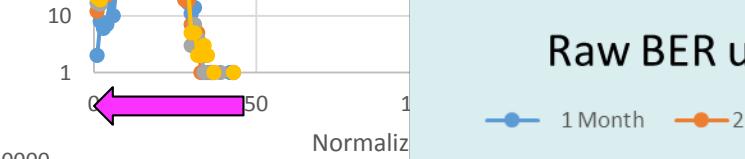
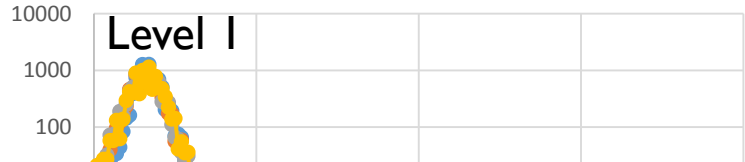
- High temperature data retention measured in our lab. (following JEDEC standard)

Raw BER under best read-retry

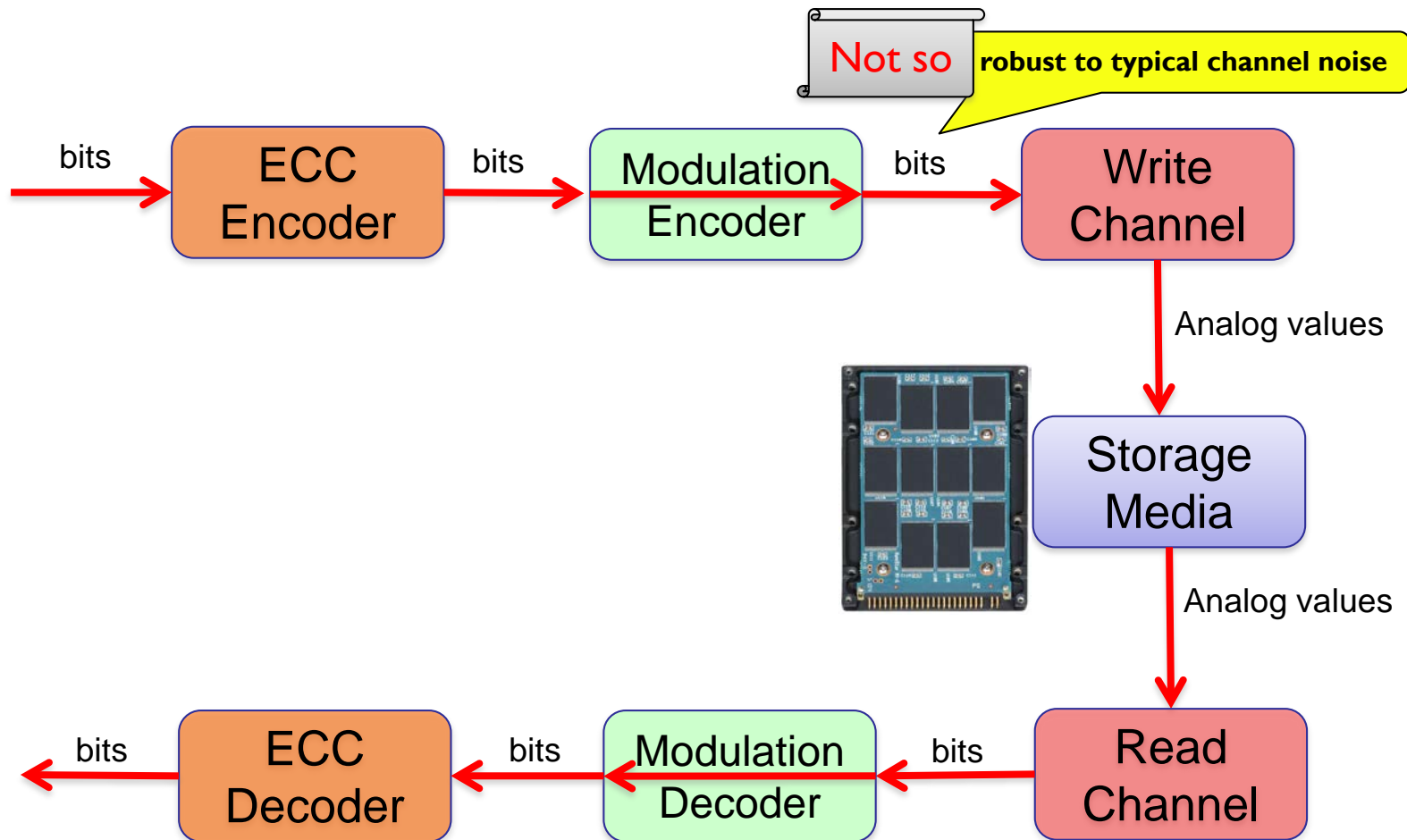


Asymmetric Voltage Drift in 1y nm TLC NAND

0 Month 1 Month 3 Months 6 Months



Flash (of High Density) Needs Modulation

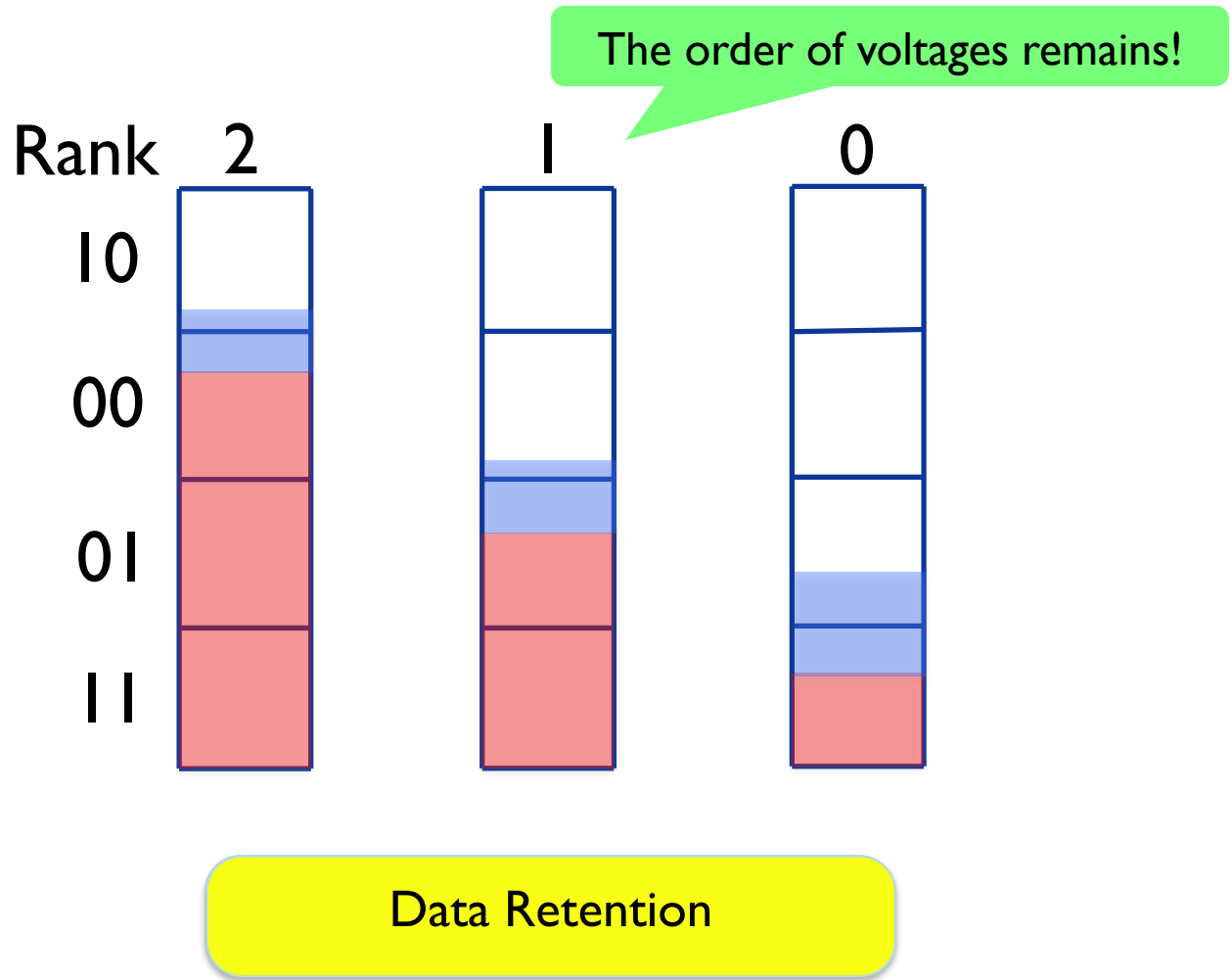


Adding Modulation for Flash

- Simple
 - Easy to implement
 - Easy to teach
- Robust against typical errors
 - Programming interference
 - Charge leakage

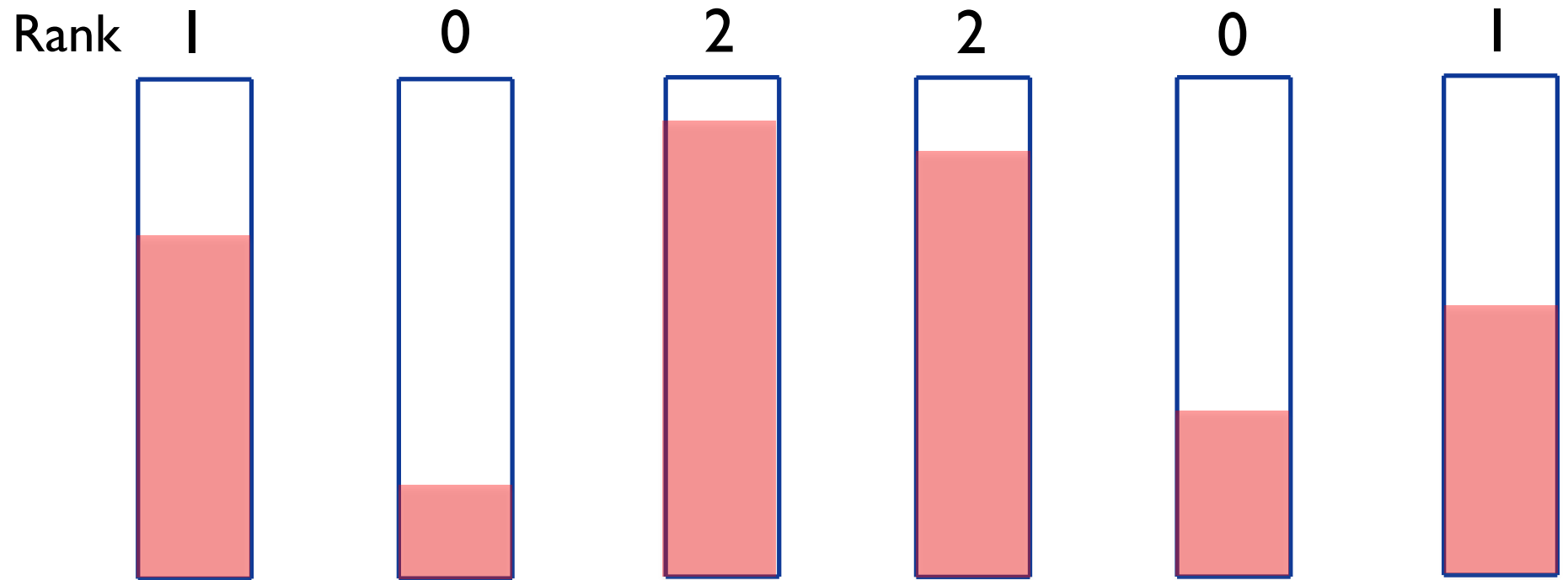


Use Relative Order to store data



A. Jiang, R. Mateescu, M. Schwartz, and J. Bruck, "Rank Modulation for Flash Memories," IEEE Transactions on Information Theory, vol.55, no.6, pp.2659-2673, June 2009

More Cells in Each Rank for Higher Storage Capacity



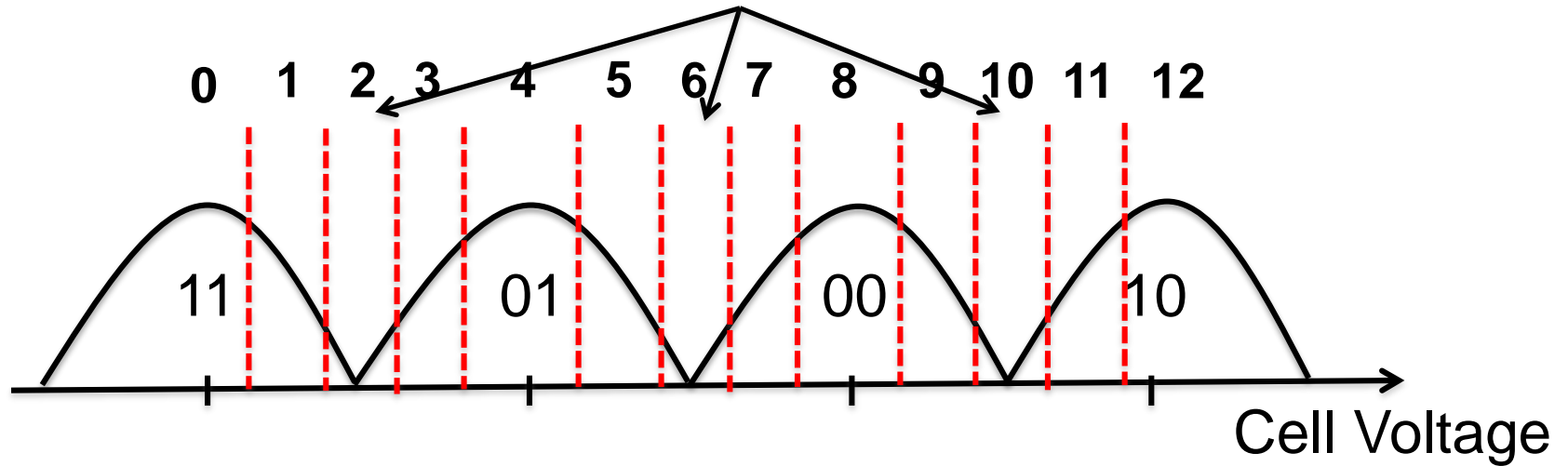
Example: 3 Ranks, 2 Cells/Rank

E. En Gad, A. Jiang and J. Bruck, "Trade-offs between Instantaneous and Total Capacity in Multi-Cell Flash Memories," ISIT 2012.



Rank Modulation in MLC

Reference threshold voltages provided by read-retry



Location	0	1	4	5	8	9	12	12
Rank	0	0	1	1	2	2	3	3

Example: 8 cells, 4 ranks

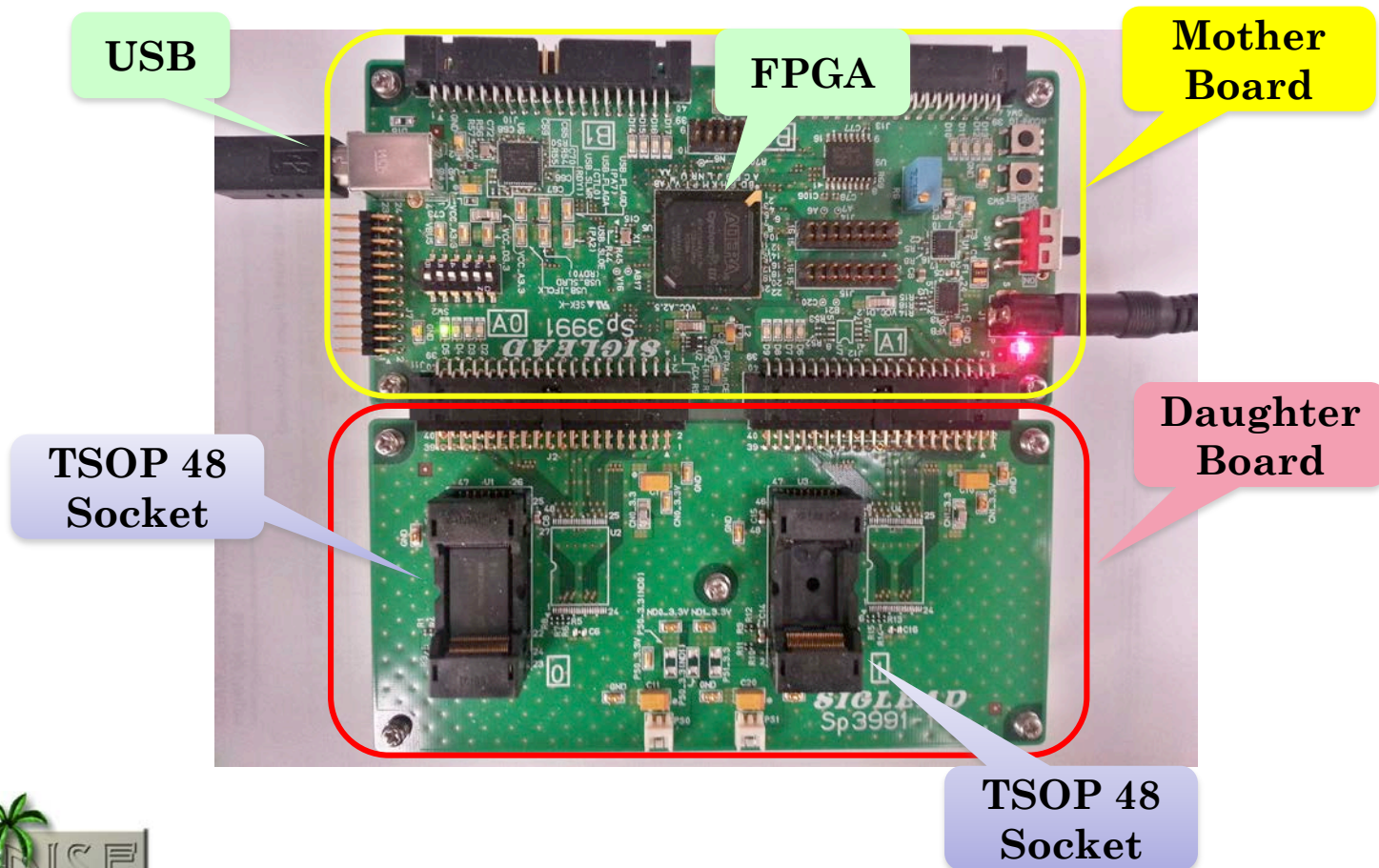
A
B
C
D
E
F
G
H
 (0, 1, 0, 3, 2, 2, 1, 3)

Input Rank
Modulation Code

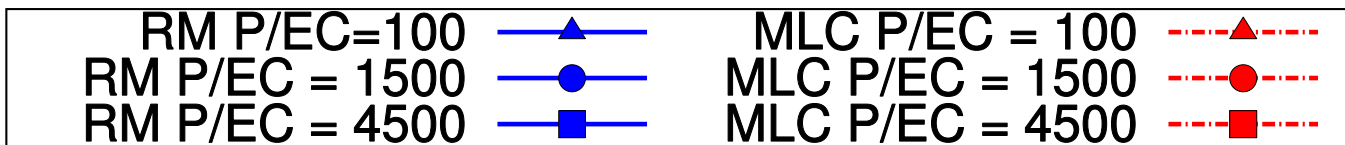
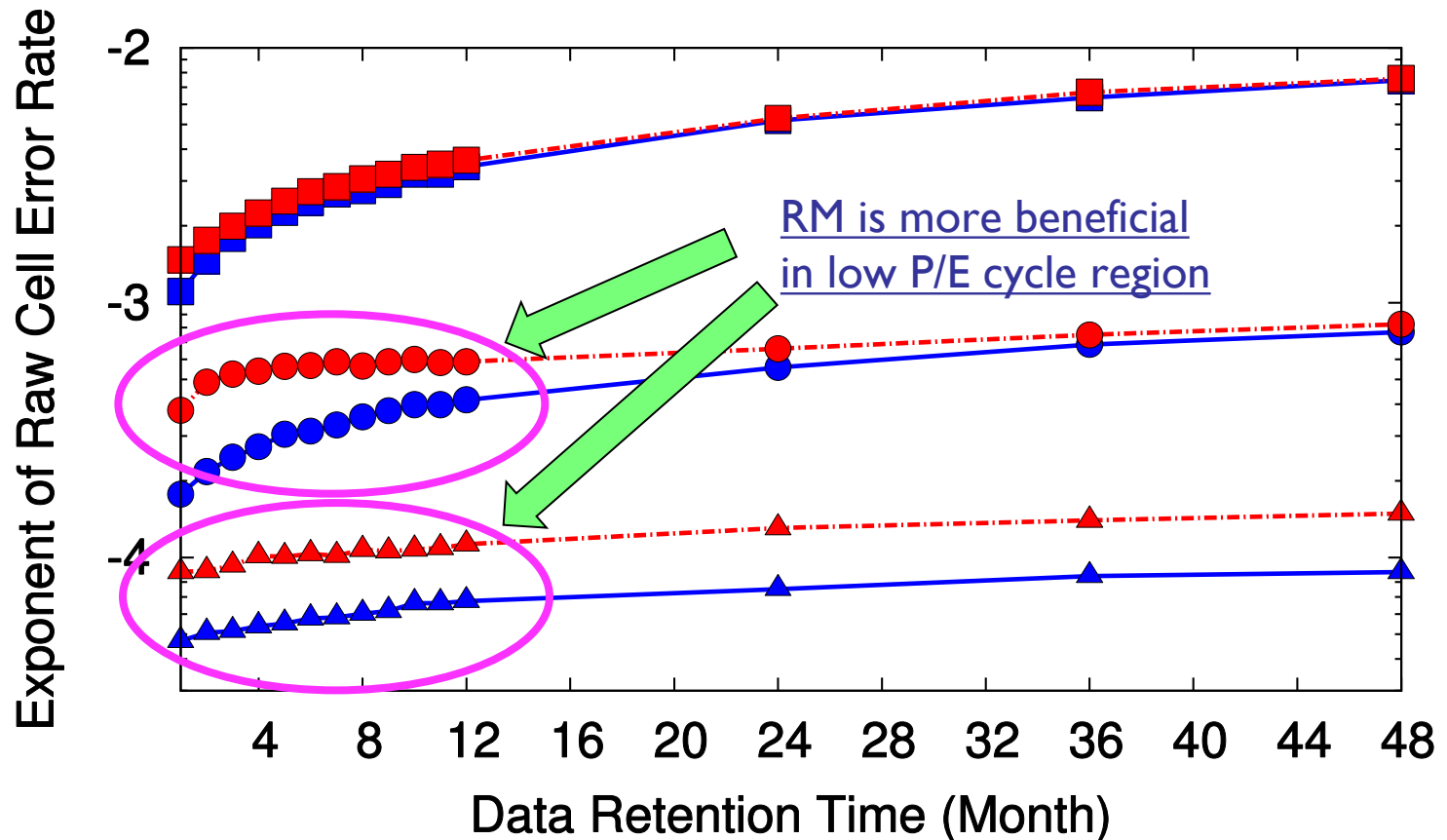


NAND Flash Tester

- SigNAS-II
 - FPGA based tester made by Siglead Inc. (Japan)



How often do cells' voltage order switch?



Flash-based Archival Storage

- Archival data
 - “Write-once read-never”
 - Long data retention time (> 100 years)
 - High reliability (UBER < 1e-15)
- Archival storage using flash
 - Pros
 - random access, efficient data dedup, low power
 - save more on the cost of cooling, power, and form factors than HDD-based archival system[1]
 - No mechanical parts
 - Cons
 - Expensive (but price is decreasing rapidly!)
 - Not reliable
 - Flash only needs to survive small number of P/E cycles.

[1] P. Gupta *et al.*, “An economic perspective of disk vs. flash media in archival storage,” in *Proceedings of the 22th IEEE International Symposium on Modeling, Analysis, and Simulation of Computer and Telecommunication Systems*, Sep. 2014.



Solution: Rank Modulation + Memory Scrubbing

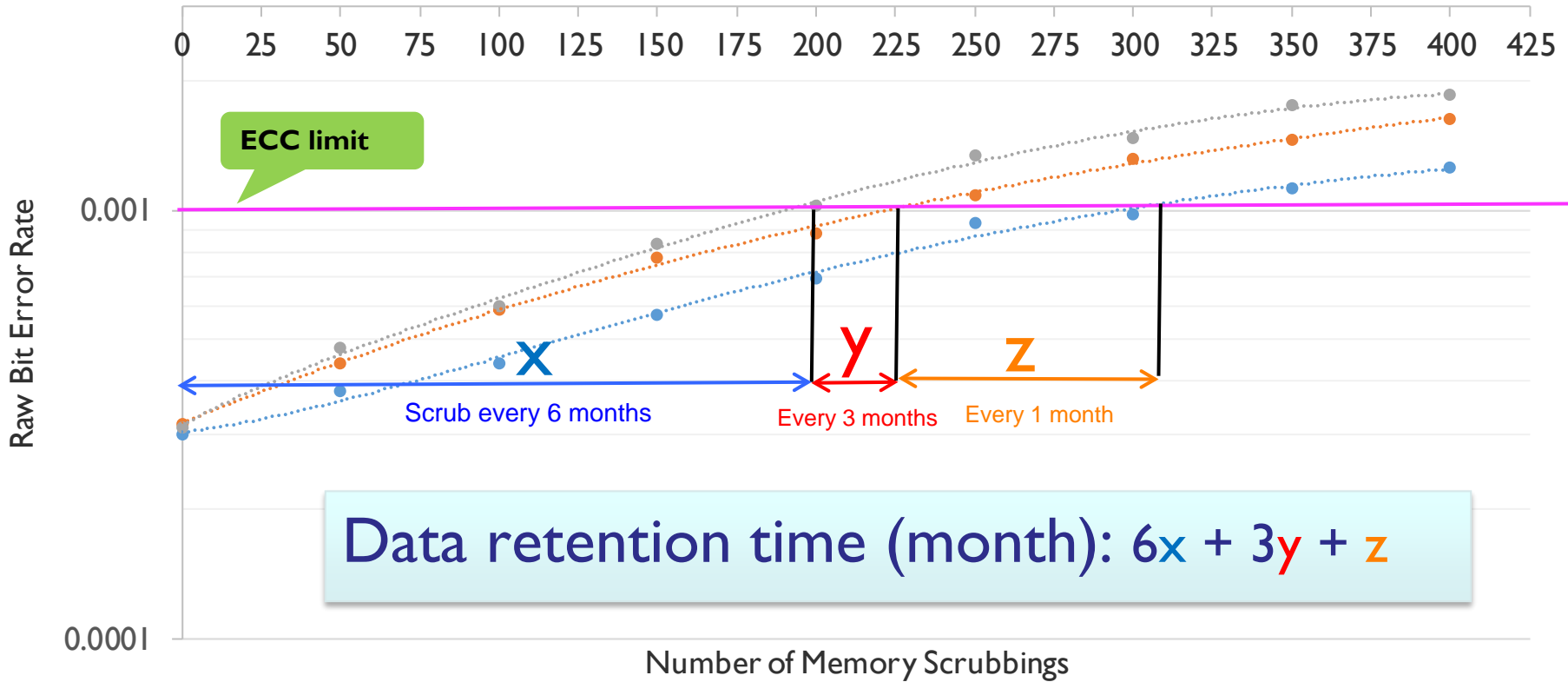
- Our flash-based archival storage solution uses
 - Rank modulation to store data
 - Memory scrubbing to refresh data
 - Scrubbing frequency is adaptive [2]
 - Low-cost ECC
 - Easy to implement, e.g., BCH
 - High code rate (~ 0.9)
 - Shorter code length ($\sim 200\text{b} - 1\text{Kb}$)
 - Very low decoding and encoding complexity
 - suitable for software implementation
 - High density flash (e.g. TLC)



[2] Y. Cai *et al.*, “Flash Correct-and-Refresh: Retention Aware Error Management for Increased Flash Memory Lifetime,” ICCD 2012.

Data Retention Performance on 1x nm TLC

Rank Modulation, N = 1024

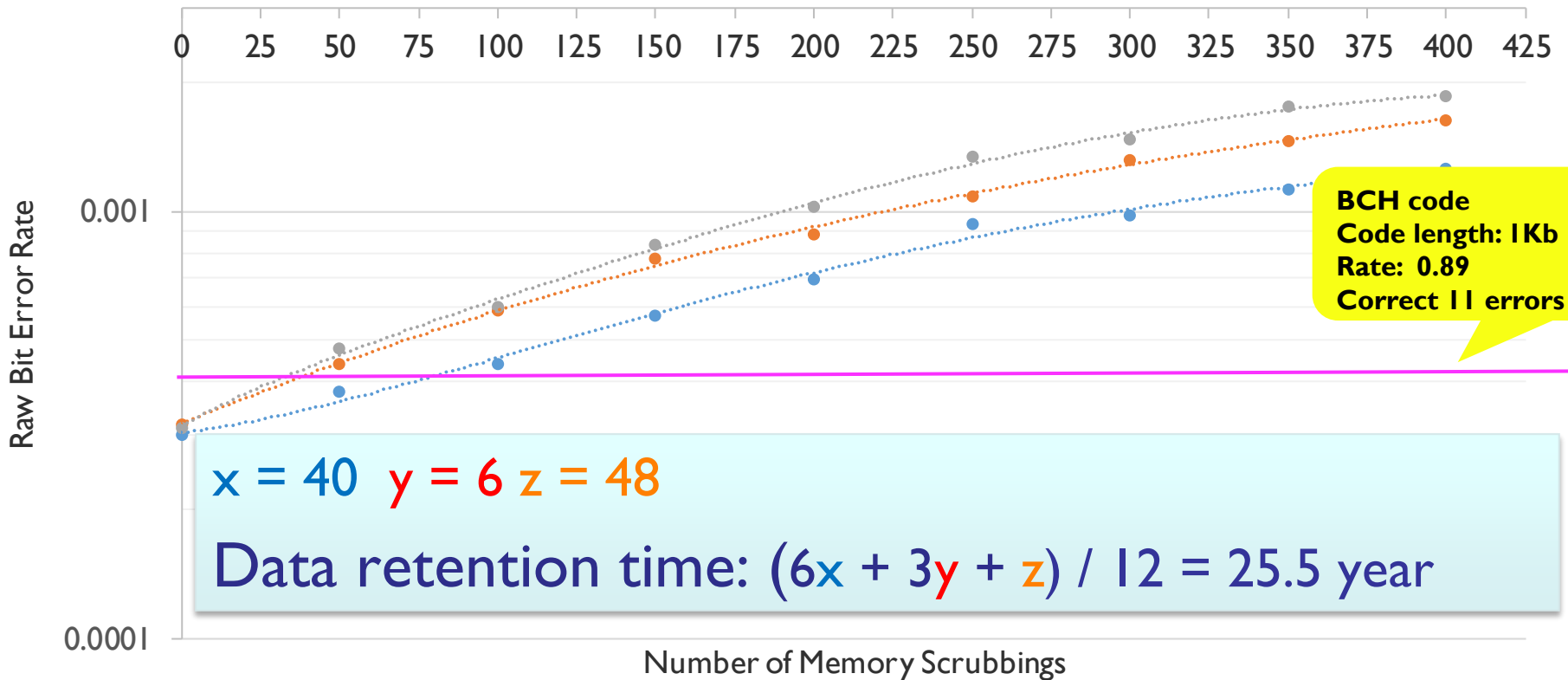


- RM-1024-1Month ● RM-1024-3Month ● RM-1024-6Month
- Poly. (RM-1024-1Month) Poly. (RM-1024-3Month) Poly. (RM-1024-6Month)



Data Retention Performance on 1x nm TLC

Rank Modulation, N = 1024



$$x = 40 \quad y = 6 \quad z = 48$$

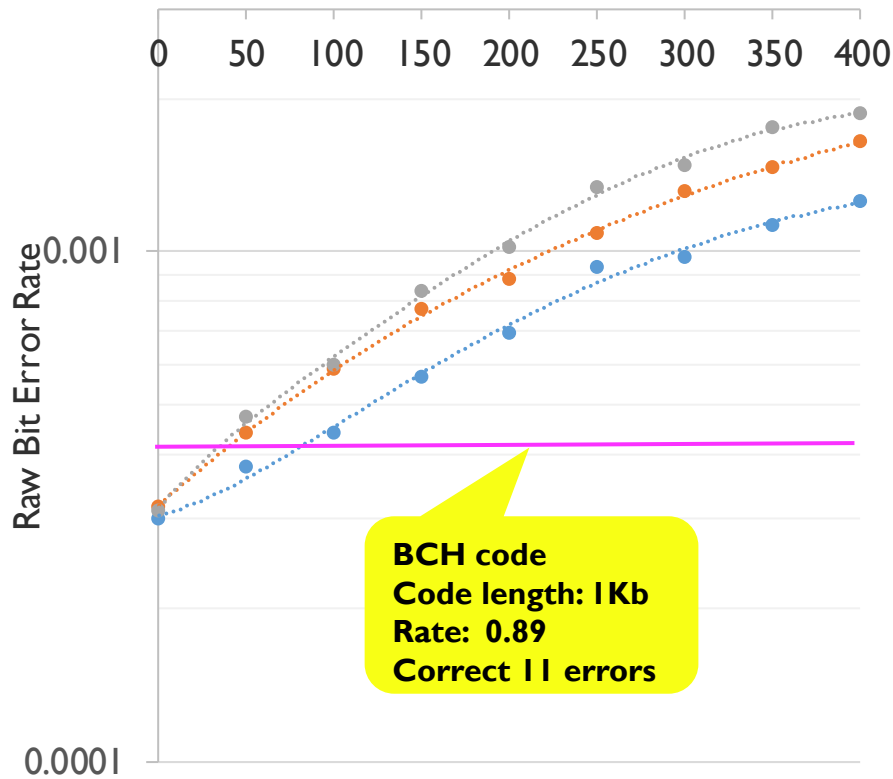
$$\text{Data retention time: } (6x + 3y + z) / 12 = 25.5 \text{ year}$$

- RM-1024-1Month ● RM-1024-3Month ● RM-1024-6Month
- Poly. (RM-1024-1Month) Poly. (RM-1024-3Month) Poly. (RM-1024-6Month)



Comparison based on Same Coding Redundancy

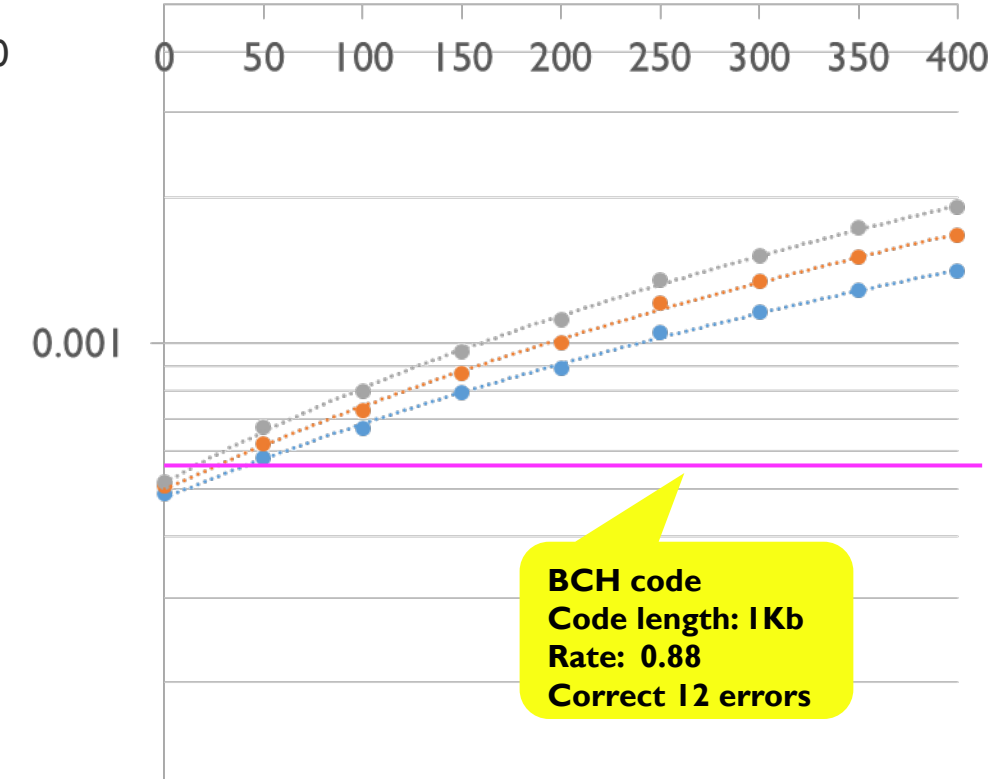
Rank Modulation, N = 1024



Number of Memory Scrubbings

- RM-1024-1Month
- RM-1024-3Month
- RM-1024-6Month
- Poly. (RM-1024-1Month)
- Poly. (RM-1024-3Month)

TLC with Retry



- 1 Month
- 3 Months
- 6 Months
- Poly. (1 Month)
- Poly. (3 Months)
- Poly. (6 Months)

25.5 years

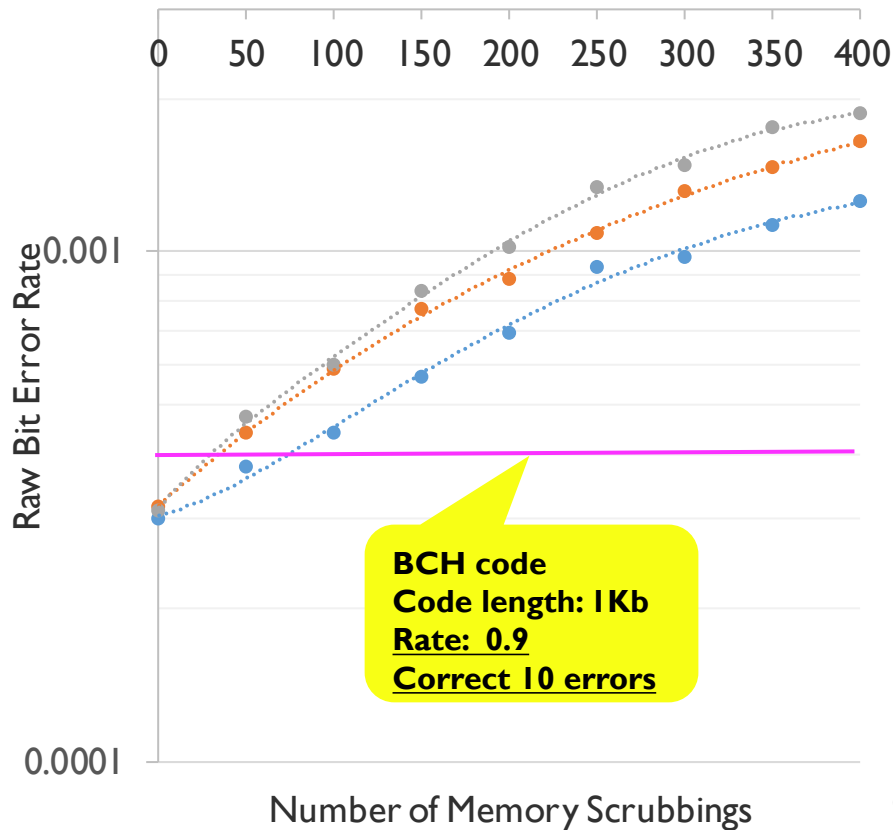
← 2x

12.5 years

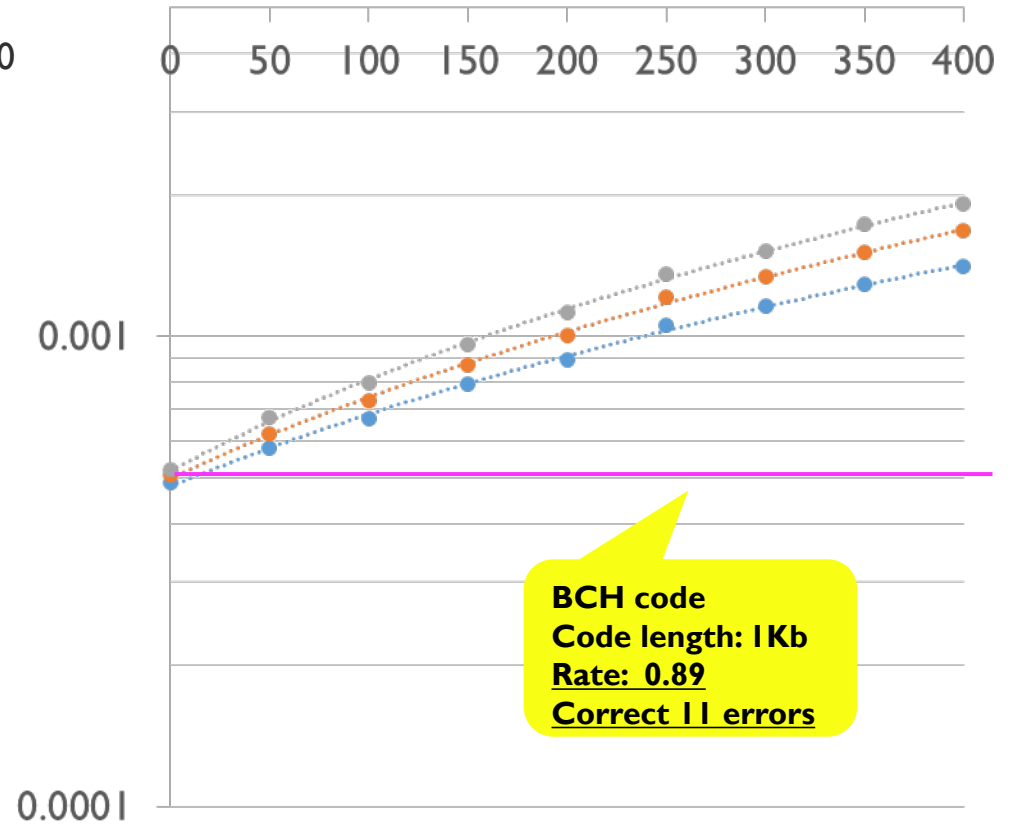


Comparison based on Same Coding Redundancy (2)

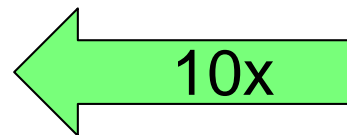
Rank Modulation, N = 1024



TLC with Retry



12.7 years



1.2 years



Summary

- Rank modulation can be implemented
 - in software using read-retry of the current NAND
 - (more efficiently) by slightly revising the current NAND architecture [3]
- [3] Y. Li *et al.*, “Implementing rank modulation,” NVMW 2015.
- Rank modulation provides
 - Significantly lower error rates in low P/E cycle region
 - Significantly longer (e.g. 10x more) data retention time for archival storage
 - Rank modulation has been tested on the chips of various vendors
 - 1x and 2x nm MLC
 - 1y nm TLC



THANK YOU
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