

Controller Concepts for 1y/1z nm and 3D NAND Flash

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NAND Evolution

- Planar NAND scaling is coming to an end in the sub-20nm process
 - 15nm and 16nm NAND are the latest geometries
- Additional capacity by going from MLC to TLC
 - TLC NAND moving from USB drives to SSDs
- 3D NAND is the scaling path going forward
 - Both MLC and TLC versions have been announced

Challenges for Planar 1y/1z nm NAND

- Disturbance Mechanisms
 - Program/erase cycling, read disturb, retention, cell-to-cell coupling
 - Wider voltage distributions, less margin between distributions
- RBER Variations
 - Between dies, blocks, pages
- New programming algorithms
 - TLC NAND has a 3-step programming algorithm with increased data movement compared to MLC NAND
- Strong ECC and intelligent NAND management needed to achieve SSD-grade endurance, especially for TLC NAND

Trends for 3D NAND

- Scaling path towards 1Tb die capacities
 - Primary approach is addition of more vertical layers: 32 and 48 layers demonstrated so far, may go up to 100 layers
- Somewhat different disturbance mechanism
 - Less cell-to-cell coupling
 - New error paths due to 3D integration
 - Yield more challenging
- New programming mechanism with higher write performance
- Block sizes are likely to increase
- Strong ECC increases endurance compared to planar NAND and enables TLC NAND with MLC-like endurance

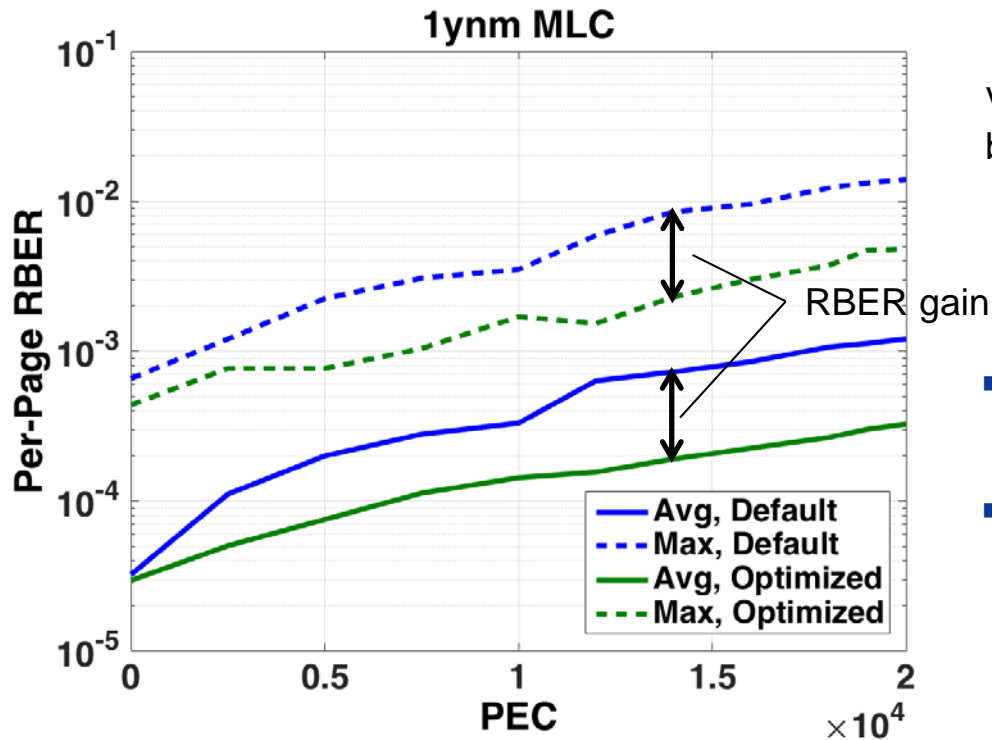
Controller Concepts to Manage 1y/1z and 3D NAND

- Intelligent noise handling
- Multi-level error correction
- Strong ECC: LDPC codes with hard and soft decision decoding
- Multiple and adaptive ECC code rates
- RAISE™

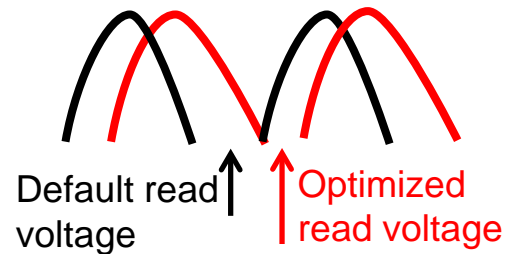
Intelligent Noise Handling

- Deal with noise sources by signal processing or NAND management instead of ECC wherever possible
 - Read disturb handling
 - Read voltage calibration
 - Cancellation of cell-to-cell coupling
- Strike right balance between ECC, recycling and retirement

Pre-Read Optimization: Read Voltage Calibration



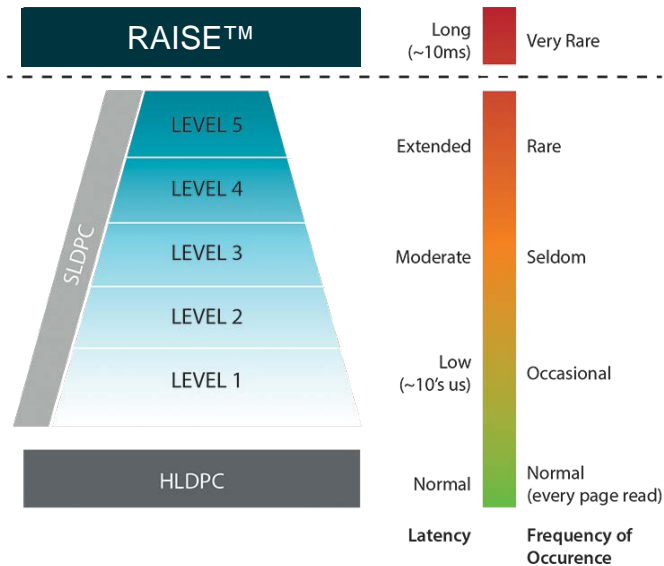
Voltage distributions
before/after cycling:



- Optimizing read voltages reduces retry rate and extends endurance
- Optimum read voltages shift as a function of endurance, retention and read disturb

Multi-Level Error Correction

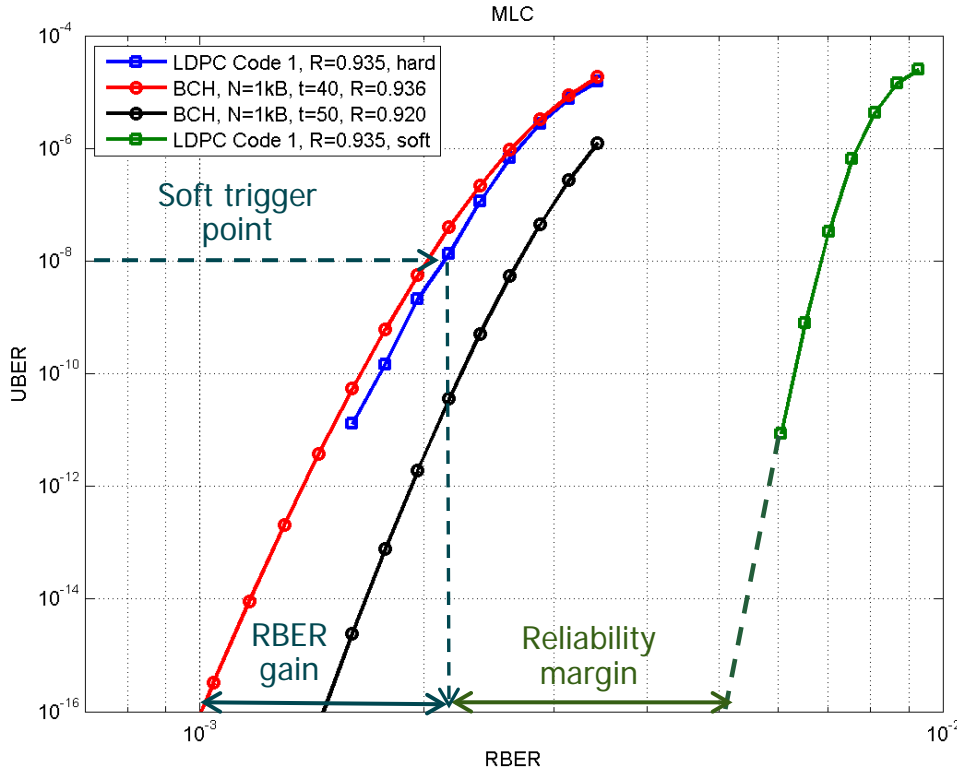
- Hard-decision LDPC decoding is on-the-fly error correction method
- Judiciously apply progressively stronger decoding methods such as soft-decision LDPC decoding and DSP technology only as necessary
- Specialized noise handling techniques for P/E cycling, retention, read disturb, etc.
- Optimize time-to-data



Error Correction Concepts

- Earlier steps in read recovery have high probability of success with low latency in order to minimize time-to-data
 - Hard LDPC followed by soft LDPC followed by RAISE™
- Proactively adjust read voltages to improve RBER
- Eventually recycle data after failures due to retention or read disturb
- Apply stronger code rate for failures due to flash wear
- Foreground tasks
 - Hard and soft LDPC decoding
 - RAISE™
- Background tasks
 - Pre-read optimization
 - Read disturb handling
 - Code rate adjustment

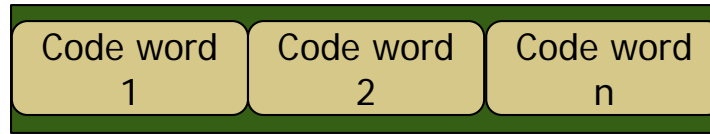
Hard/Soft LDPC vs. BCH Capability



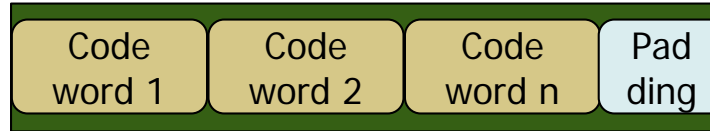
- Target code word failure rate for hard decoding is low
- Hard decoding failure rate defines trigger point for soft decoding
- Impact of soft decoding to read performance is low
- Hard LDPC error rate determines on-the-fly RBER capability
- Soft LDPC error rate guarantees reliability at target UBER
- Hard + infrequent soft LDPC decoding provides significant RBER gain over BCH

Multiple Code Rates and Code Rate Granularity

Good code rate granularity:
No or little padding

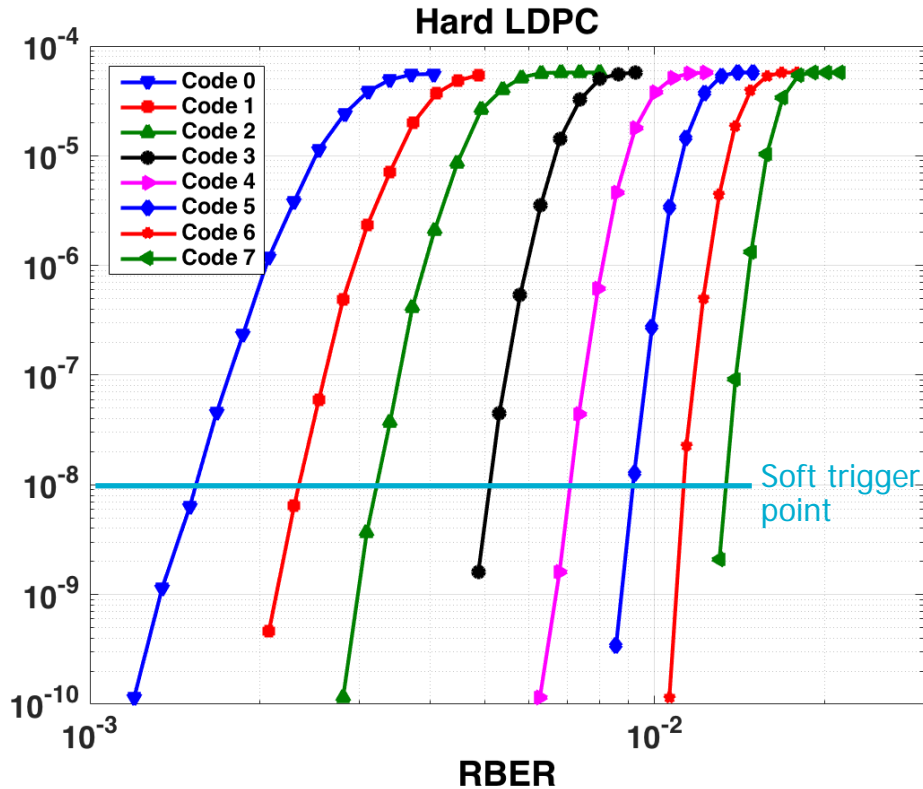


Insufficient code rate granularity:
Significant padding



- ECC requirements vary between flash vendors, geometries, MLC/TLC, planar/3D
- Significant RBER differences across different page types and blocks
- Controller needs capability to support multiple codes simultaneously with sufficient code rate granularity
- Parameters:
 - User data and parity length determine code rate = correction strength
 - Codeword length and number of codewords per physical flash page determine padding = format efficiency

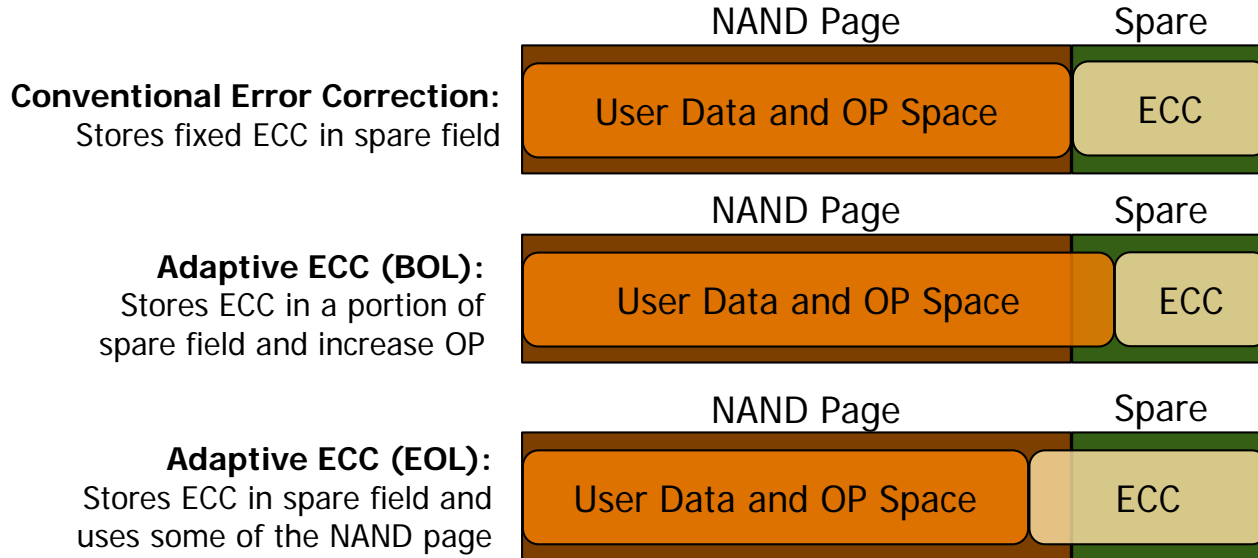
Switching Code Rates



- Multiple LDPC codes cover wide RBER range
- As NAND flash ages, controller switches to the next stronger code
- Read performance improves, since stronger LDPC codes converge faster

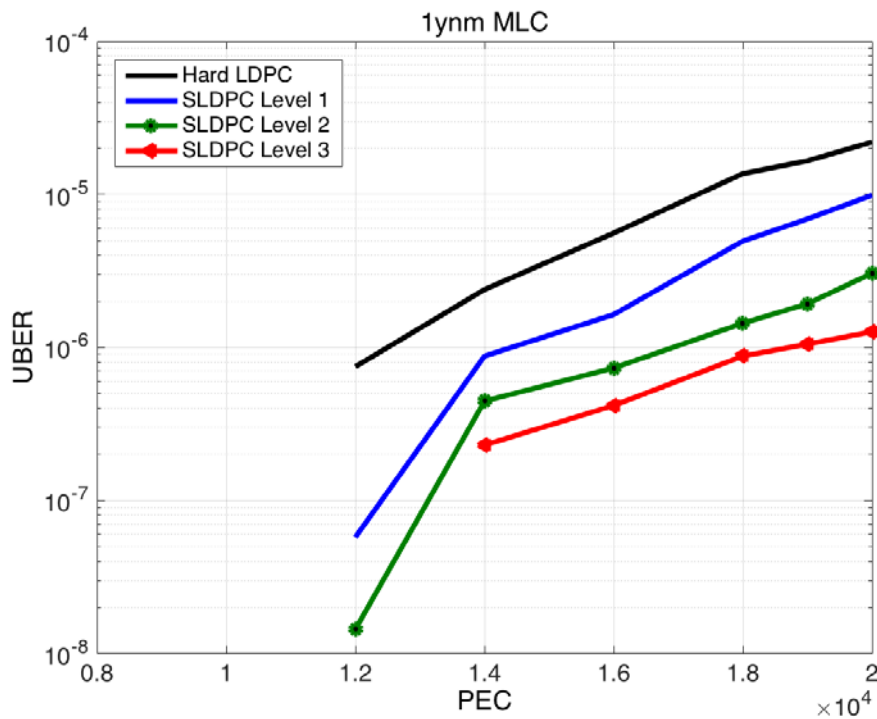
Adaptive Code Rates

- Flash at beginning of life (BOL) is more robust, requires less ECC: use more free space for overprovisioning and increase performance
- As drive reaches end of life (EOL), increase ECC to maintain readability and increase endurance beyond NAND spec

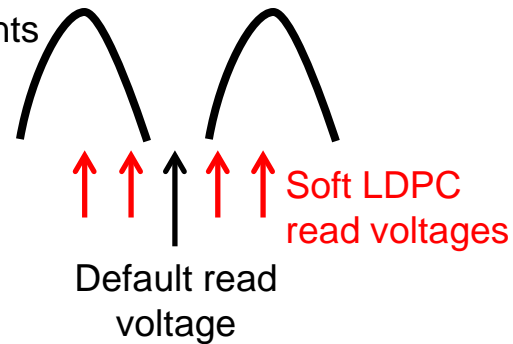


Adaptive ECC allows for more free space @ BOL = Higher Performance

Soft LDPC Levels

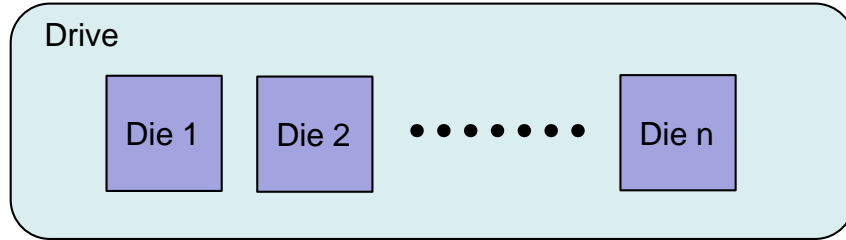


Read voltage placements for soft LDPC:



- Sequence of retries with varying read voltage settings
- Computation of soft information (LLRs) based on multiple read decisions
- Additional signal processing increases reliability

RAISE™: Redundant Array of Independent Silicon Elements



- RAID-like data protection within the drive
- Writes data across multiple dies
- Corrects full page, block or die failures when all SLDPC levels fail

Conclusion

- Latest memory geometries demand intelligent NAND management features
- 3D NAND will still rely on strong ECC and advanced NAND management features to enable high endurance and to make TLC mainstream for SSD applications

Thank You! Questions?



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