Extending NAND Endurance with Advanced Controller Technology

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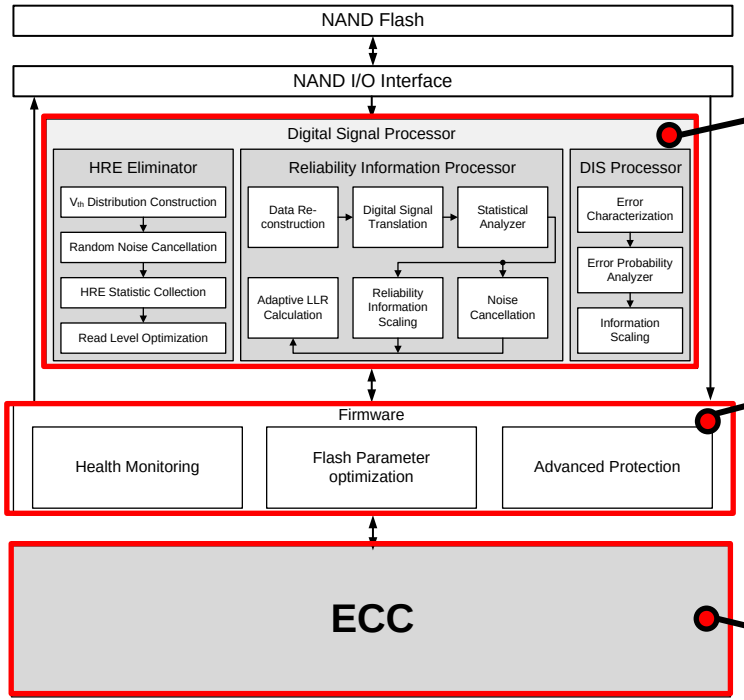
Error Handling Tech. in Controller



- **Digital Signal Processors:**
  - Reduce Error.
  - Collect/transfer the channel info.
- **Firmware:**
  - Judge the info. form DSP/ECC.
  - Adaptively control ECC engine.
  - Adaptively control NAND Flash.
  - Adaptively change the data Structure.
- **ECC Engine:**
  - Low Power.
  - Low Cost.
  - Excellent Correction Strength.

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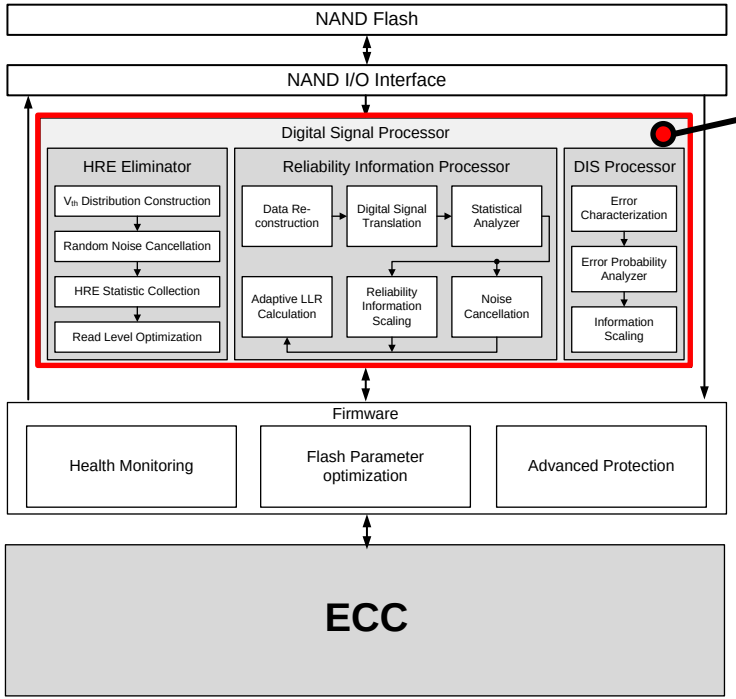
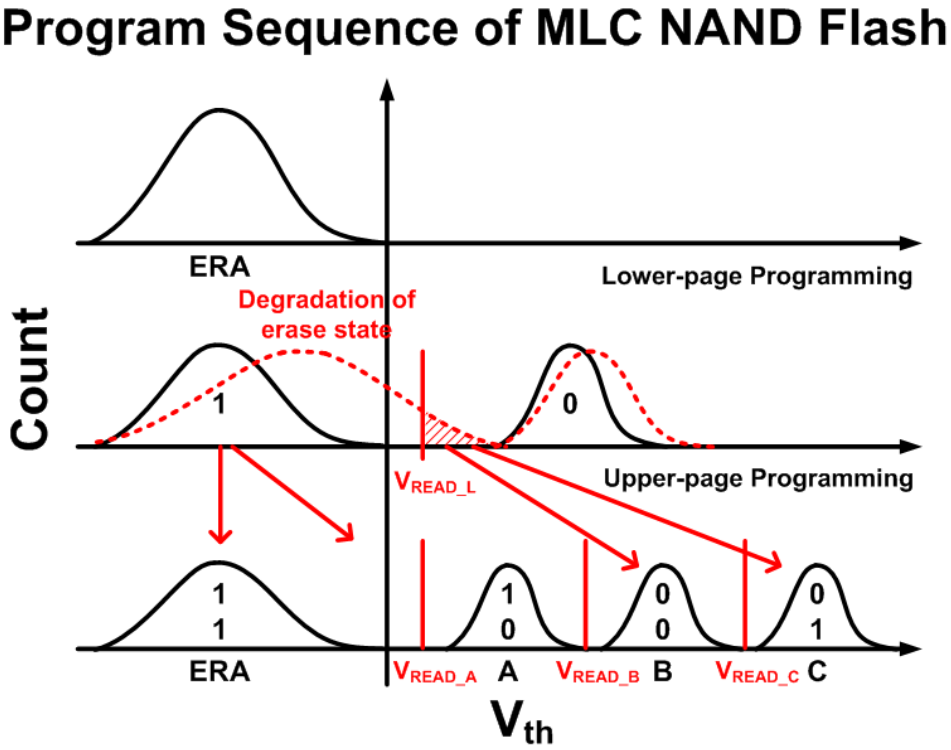


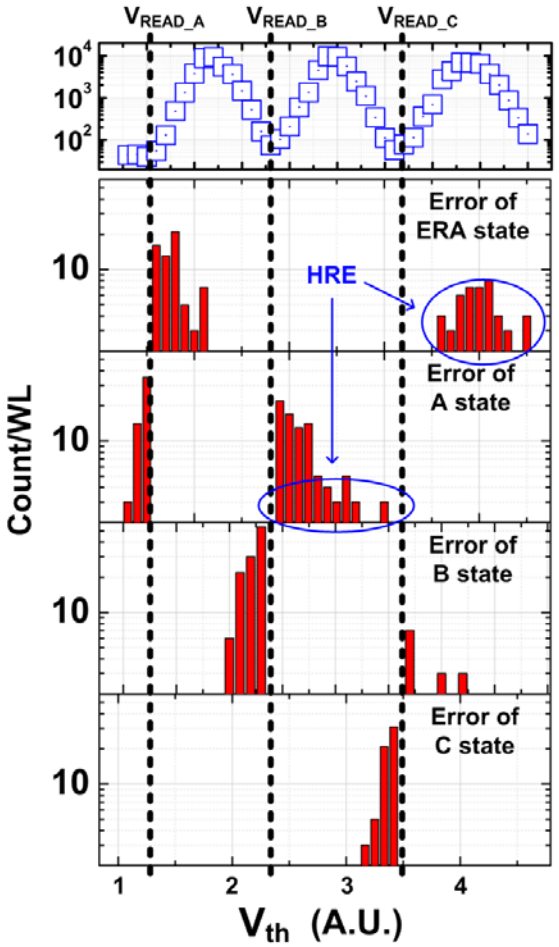
- **Digital Signal Processors:**
  - **Reduce Error.**
  - **Collect/transfer the channel info.**

Digital Signal Processor in Controller

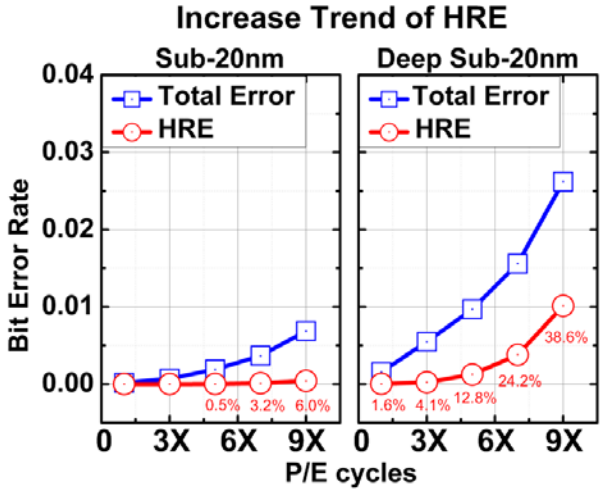
- Monitor the health of the Data.
- Estimate/collect the channel information.
- Convert the channel information to reliability info. for ECC.
- Reduce the input errors (normal errors & HRE).
- Improve the decoding throughput.
- Reduce the complexity of the decoding flow.

What's HRE?

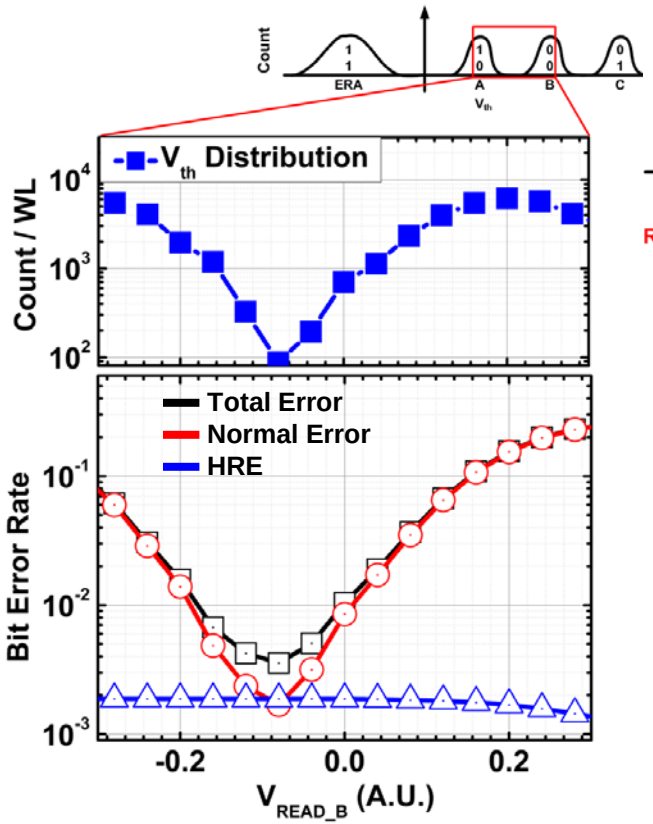

Program Sequence of MLC NAND Flash
Count
ERA
Lower-page Programming
Degradation of erase state
1
0
V_{READ_L}
Upper-page Programming
1 1
1 0
0 0
0 1
ERA
V_{READ_A} A
V_{READ_B} B
V_{READ_C} C
V_{th}


V_{READ_A}
V_{READ_B}
V_{READ_C}
10^4
10^3
10^2
Error of ERA state
HRE
Error of A state
Error of B state
Error of C state
10
Count/WL
1
2
3
4
V_{th} (A.U.)

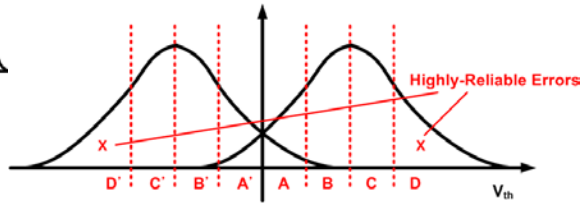
The Impact to the Reliability



BCH

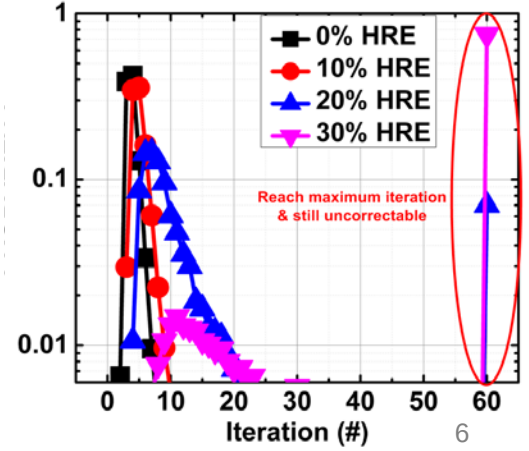


LDPC

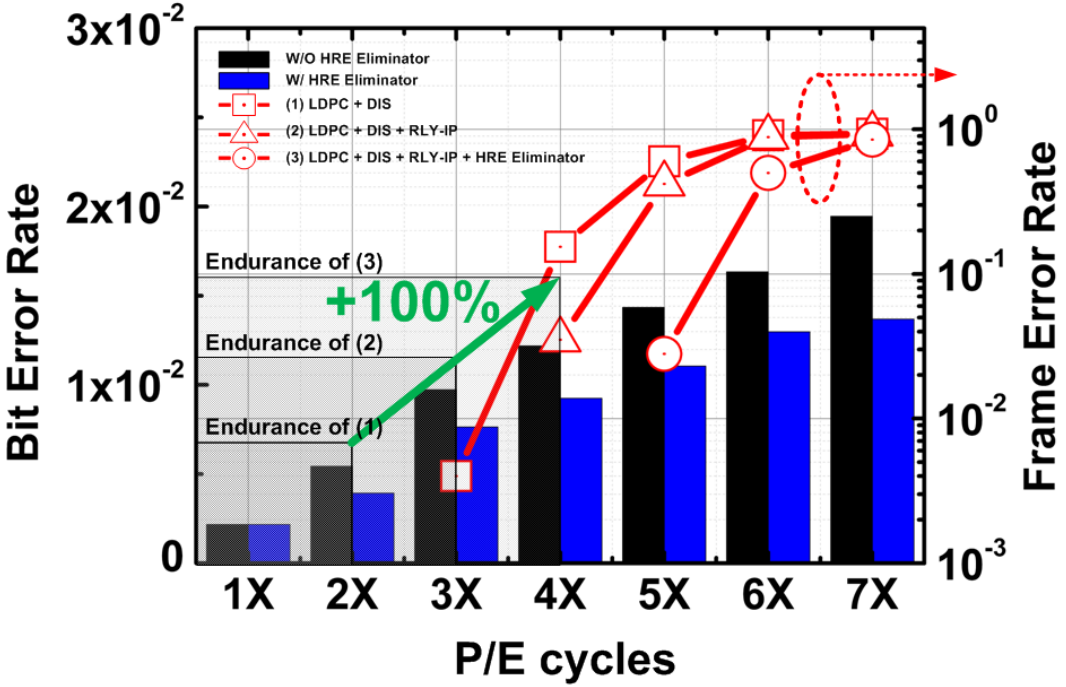


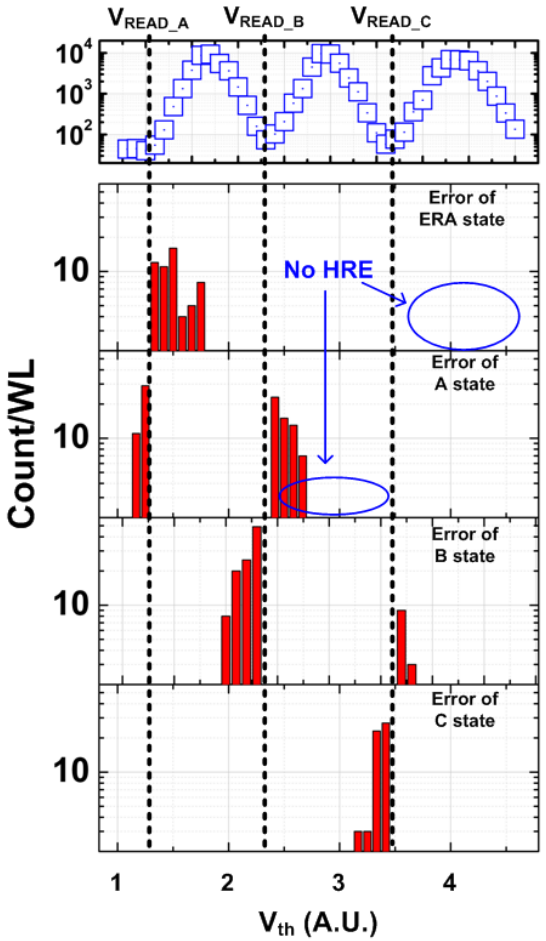
Reliability Information (RLY-I) : | D | > | C | > | B | > | A |

$$\text{RLY-I} = \log \frac{P(x_i=0|y_i)}{P(x_i=1|y_i)}$$



HRE Eliminator





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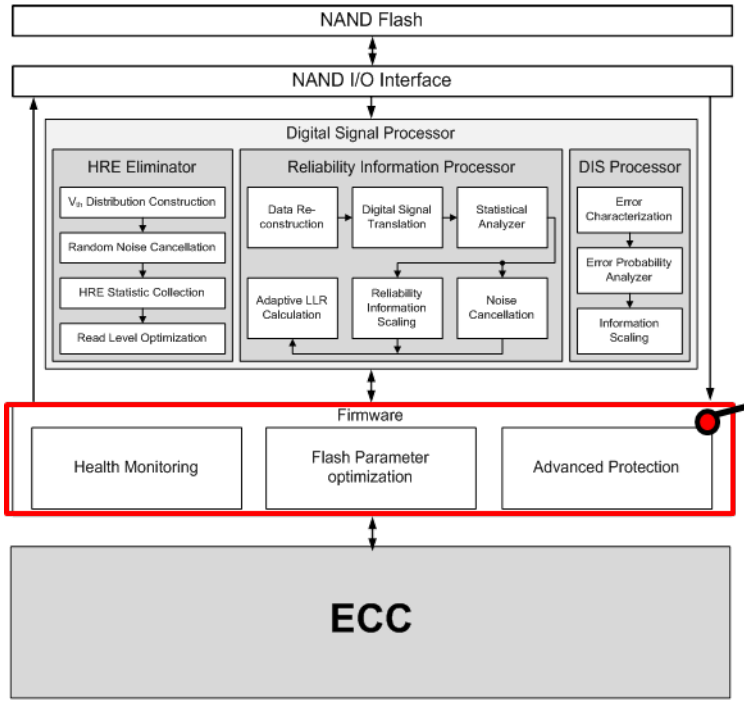

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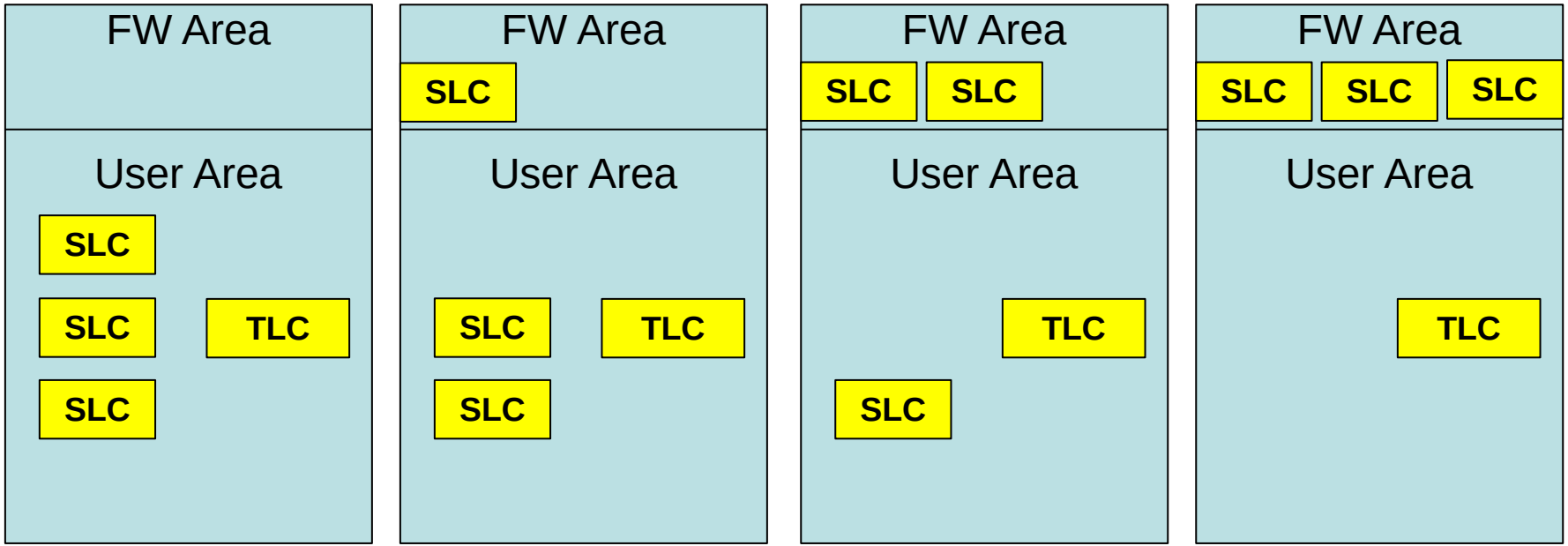
Adaptive Data Structure



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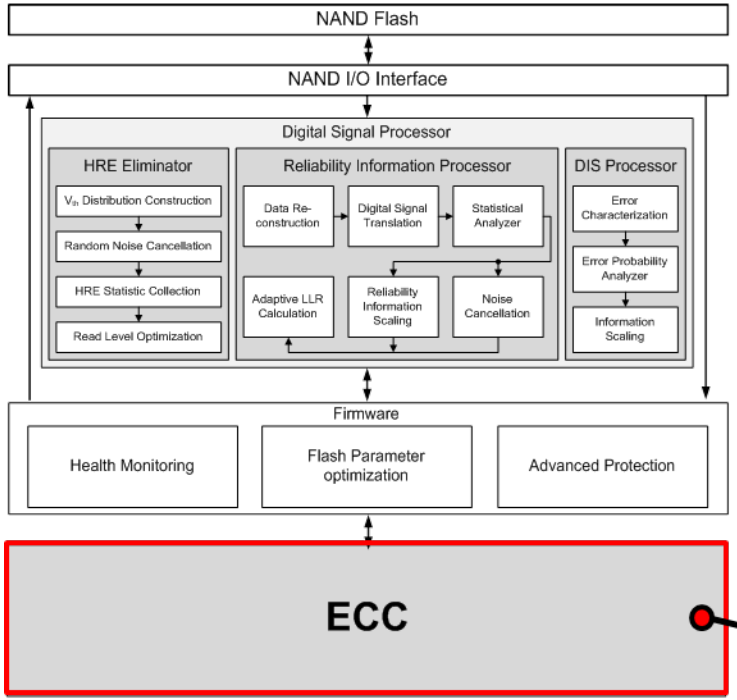

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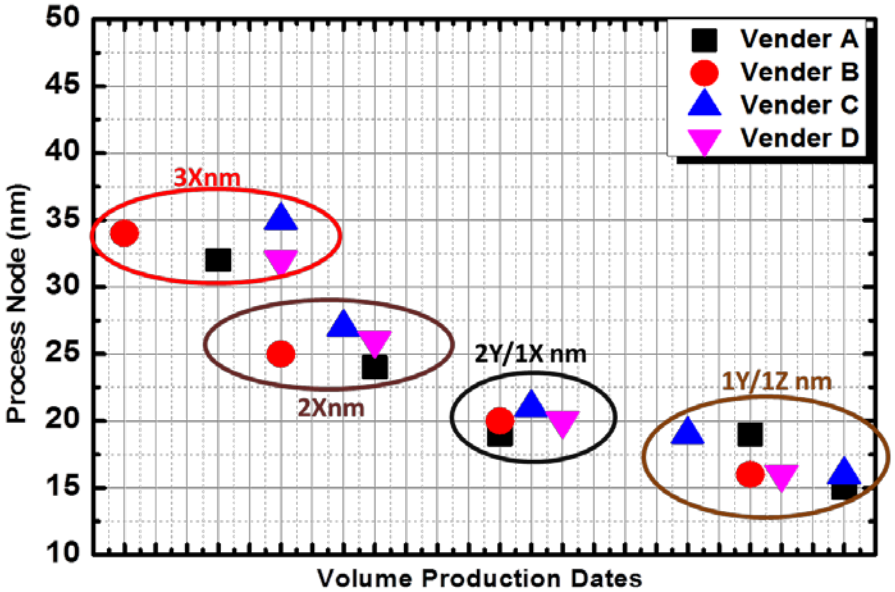
Migration of ECC Technologies



	2009	2010	2011	2012	2013	2014	2015
Technology (nm)	3x	3x	3x/2x	2x/1x	1x/1y	1y/1z	1z
ECC/Signal Processing	BCH	BCH	BCH/Retry	BCH/Retry/LDPC	BCH/Retry/LDPC	Advanced DSP	Advanced DSP

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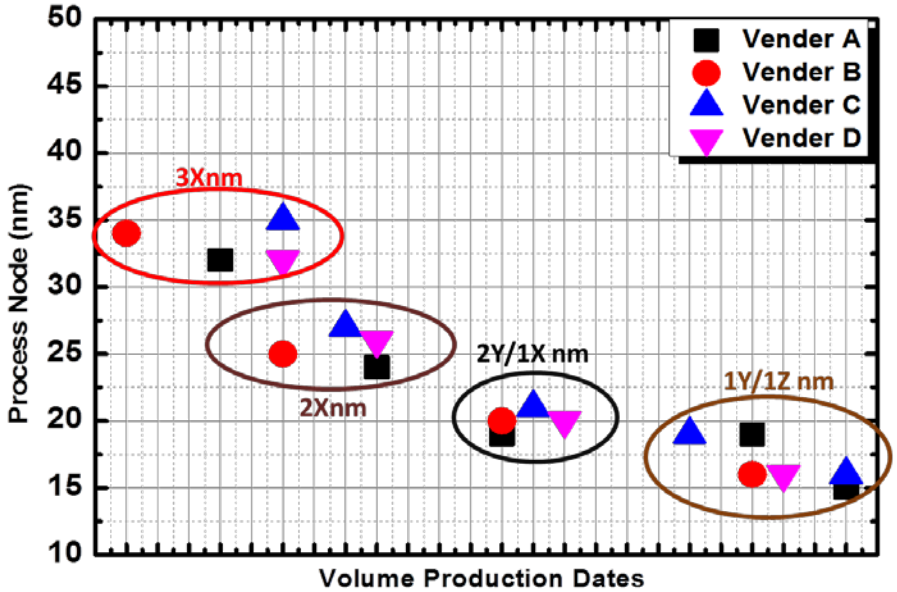

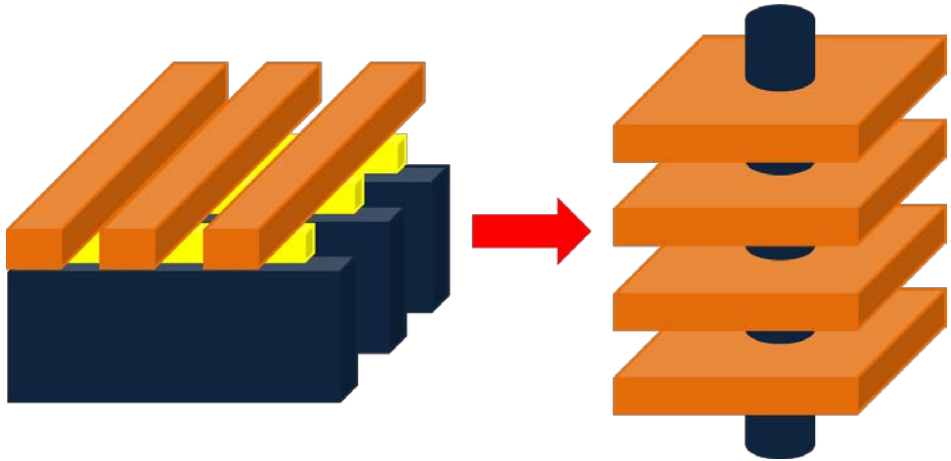

MLC -> TLC -> QLC

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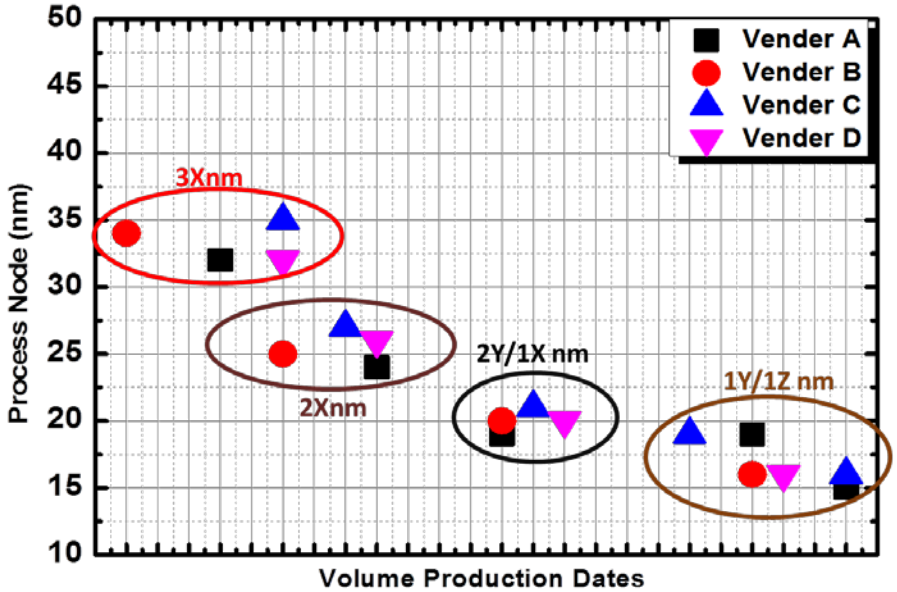

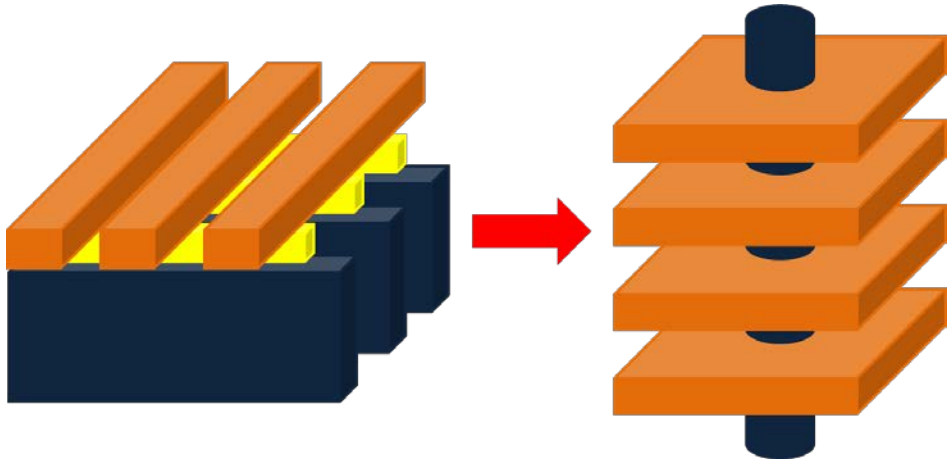

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Even We Changed to LDPC…

- Larger chip size.
- Huge power consumption.
- A Gap between simulation and real NAND channel on Correction capability.
- Weak immunity to HRE.
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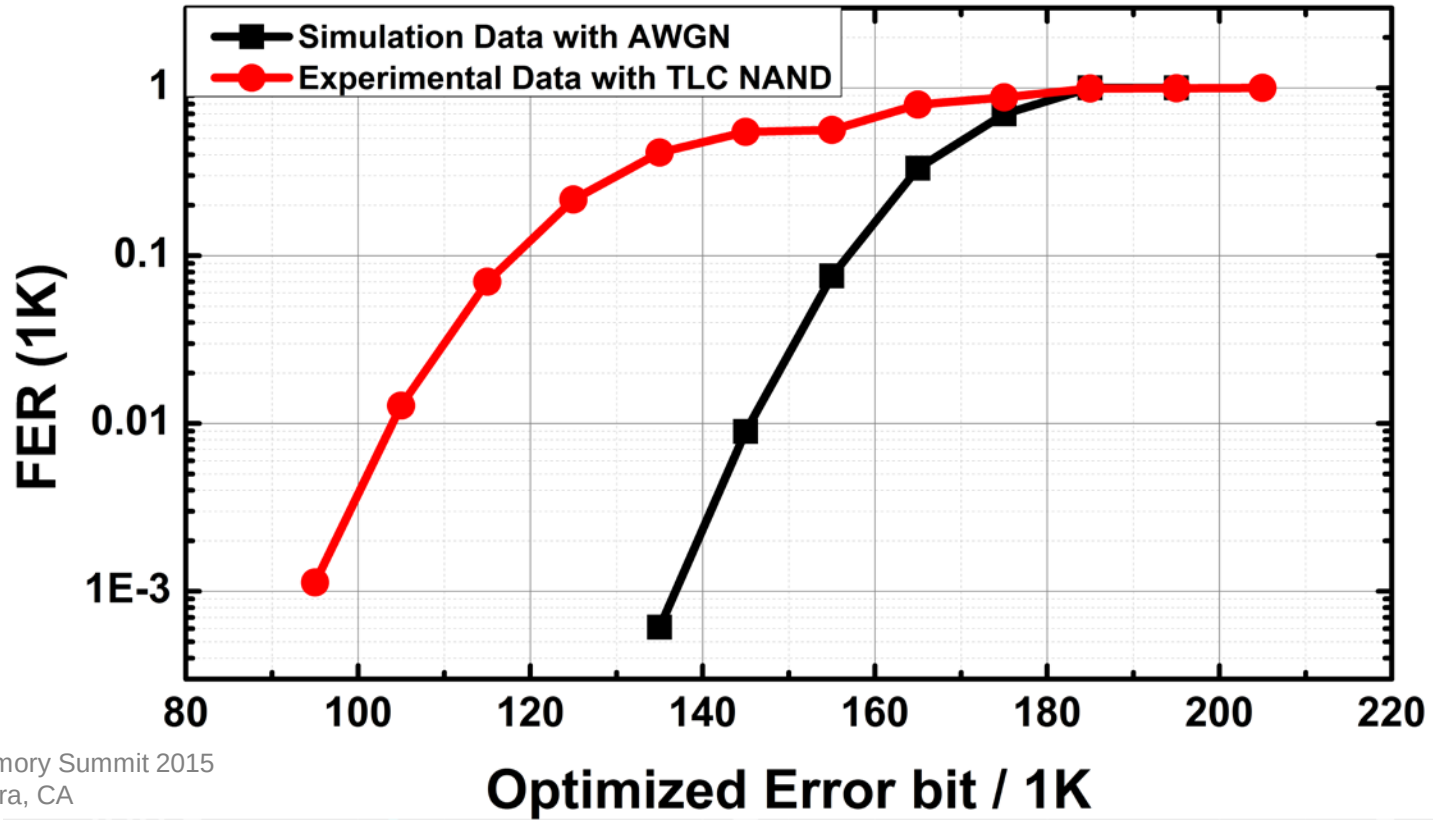
The Gap between NAND and Theory



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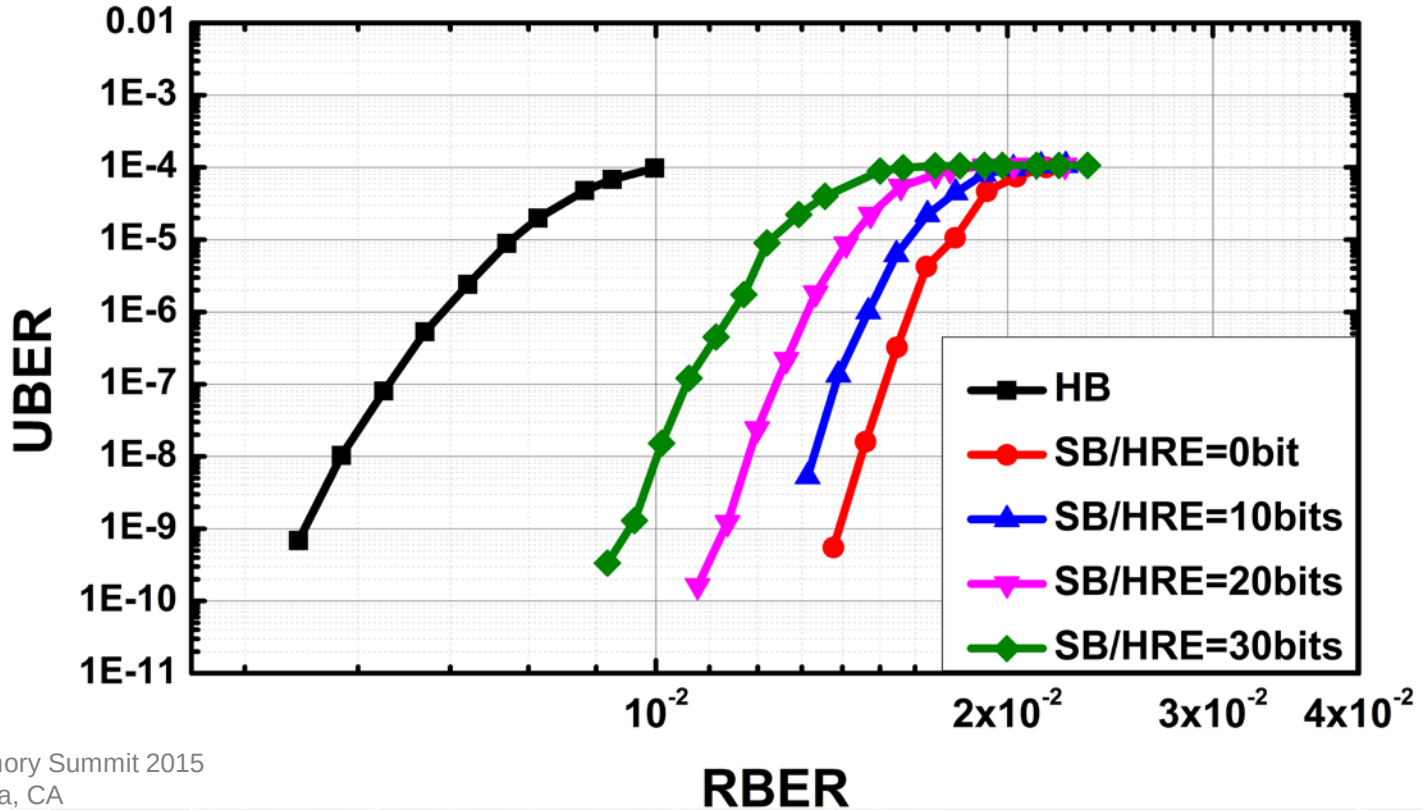
Weak Immunity to HRE



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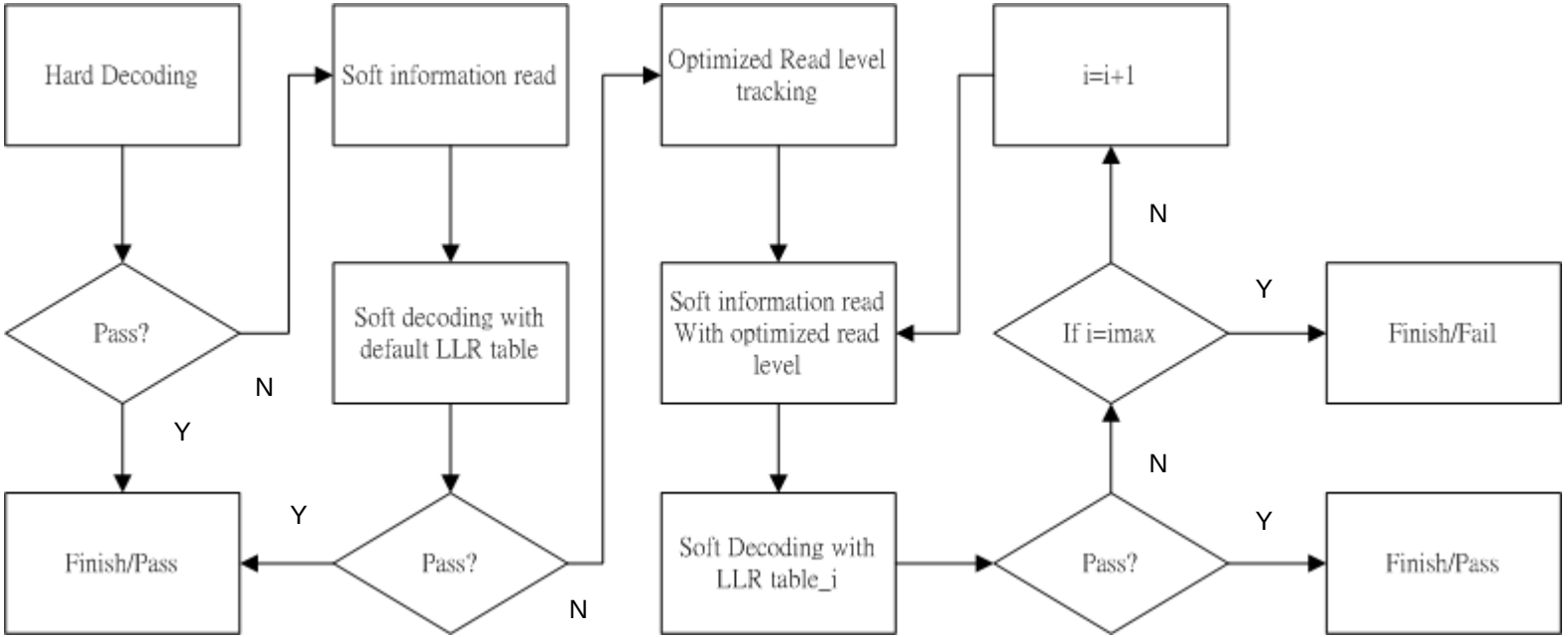
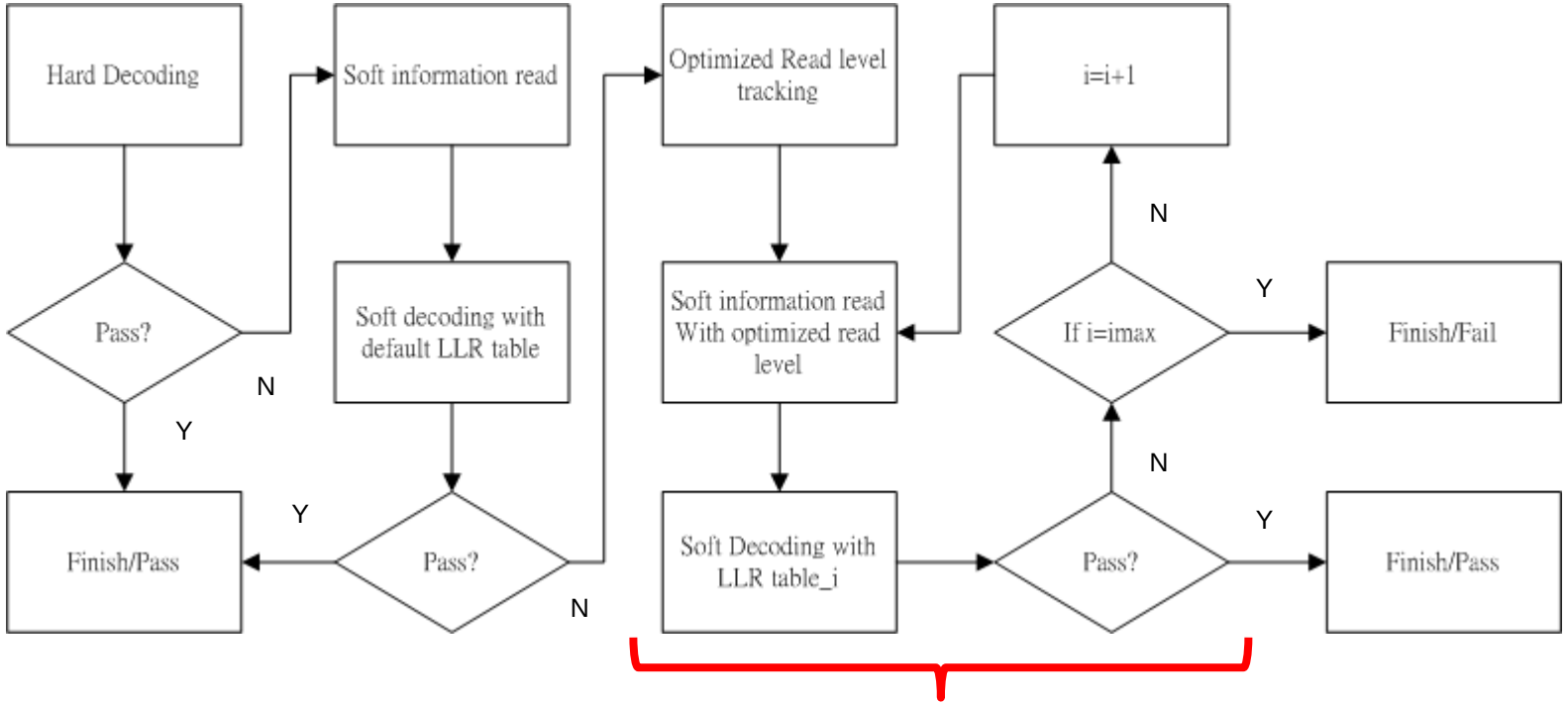


Complex Decoding Flow



A Novel ECC is Proposed

- Superior correction capability then BCH and the HB of LDPC.
- Support soft decoding.
- 1/3 power consumption than BCH.
- Same gate count as BCH.
- Simple decoding flow.
- No need to use soft bit information.
- Excellent HRE immunity.

Summary

- A Novel ECC engine with superior correction capability is proposed for next generation NAND Flash memory.
- Digital signal processors are proposed to improve the system performance and reliability.
- Adaptive controlling technology is implemented to control the DSP/ECC/NAND/Data structure for superior reliability.