“High Radix” LDPC
A Silicon Saving Approach

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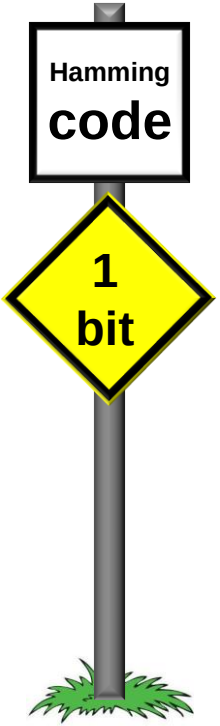
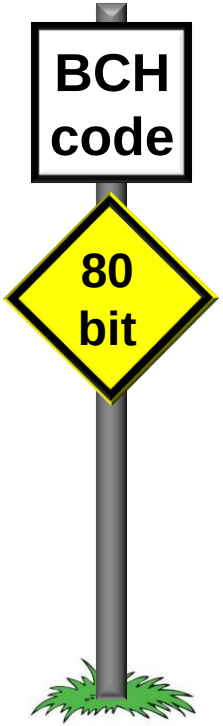
Siglead Europe Limited

ECC for SSD: Where We Started



ECC for SSD: Where We Are Now



ECC for SSD: Where We Go Next

iterative BCH

- theoretical error performance often computable
- cannot be soft decoded
- hard decoding does not require channel information

LDPC code

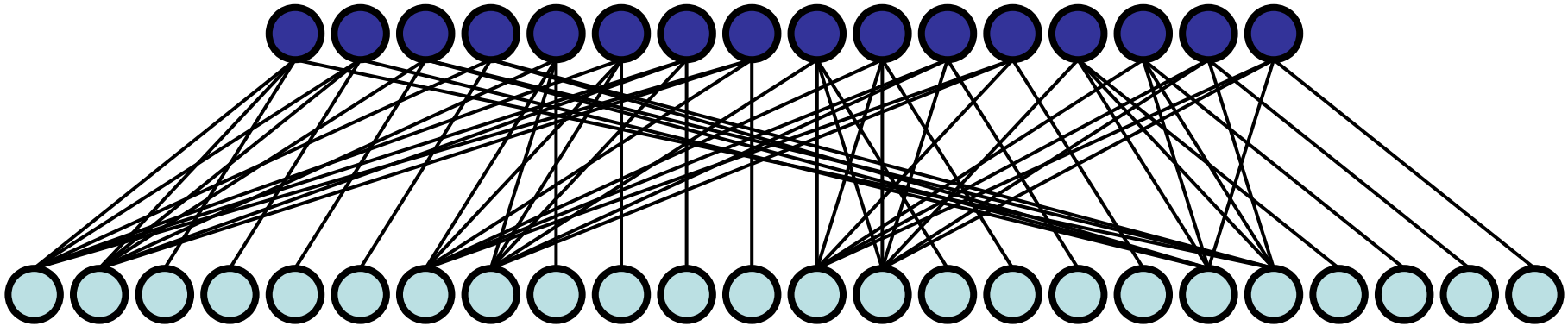
- control/prediction of error floor difficult
- excellent performance under soft decoding
- can we obtain/process soft information?

What is “High Radix” LDPC?

- **replacement for low rate/high correctability BCH code**
  - designed for hard decoding
  - silicon/power budget must be smaller
  - error correction capabilities must be stronger
  - performance must be accurately estimatable
- **linear ECC with sparse edge matrix representation**
- **multi-bit symbols, not bits**
  - not restricted by Galois arithmetic

“High Radix” LDPC: Tanner Graph

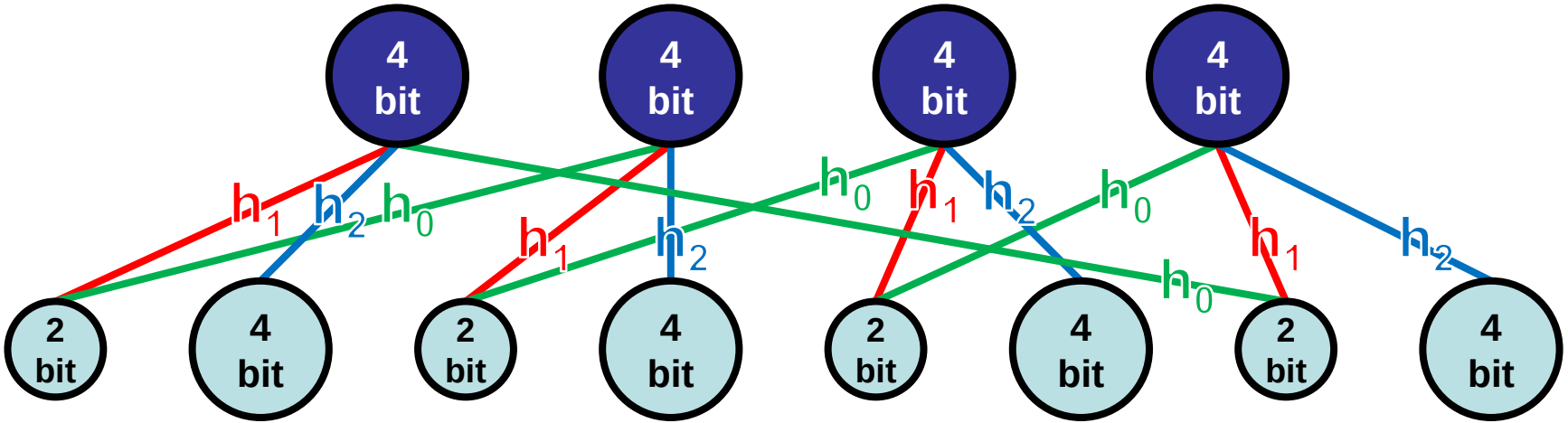
merge variable/check nodes of binary LDPC…



“High Radix” LDPC: Tanner Graph

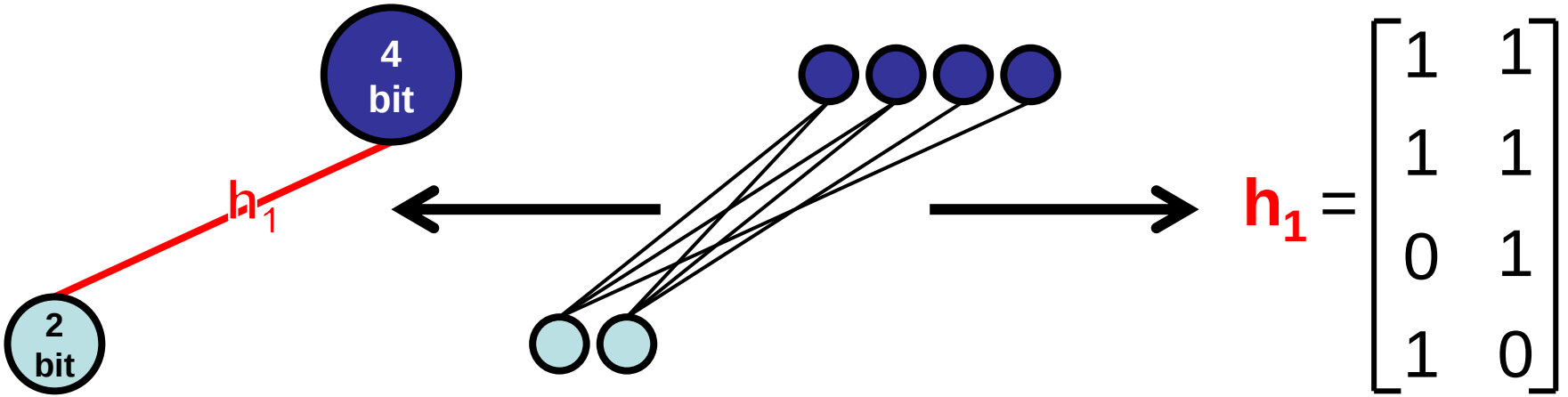
merge variable/check nodes of binary LDPC…

…to get variable/check nodes of symbols + edges labels



“High Radix” LDPC: Edge Matrix

- **edge label is matrix representation of merged edges of binary LDPC**



"High Radix" LDPC Edge Matrix

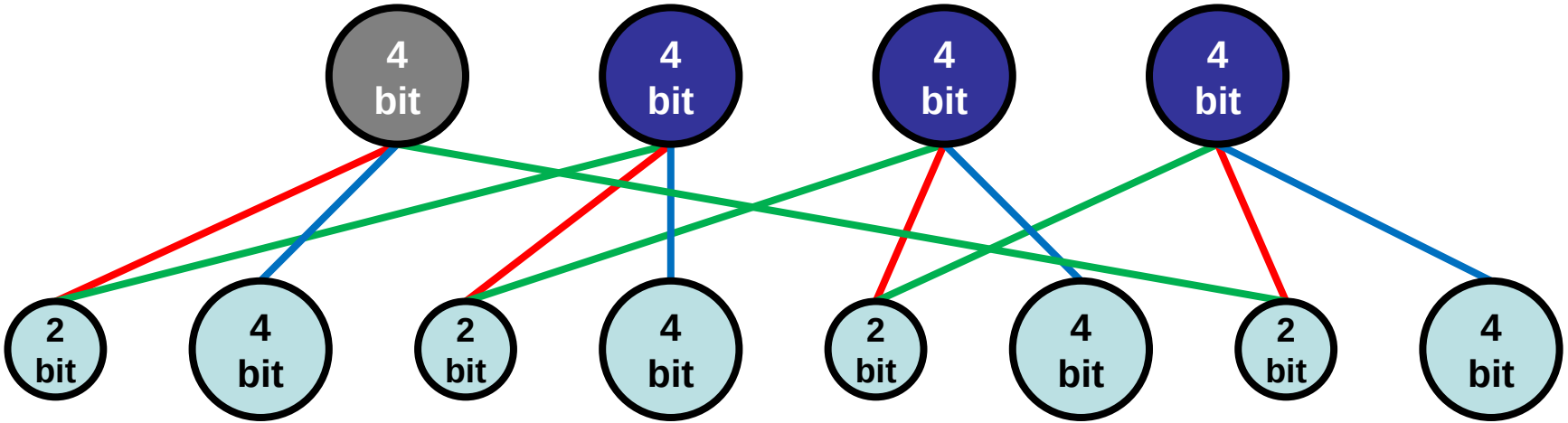
- "High Radix" LDPC edge matrix is a matrix of sub matrices!

$$H = \begin{bmatrix} h_1 & h_2 & 0 & 0 & 0 & 0 & h_0 & 0 \\ h_0 & 0 & h_1 & h_2 & 0 & 0 & 0 & 0 \\ 0 & 0 & h_0 & 0 & h_1 & h_2 & 0 & 0 \\ 0 & 0 & 0 & 0 & h_0 & 0 & h_1 & h_2 \end{bmatrix}$$

where $h_0 = \begin{bmatrix} 0 & 1 \\ 1 & 0 \\ 1 & 1 \\ 1 & 1 \end{bmatrix}$, $h_1 = \begin{bmatrix} 1 & 1 \\ 1 & 1 \\ 0 & 1 \\ 1 & 0 \end{bmatrix}$ and $h_2 = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}$

“High Radix” LDPC: Decoding

- **Cascade decoding**



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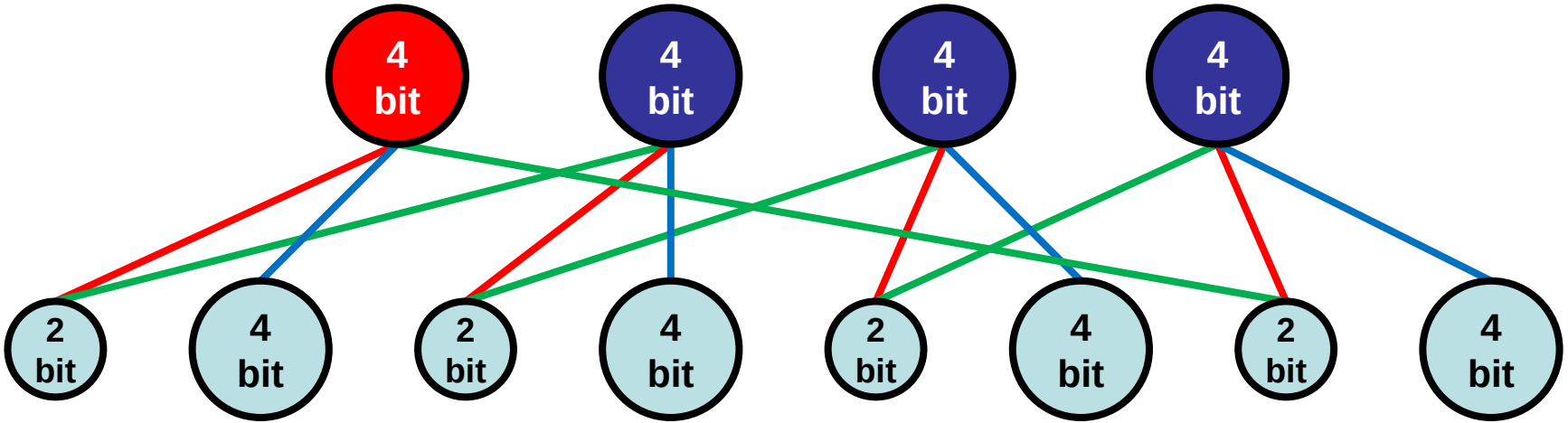

“High Radix” LDPC: Decoding

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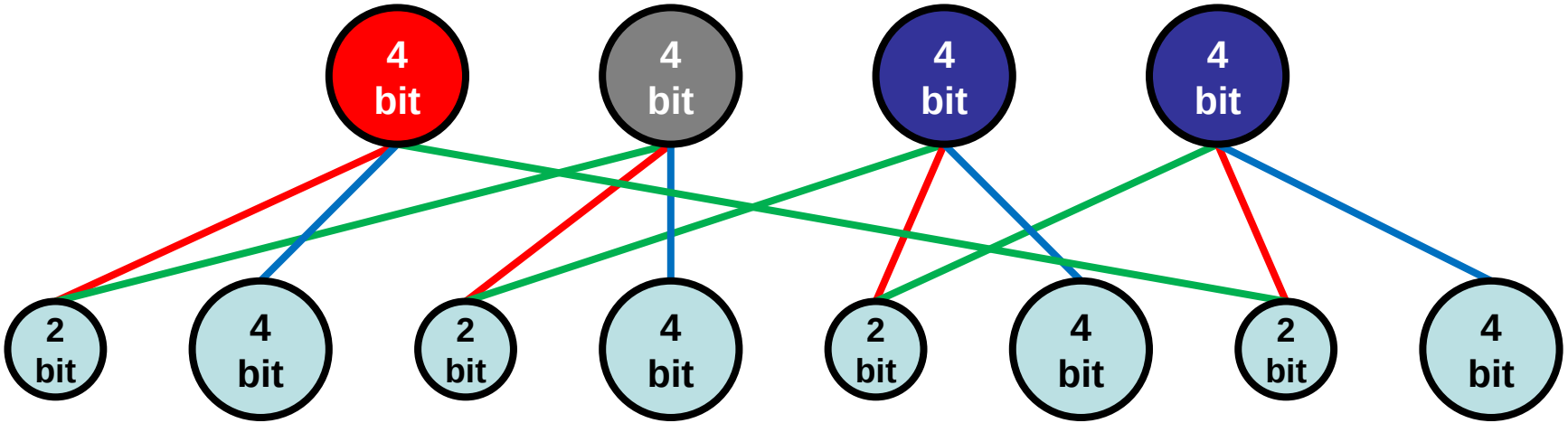

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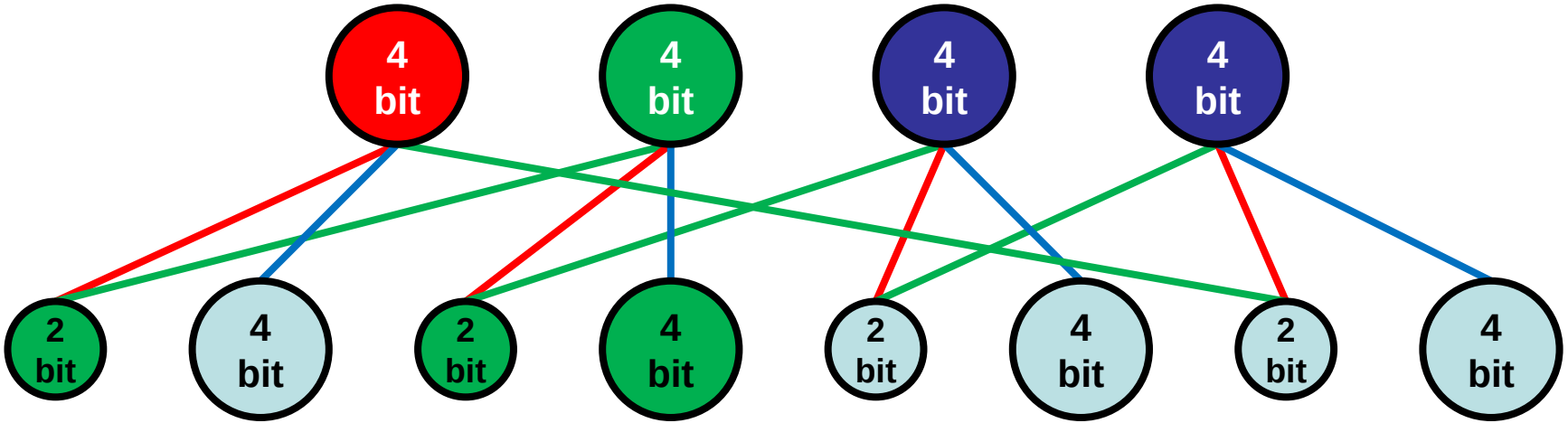

“High Radix” LDPC: Decoding

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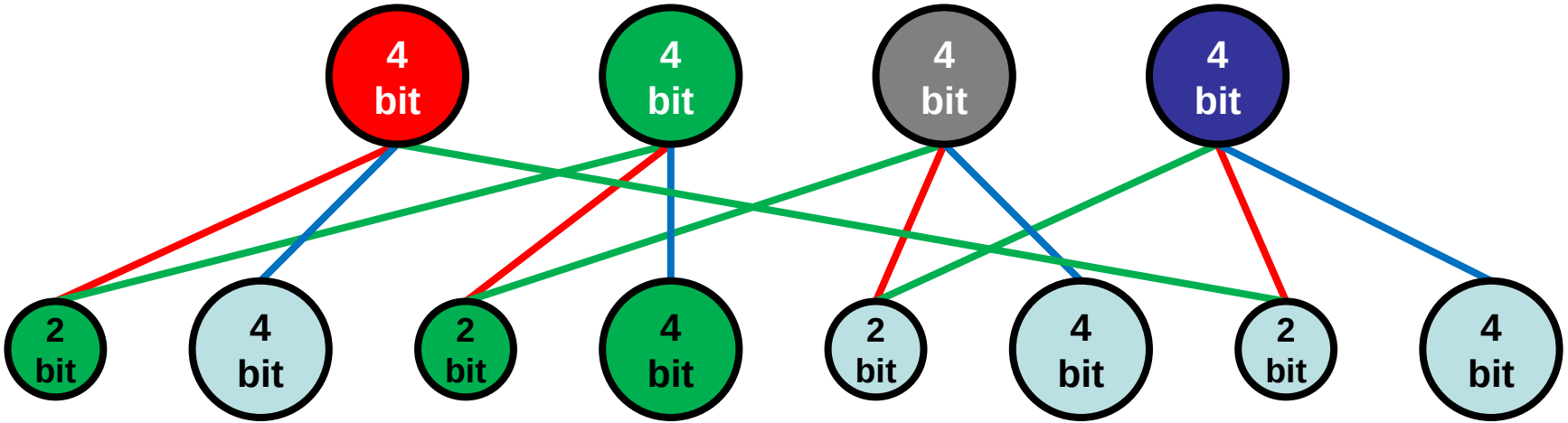

“High Radix” LDPC: Decoding

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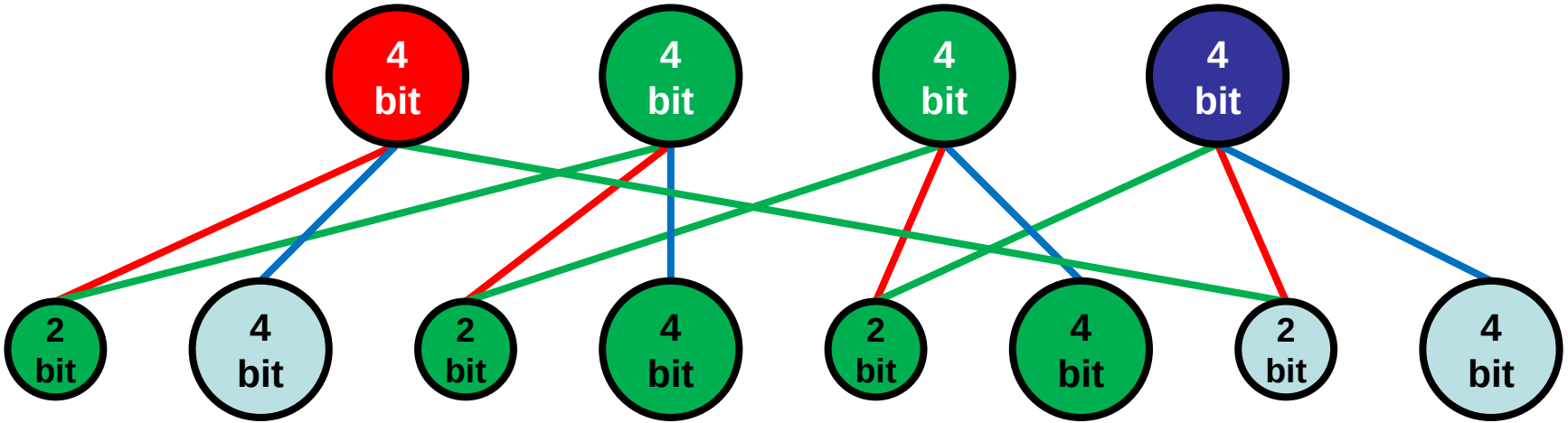
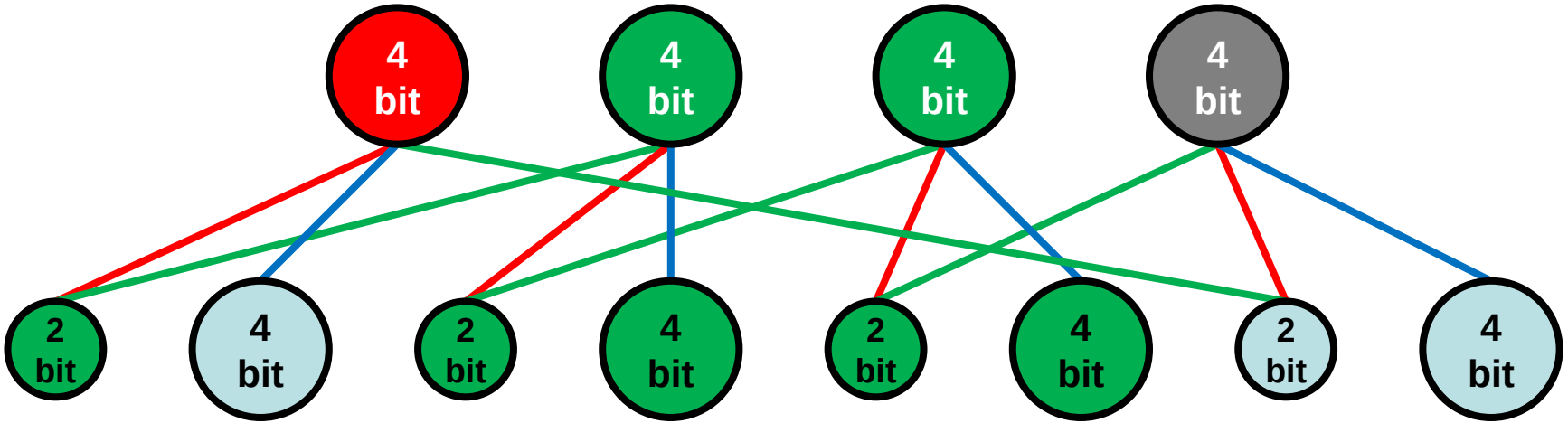


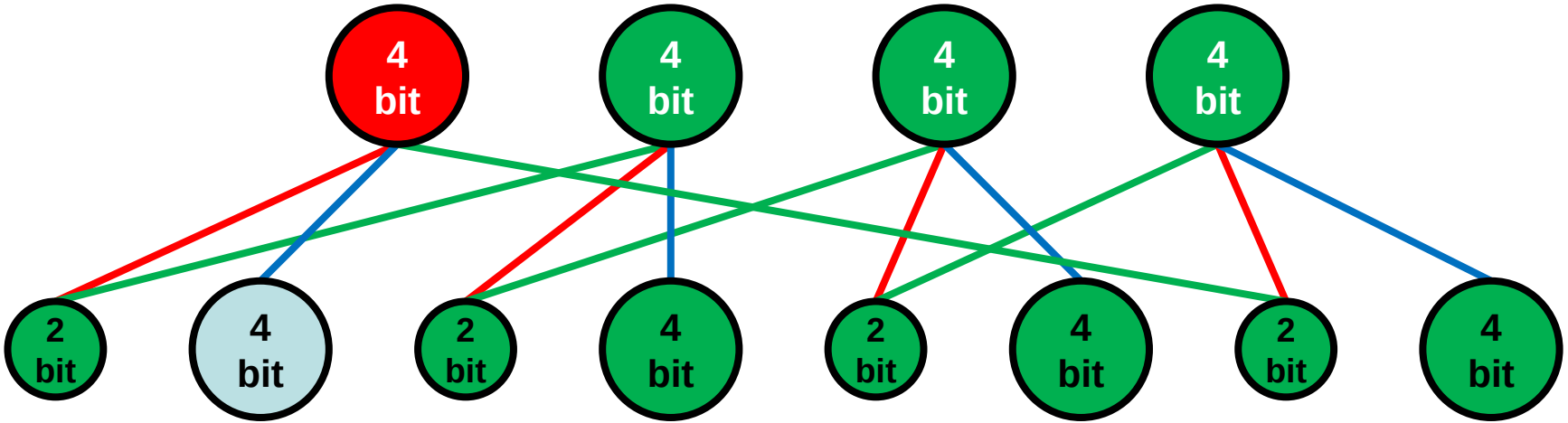
“High Radix” LDPC: Decoding

- **Cascade decoding**



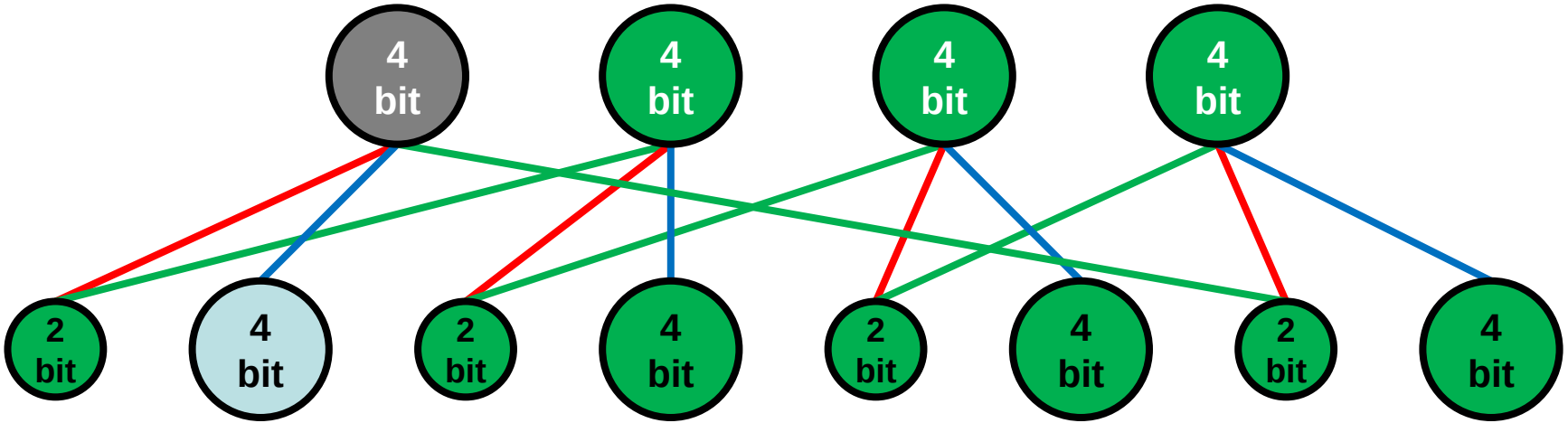
“High Radix” LDPC: Decoding

- **Cascade decoding**



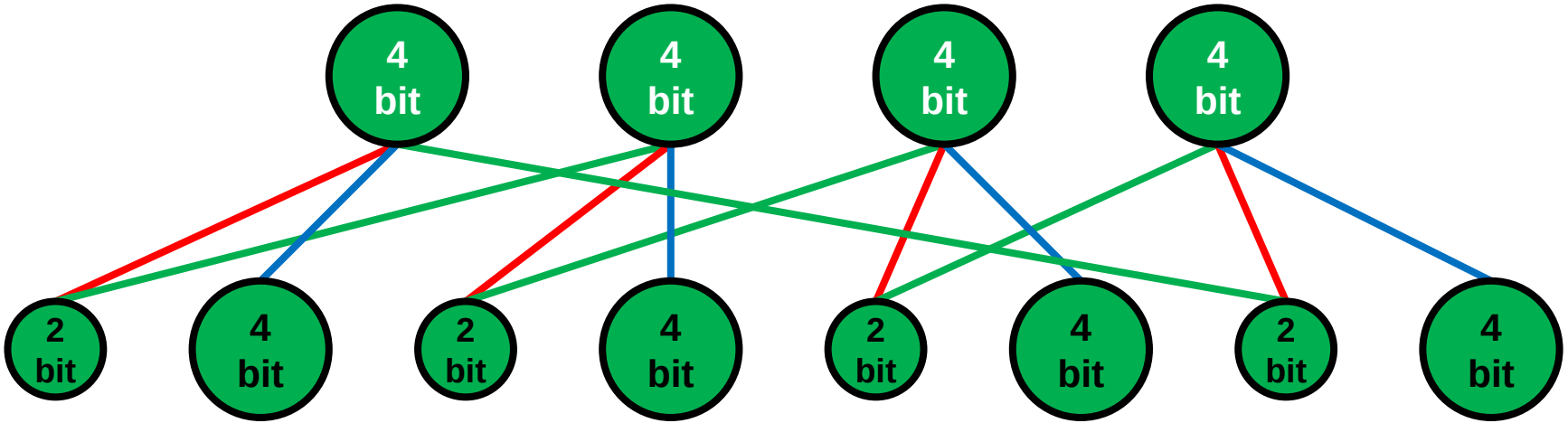
“High Radix” LDPC: Decoding

- **Cascade decoding**



“High Radix” LDPC: Decoding

- **Cascade decoding**



“High Radix” LDPC for SSD

just a flavor to spark your curiosity!

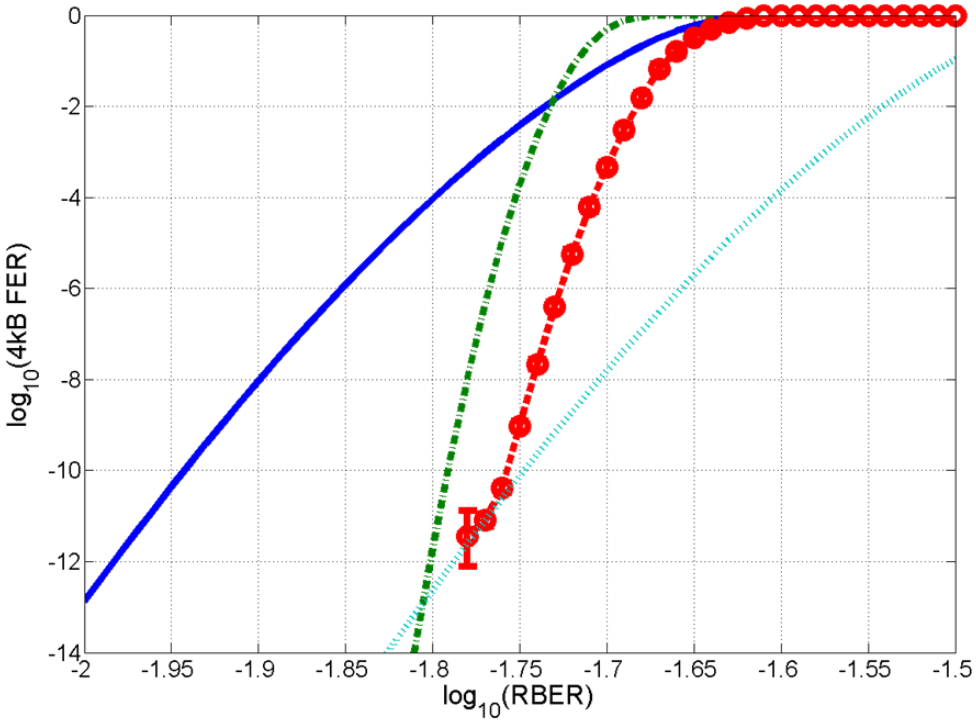
$$H = \begin{bmatrix} h_0 & & \\ & \leftarrow 136 \rightarrow & \\ & & h_{255} \end{bmatrix} \begin{matrix} \uparrow \\ 16 \\ \downarrow \end{matrix}$$

edge matrix:16x136 containing 256 non-zero sub matrices

HRLDPC(48128,32768)

- hard error correction
  - no channel information needed
- 4kB frame size
- combats high raw bit error rate
  - in excess of 1%
- low rate ECC
  - step down from 16kB to 12kB user information per page
- higher/lower code rate/frame size also possible

Binary Symmetric Channel Correctability



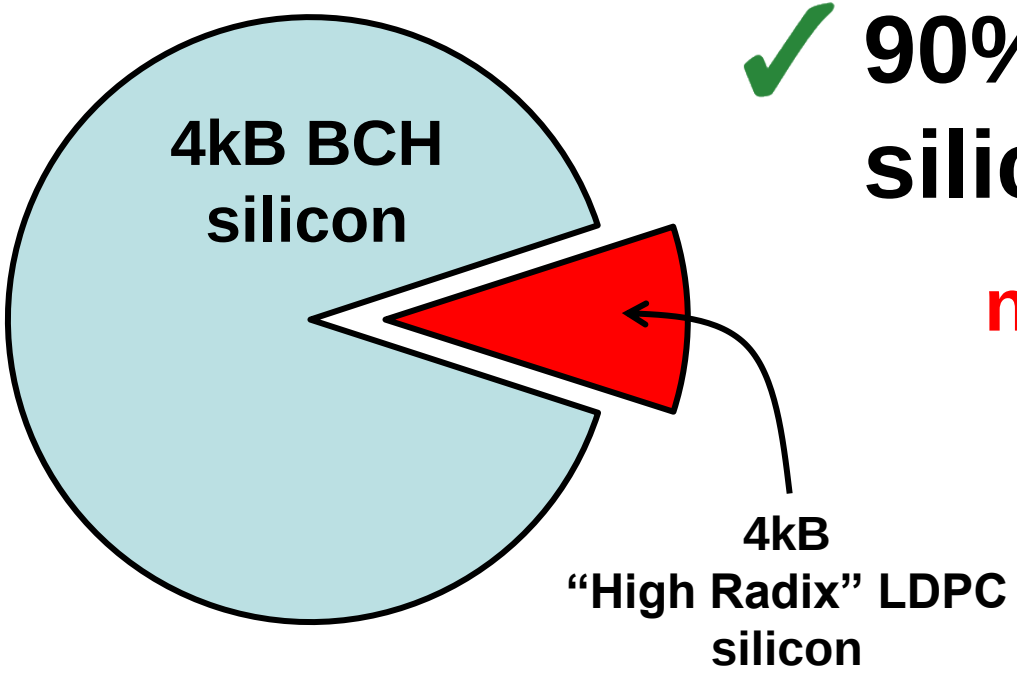
3 codes:

- 16x[BCH(3008,2048) - 80bit correctable]
- BCH(48128,32768) - 960bit correctable
- HRLDPC(48128,32768) - simulated (99% CI)
- HRLDPC(48128,32768) - error floor estimation

✓ HRLDPC tolerates higher RBER than 960bit correctable BCH code

✓ HRLDPC has accurate error floor estimation

Silicon Saving



✓ **90% reduction in silicon size**

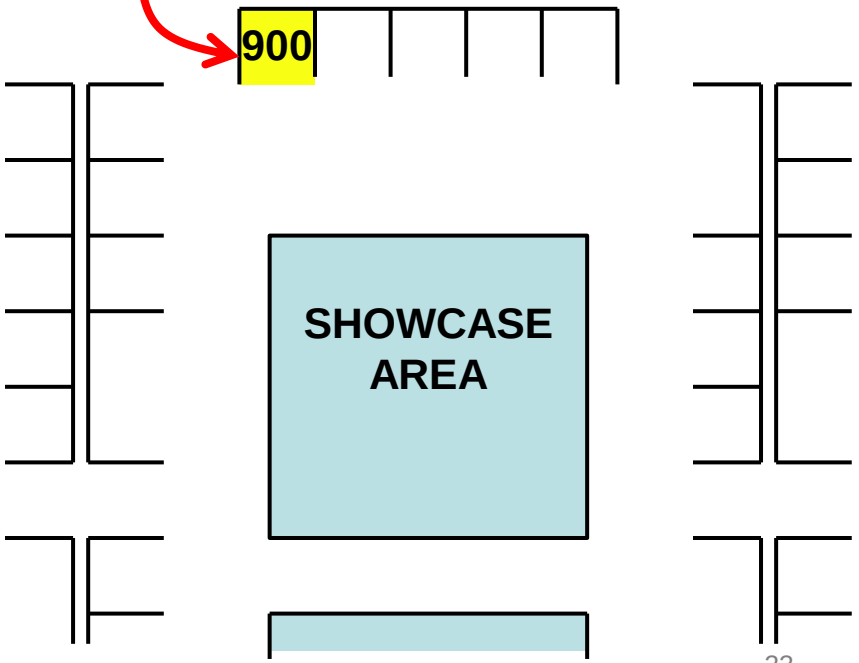
no compromize in throughput

VISIT OUR BOOTH!

BOOTH 900

(FAR RIGHT CORNER)

SIGLEAD IS HERE!



- **take control of our NAND analyzer systems**
  - **SigNASII**
  - **SigNAS3**

NAND supplied
or
BRING YOUR OWN!

- **SL2007 – SSD controller IC**
- **discussion & chat**