Read Disturb Characterization for Next-Generation Flash Systems

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Agenda

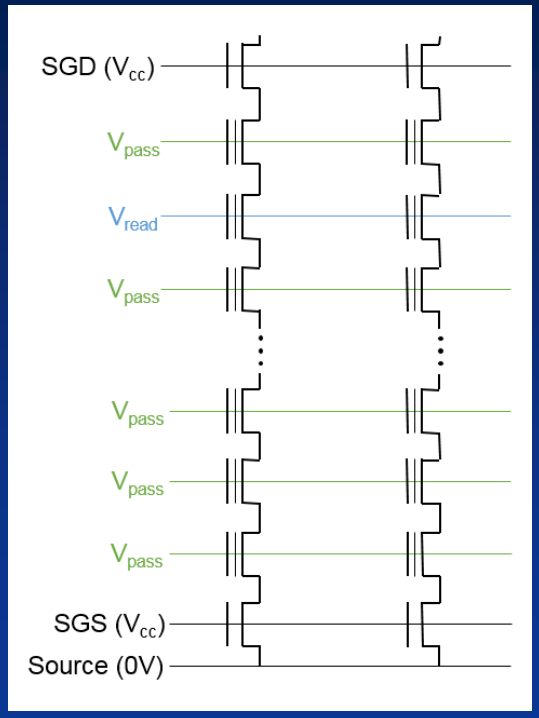
- *Industry Trend*
- *Background*
- *Mixed Mode Analysis*
- *Influence of Environment / Flash Access Mode*
- *Read Disturb Tolerance vs. Technology*
- *MLC Read Cycling Analysis*
- *Initial TLC Analysis*
- *Dynamic Analysis*
- *Summary*

Read Disturb – Industry Trend

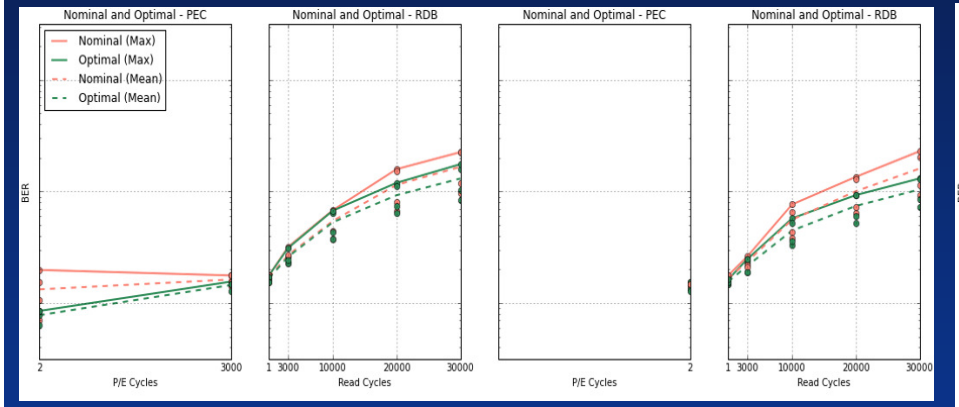
- *With technology advancement, Flash industry began to make tradeoffs to maintain endurance levels*
  - *Read disturb tolerances were reduced in some cases*
- *Read intensive Flash applications have increased focus on read disturb failure mechanism*
- *Growth and application of TLC have also highlighted read disturb tolerance as a key specification*
- *Traditionally, read disturb specifications are not widely available in supplier data sheets*
- *NET: Based on technology advancement, emergence of read intensive applications and TLC, read disturb tolerances must be thoroughly evaluated and better understood*

Read Disturb – Background

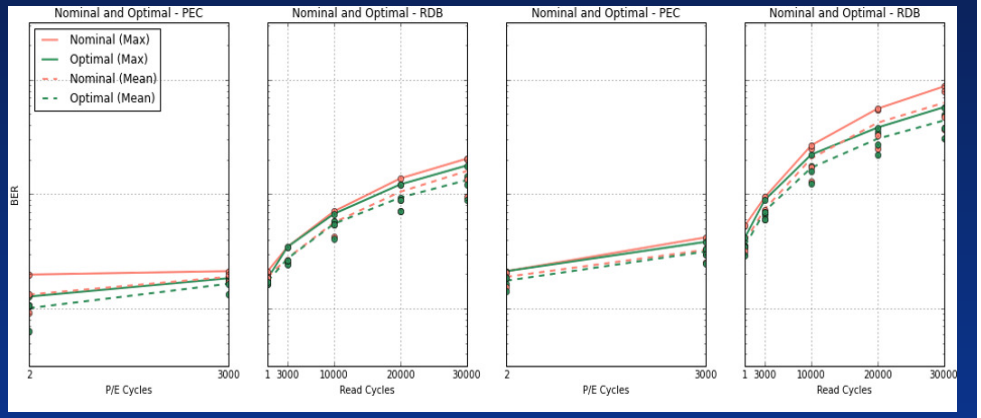
- *Read disturb occurs when programmed blocks are read repeatedly without any erases in between these reads*
  - *When one wordline is read, other wordlines in the block are weakly programmed (V_{pass} applied)*
  - *Repeated reads without an erase can cause cells to shift enough to change their state*
  - *Read disturb effect is exacerbated by P/E cycling stress*
  - *Block erase resets read disturb effect*
- *JEDEC read disturb test specification is to read all pages in a Flash block sequentially*
- *Read disturb effects are more pronounced in smaller technology nodes*



Mixed Mode Analysis



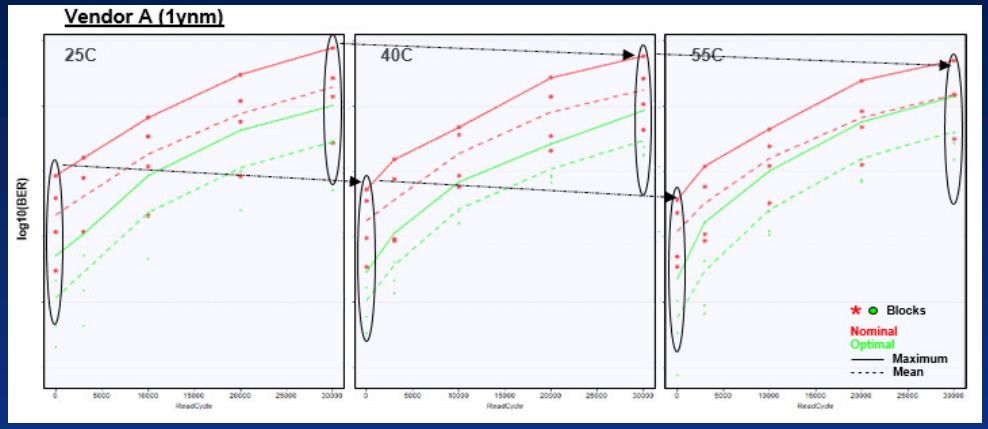
2 PE Cycles Inserted Between 30K Read Cycle Runs (3002 PE Cycles Total)

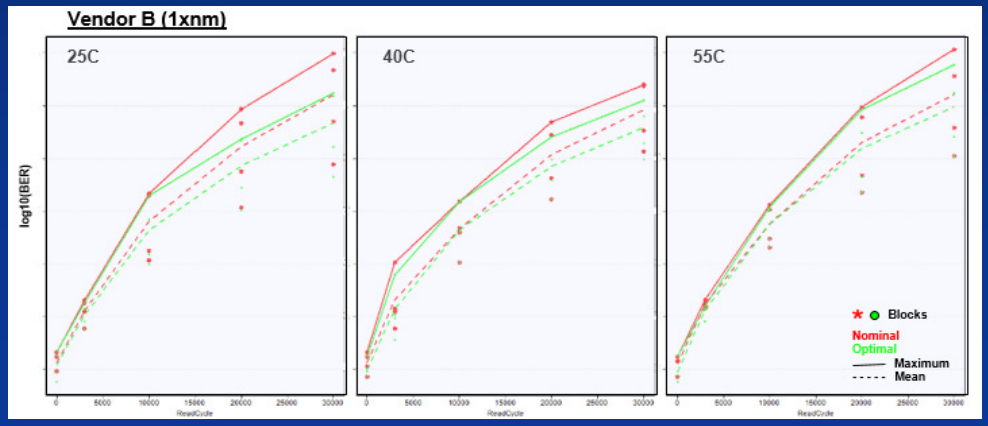


3K PE Cycles Inserted Between 30K Read Cycle Runs (6K PE Cycles Total)

- *Experiment confirms*
  - *PE cycling stress worsens read disturb effect*
  - *Block erase resets read disturb effect*
  - *Read cycling interspersed between PE cycles does not affect wear rate*

MLC Read Cycling – Temperature Analysis



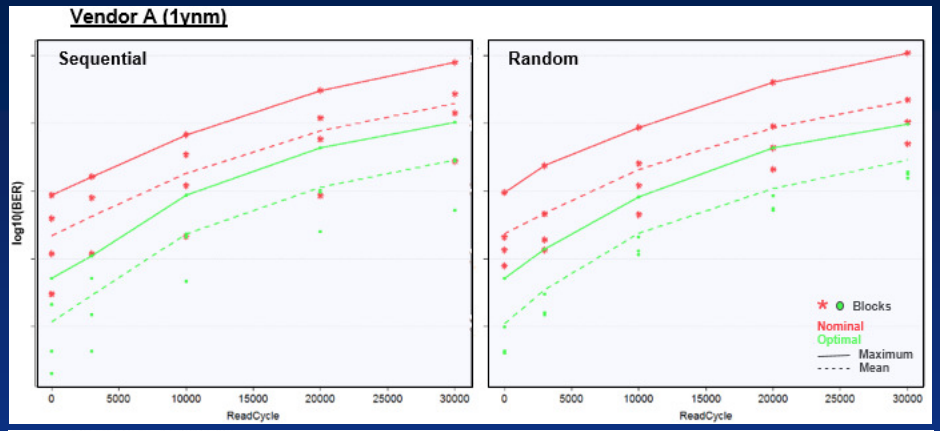


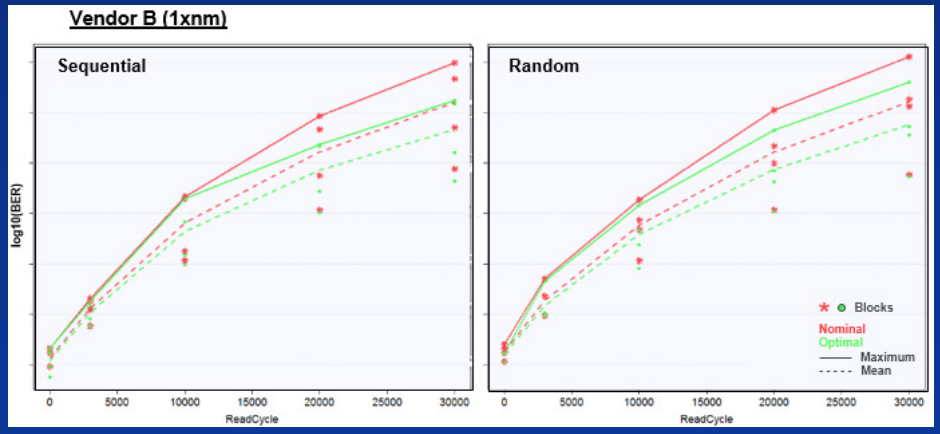
Note:
Nominal - No Read Optimization
Optimal - Read Optimization

- *Slight relative offsets in BER curves across temperature track with initial read cycle offsets*
  - *No indication of temperature sensitivity*

- *Lower BER profile at 40'C points to variability in overall results*
  - *No indication of temperature sensitivity*

MLC Read Cycling – Address Sequencing Analysis





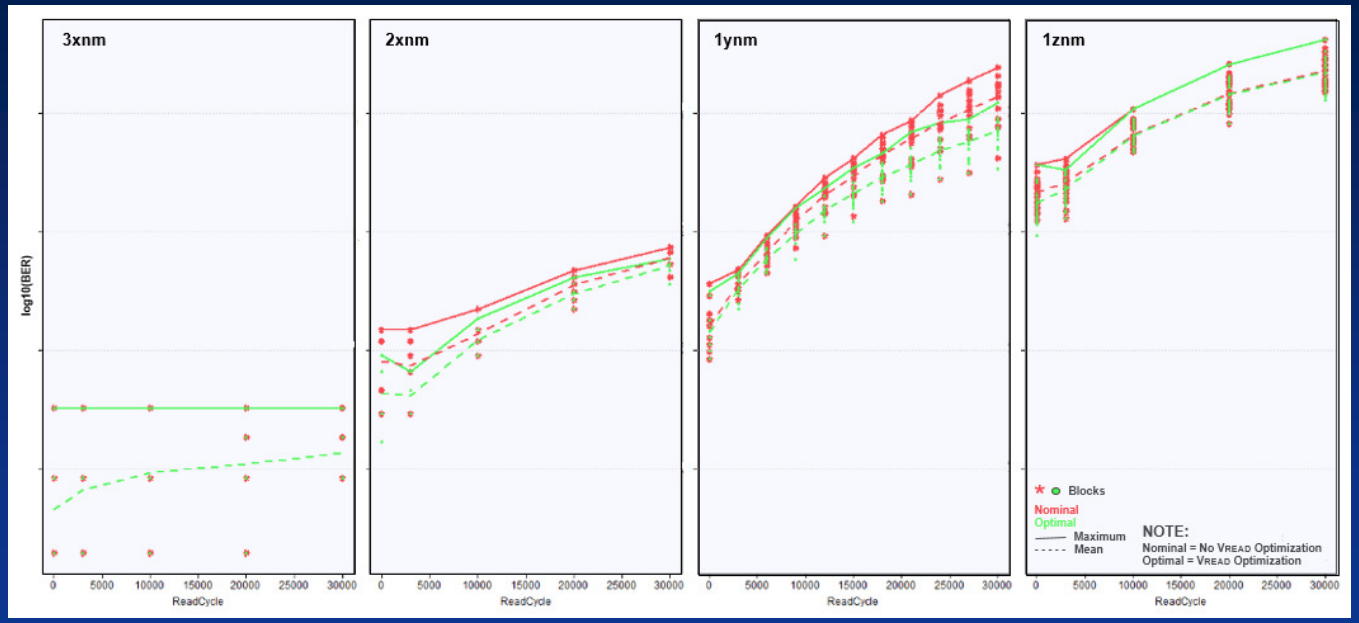
Sequential - block read = all 'X' pages read in sequence
Random - block read = 'X' page reads with random page addressing

Note:
Nominal - No Read Optimization
Optimal - Read Optimization

- *No significant differences in BER profiles seen between*
  - *Sequential page access*
  - *Random page access*

for multiple suppliers / technologies

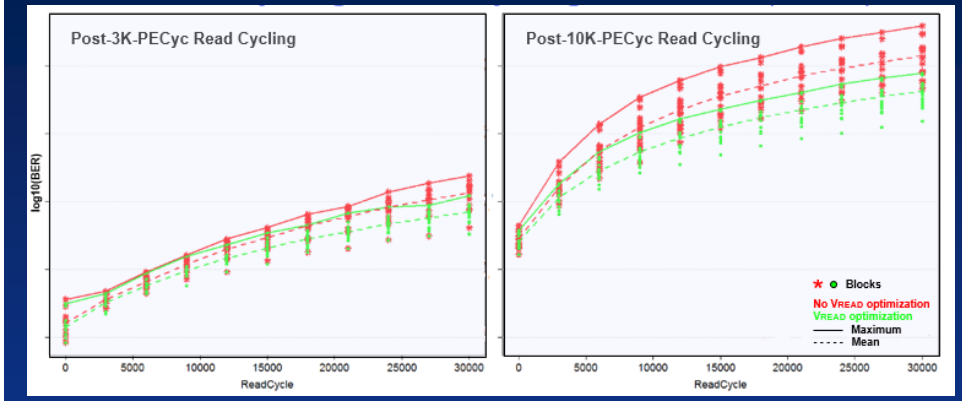
Read Disturb Performance – Technology Progression



Supplier Z: Post 3K PE cycling, 30K Read cycling (80/20% PE cycling @ 59.2'C, Read cycling @ 40'C)

- *Notable degradation of MLC read cycle performance with technology progression*
  - *1znm read error rate is 1.5 orders of magnitude worse than 3xnm*
  - *However, resulting read error rate also driven by degradation in PE cycle capability vs. technology*
  - *1znm read cycle tolerance is slightly improved from prior generation*
- *3D NAND expected to provide temporary relief of read disturb effects, but further degradation must be monitored*

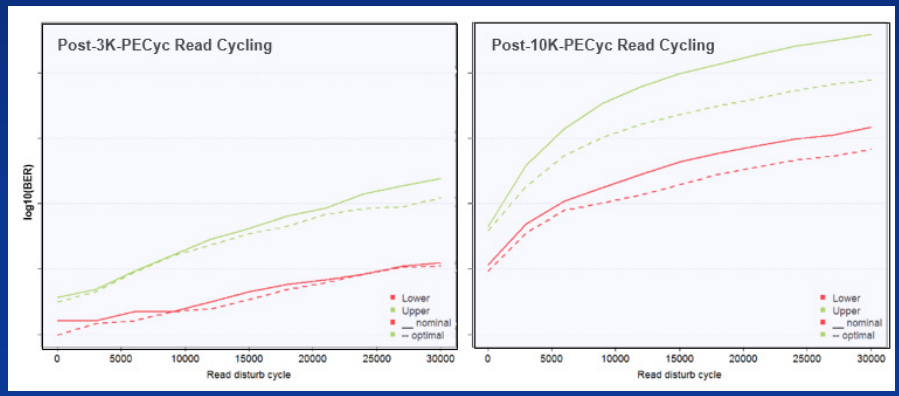
MLC Read Cycling Analysis



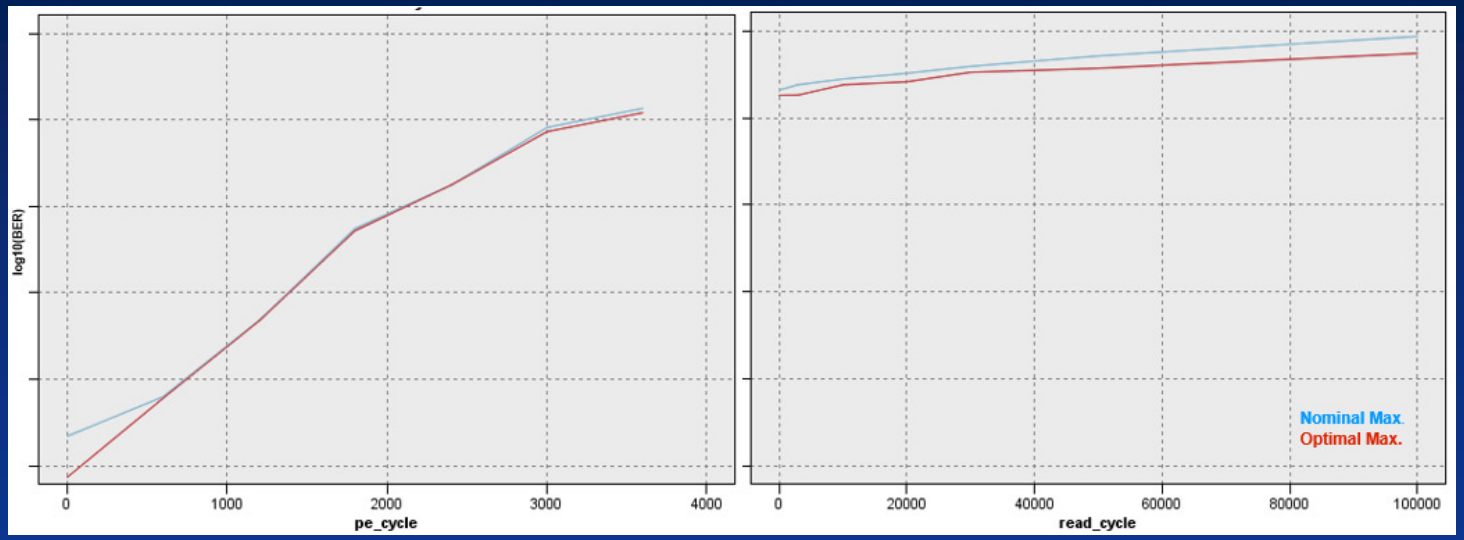
Note:
Nominal - No Read Optimization
Optimal - Read Optimization

- *Read cycling BER accelerates at higher rate after 10K PE cycles (relative to 3K PE cycles)*
- *Indication of increased wear due to PE cycling contributing to higher Read Cycling BER*

- *Read cycling BER acceleration (post 10K PE cycling) is more prominent in upper pages*



Initial TLC Analysis



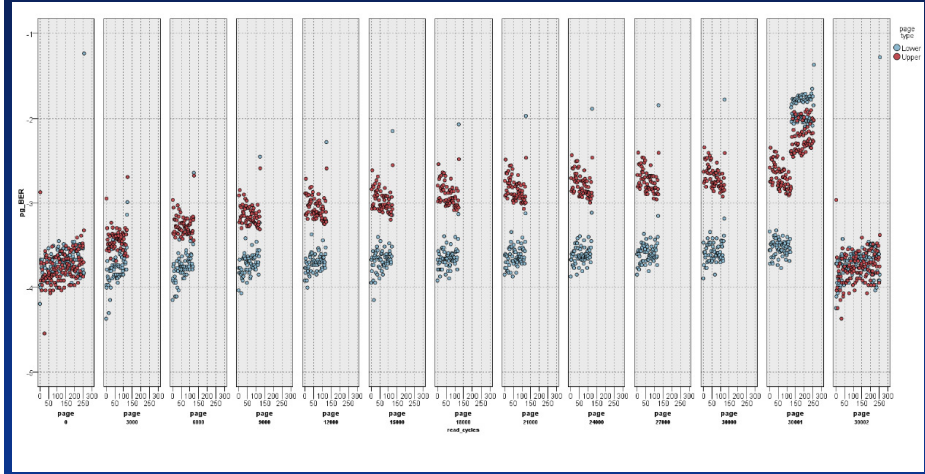
Supplier K (TLC): Post-3600-PE Cycling, 100K Read Cycling (Non-Accelerated PE Cycling @59.2C, Read Cycling @40C)

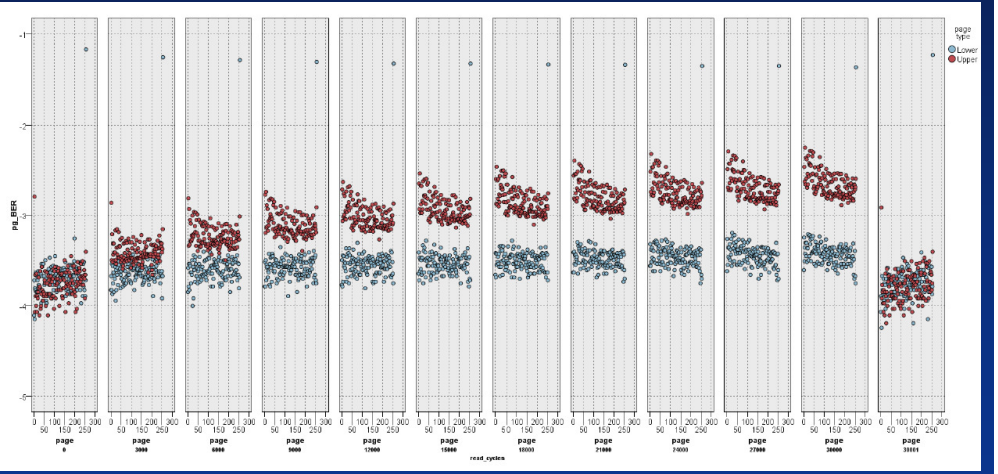
- *Initial TLC analysis shows solid read cycling BER performance (relative to PE cycling)*
- *May be an appropriate design point for read intensive applications*
- *Minimal gain observed with read level optimization for both PE cycling and read cycling*

Dynamic Read Disturb Analysis

- 6K PE cycles, Partial program of block, 30K read cycles of programmed pages with 3K readouts
- Program remaining un-programmed pages, readout, final PE cycle with readout

- 6K PE cycles, Full program of block, 30K read cycles of programmed pages with 3K readouts
- Final PE cycle with readout





- *Some applications are dependent on manipulation of partially programmed Flash blocks*
- *Read disturb effect is much worse for partially programmed blocks (un-programmed pages once programmed are degraded)*
  - *Affects erase states dramatically*
- *"Reset" is performed through typical block erase operation – degraded BER performance no longer evident*

Summary

- *With the emergence of read intensive applications and TLC, the Flash read disturb failure mechanism must be thoroughly evaluated and well understood*
- *Read disturb effects are more pronounced with the progression of technology groundrules*
- *Initial TLC read disturb tolerance analysis looks promising*
- *Dynamic Flash operations require careful consideration of read disturb effects*
- *Read disturb tolerance specifications must be documented in supplier Flash component data sheets*

Thank You

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