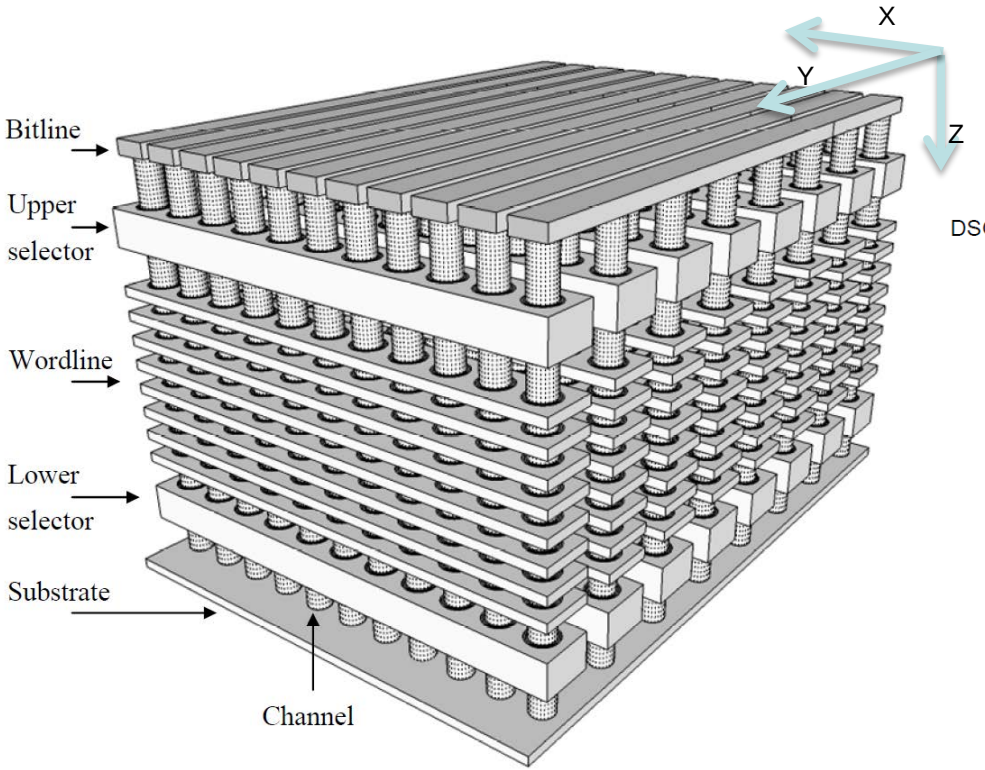
New ECC/DSP Solution Helps Migration to 3D NAND Era

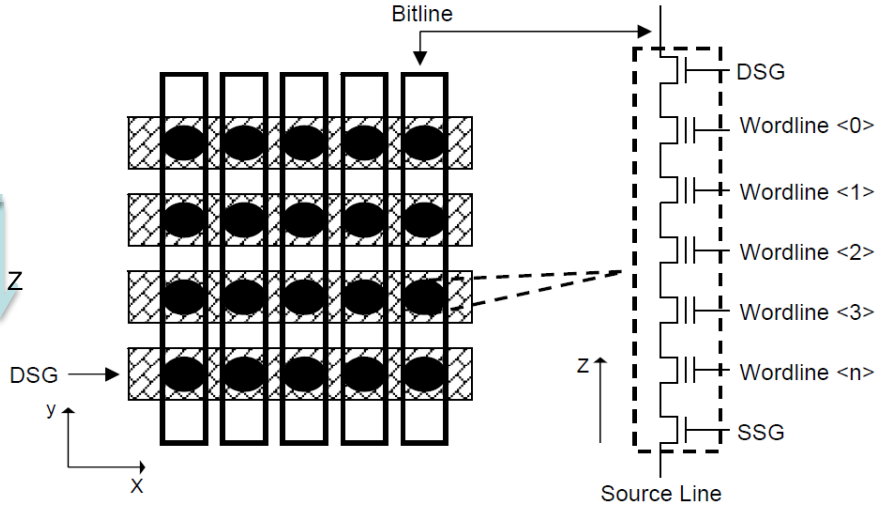
Jeff Yang

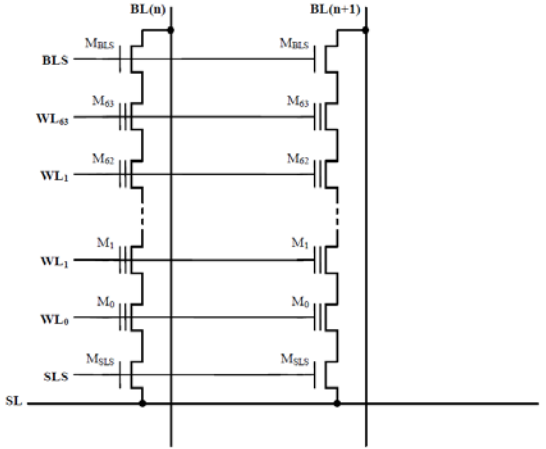
Principle Engineer

SiliconMotion

From 2D to 3D

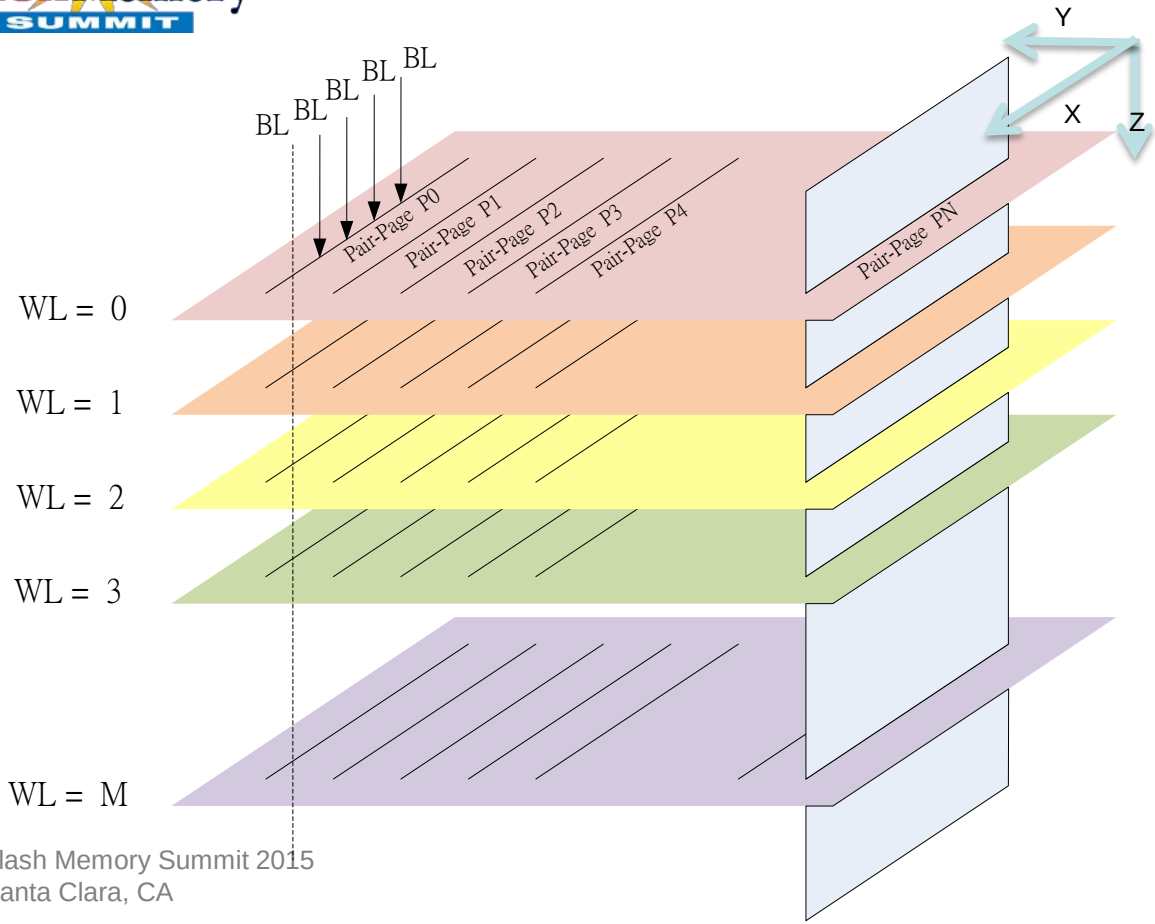






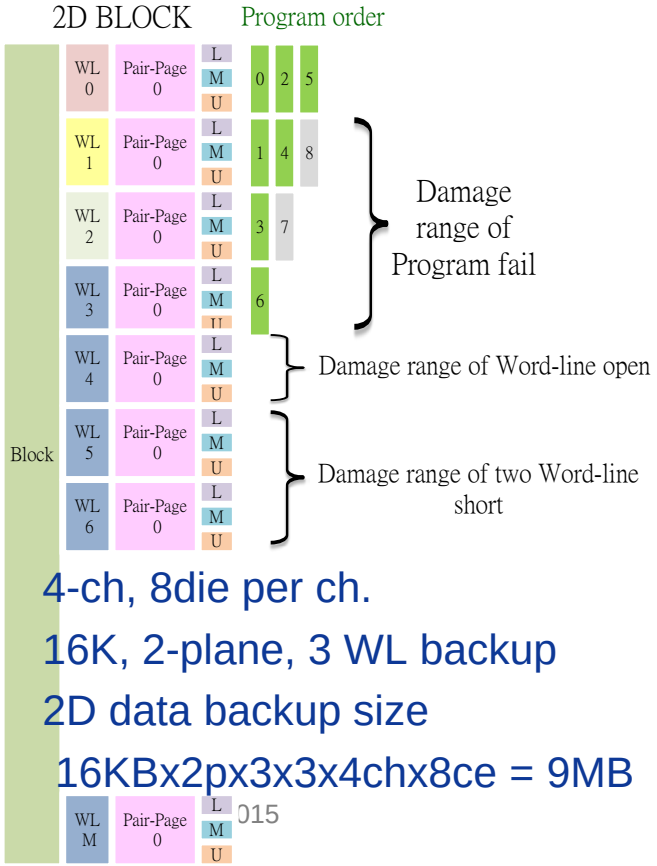
[ref]: Rino. M, Luca. C, Alessia. M, "Inside NAND Flash Memories, Springer". 2010

3D/2D logical view vs. Physical view.



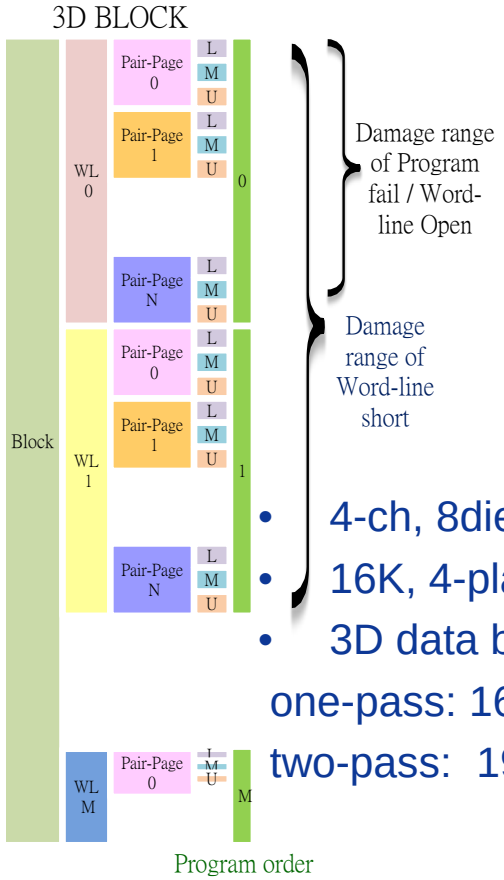
- X-Z view is similar to 2D structure.
- 2D block only include the X&Z view.
- Block Erase: Whole block(X&Y&Z) cell will be erased.
- Program order.
  - WL by WL.
  - Within WL: pair-page by pair-page.
- One-pass vs. multi-pass program.
  - Three pass(foggy-fine) ➔ one-pass.
  - Three pass(foggy-fine) ➔ two-pass

Failure range from 2D to 3D.



- 4-ch, 8die per ch.
- 16K, 2-plane, 3 WL backup
- 2D data backup size

  16KBx2px3x3x4chx8ce = 9MB



- 4-ch, 8die per ch.
- 16K, 4-plane, 2 or 1WL backup, N=15
- 3D data backup size

one-pass: 16KBx4px3x16x4x8=98MB

two-pass: 196MB

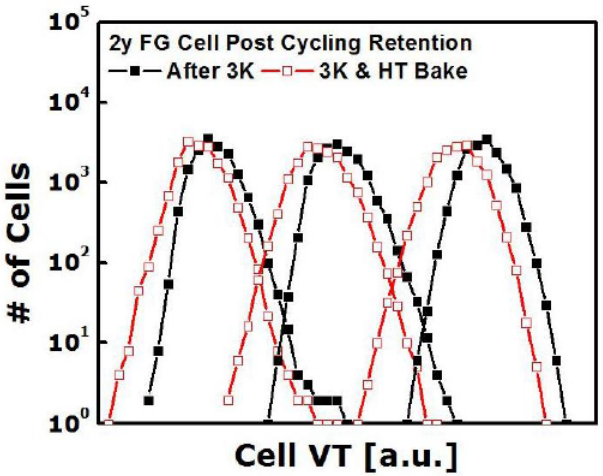
The application of RAID for failure.

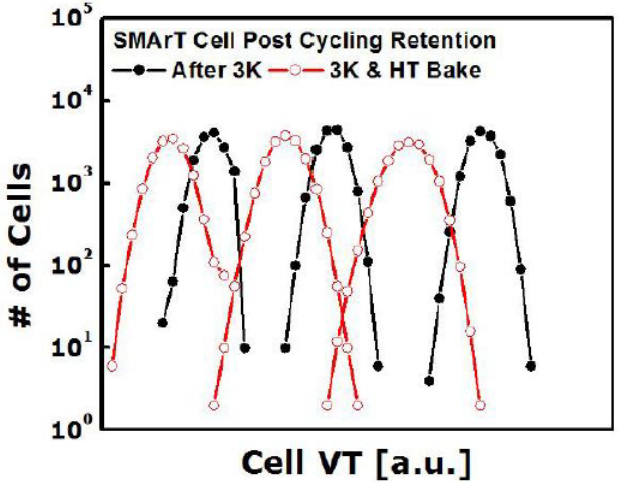
	CH#	0	0	1	1	
	CE#	0	1	0	1	
WL0	pair-page	P0	P0	P0	P0	S0
	pair-page	P1	P1	P1	P1	S1
	pair-page	P2	P2	P2	P2	S2
	pair-page	P3	P3	P3	P3	S3
WL1	pair-page	P4	P4	P4	P4	S4
	pair-page	P5	P5	P5	P5	S5
	pair-page	P6	P6	P6	P6	S6
	pair-page	P7	P7	P7	P7	S7
WL2	pair-page	P8	P8	P8	P8	S8
	pair-page	P9	P9	P9	P9	S9
	pair-page	P10	P10	P10	P10	S10
	pair-page	P11	P11	P11	P11	S11
WL3	pair-page	P12	P12	P12	P12	S12
	pair-page	P13	P13	P13	P13	S13
	pair-page	P14	P14	P14	P14	S14
	pair-page	P15	P15	P15	P15	S15

- Program failure may use the RAID to reduce the data-backup overhead.
- For the small SSD with binary capacity requirement is important.

  i.e, 128GB = 137,438,953,472B
- RAID with XOR becomes challenges to keep the binary capacity
- Make the same failure group into different RAID protection family.
- 3D-TLC smaller capacity SSD with binary capacity is the most cost-attractive solution in client SSD.

Retention issue on 2D/3D

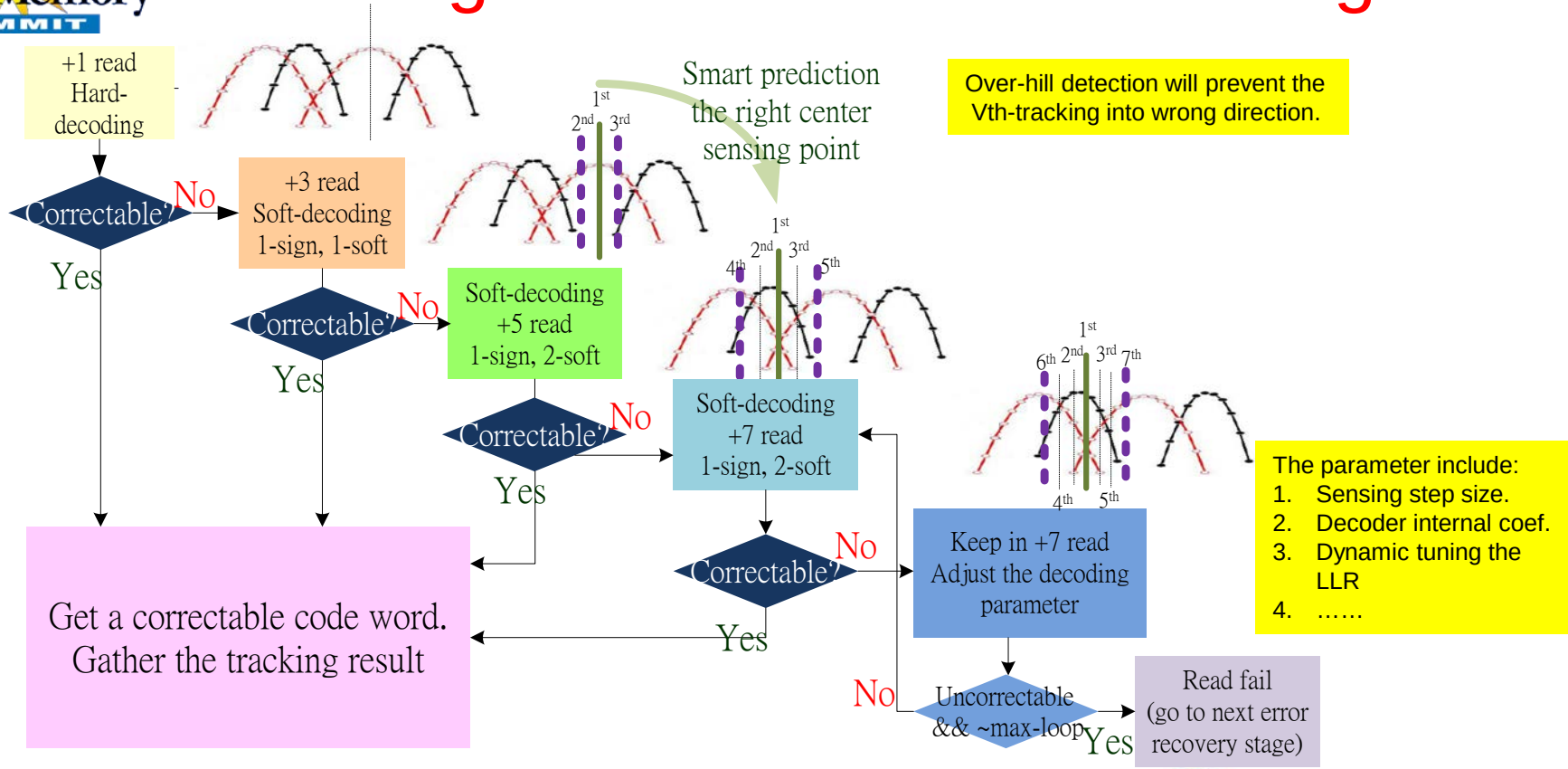




- Both the 2D and 3D will have the data retention problem.
  - 1Znm MLC need 6~10 read-retry tables, But TLC need 40~45 tables with less endurance and retention.
  - 3D will have more severe Data retention issue.

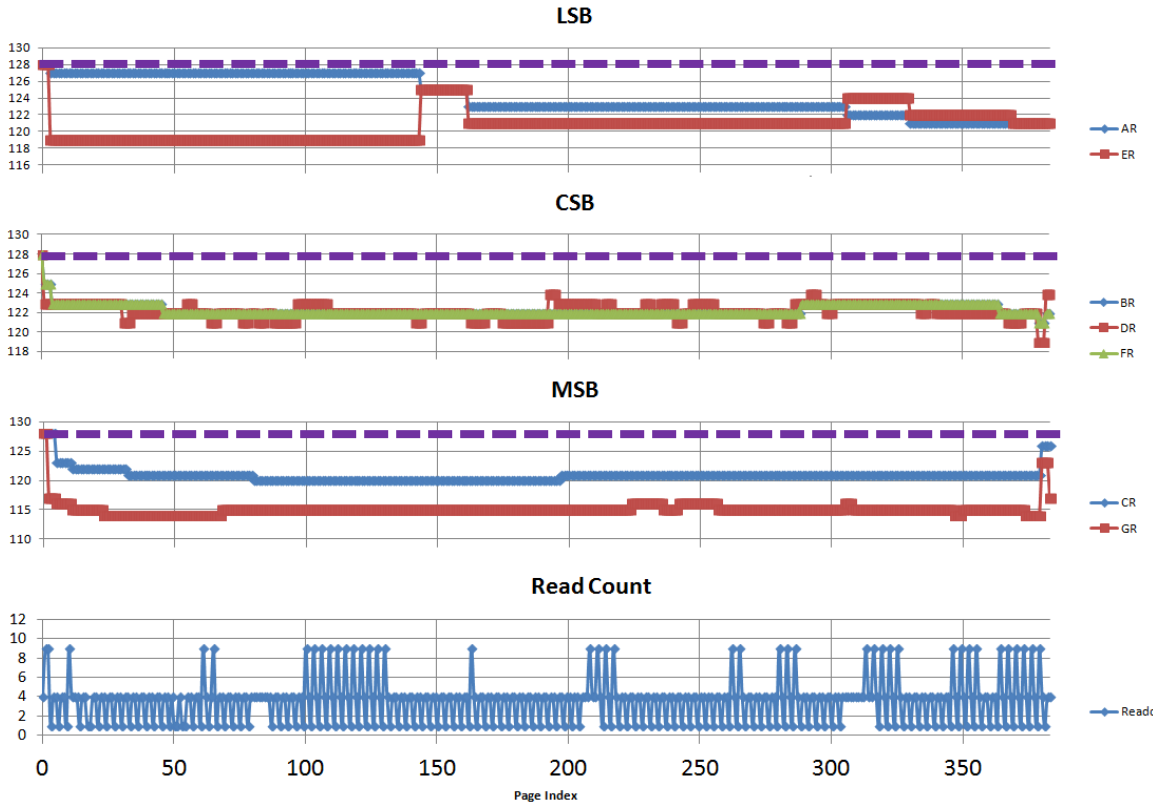
[ref]: E.S. Choi, S.K. Park, “Device Considerations for High Density and Highly reliable 3D NAND Flash Cell in Near Future”. IEDM 2012

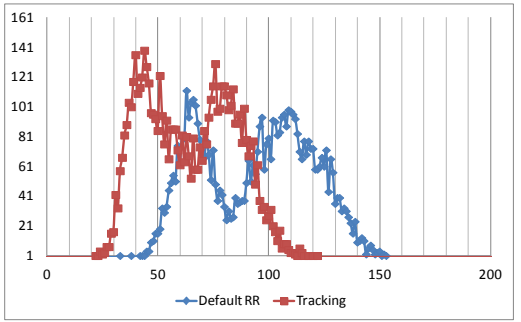
DSP algorithm for the Vth-tracking



Vth tracking example in 2D TLC

900 P/E,
6hr. 100'C
(3year. 25'C)





Always start from Hard-decoding
Hard-decoding only ➔ read-count =1
1-sign, 1soft ➔ read-count = 4
1-sign, 2soft ➔ read-count = 9
Most of LSB-page success in hard-decoding

Original read-count = 384 (page-number)
Vth-tracking read-count =1378
Using read-retry table = 9242

Runtime and background calibration

RBER for A: default Read-Point, B: using read-retry table.
C: Vth-tracking result.

DefaultRP

PE\HR	0	1	2	3	4	5	6
0	0.0013	0.0014	0.0014	0.0014	0.0014	0.0015	0.0016
100	0.0011	0.0011	0.0018	0.0019	0.0021	0.0021	0.0023
300	0.0011	0.0026	0.0029	0.0031	0.0033	0.0035	0.0039
500	0.0013	0.0036	0.0041	0.0044	0.0049	0.0051	0.0058
700	0.0014	0.0058	0.0067	0.0073	0.0082	0.0086	0.0097
900	0.0014	0.0066	0.0078	0.0085	0.0098	0.0104	0.0117

TableRR

PE\HR	0	1	2	3	4	5	6
0	0.0013	0.0013	0.0014	0.0014	0.0014	0.0014	0.0014
100	0.0011	0.0016	0.0017	0.0018	0.0019	0.0019	0.0019
300	0.0011	0.0023	0.0024	0.0026	0.0028	0.0029	0.003
500	0.0013	0.003	0.0033	0.0035	0.0039	0.0041	0.0041
700	0.0014	0.0043	0.005	0.0053	0.0061	0.0063	0.0065
900	0.0014	0.0047	0.0055	0.0059	0.0069	0.0074	0.0075

TrackingRR

PE\HR	0	1	2	3	4	5	6
0	0.0013	0.0014	0.0014	0.0014	0.0014	0.0015	0.0015
100	0.0011	0.0017	0.0018	0.0019	0.0021	0.0021	0.0021
300	0.0011	0.0016	0.0028	0.0031	0.0033	0.0034	0.0035
500	0.0013	0.0023	0.0036	0.0038	0.0041	0.0042	0.0042
700	0.0014	0.003	0.0048	0.0052	0.0054	0.0057	0.0059
900	0.0014	0.0031	0.0051	0.0058	0.0063	0.0067	0.007

- Vth tracking provide efficient read-count and similar RBER accuracy.
- BCH-1K/72bit with read-retry table supports the green region only.
- LDPC with Vth-tracking is wider than this table.
- The gap between Default and Tracking will become huge from 2D to 3D flash.
- Vth-tracking is suitable for Runtime and background calibration.
- Each block needs a read-count, P/E count and retention count.
- The retention count includes the Vth-shifting value and the RBER.

When a TLC SSD project kick-off~

Make the decision on:

- DRAM or DRAM-less.
- Data will write into SLC or directly write into TLC.
- Fixed or Dynamic SLC buffer.
- NAND failure model and collapse range. Need RAID or not.
- Warranty, TBW(total Byte write) and the Data-Retention requirement.
- Guarantee good block number and the capacity.(binary/decimal/arbitrary)
- Access behavior to WAF

THEN:

- Check the NAND's Characteristics on RBER and ECC is affordable or not.

- Finally, the controller cost should be 10~15% to the Client SSD module.
- Higher cost ECC is affordable for Larger capacity SSD, but Larger capacity has more relaxed requirements.
- Smaller capacity with severe restriction will need a more complicated controller.

SM2258/2256 ready to support 3D flash

Encoder:
Process change from 55nm to 40nm (30%), architecture change (45%)
Decoder:
Process(30%), architecture change (20%)

- Support RAID capability.
- Support high endurance and Data-retention by DSP-LDPC engine.
- Reduce 75% Encoding power from 2256 to 2258.
- Reduce 50% decoding power.
- **Visit us at the booth - 313**