Radiation Effects in SSDs

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Outline

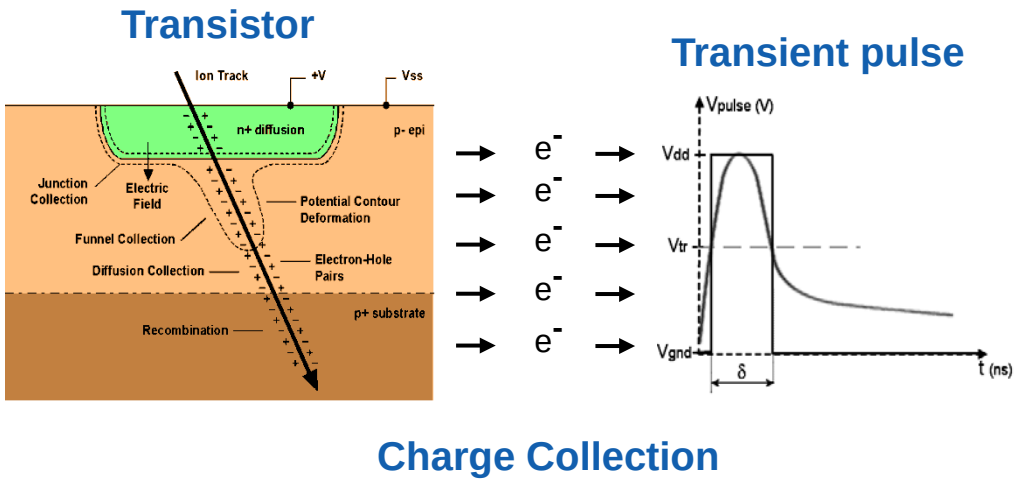
- Introduction
- Soft Errors in SSDs
- Radiation Testing
- Test Results
- *Early* Reliability Analysis
- Conclusion

Introduction

Soft Errors

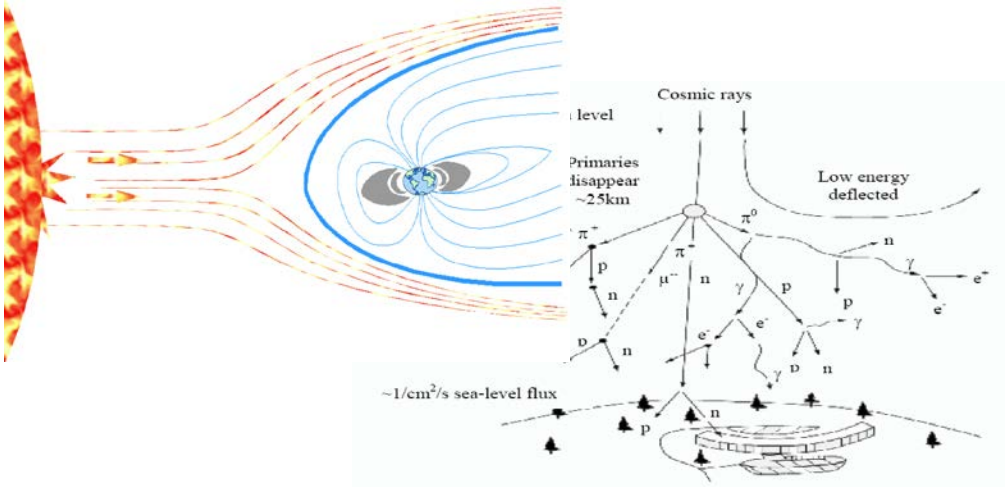
Soft Errors are caused by ionizing radiations (neutrons, alpha particles)

- Interaction with silicon
- Charge deposition and collection
- Current spike
- Upset (SEU) or Transient (SET)

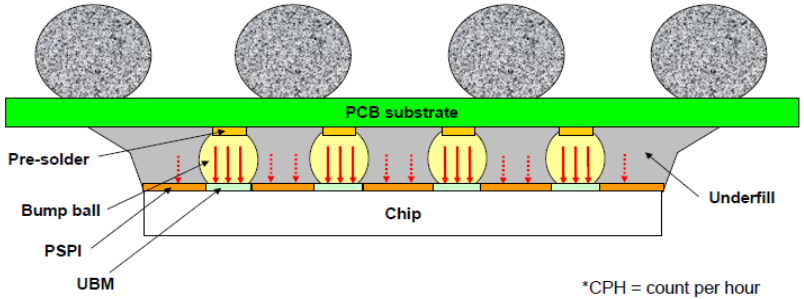


Source of Ionizing Radiation

- Neutrons (High energy and Thermal) generated by high energy particles, coming from space, entering the atmosphere and interacting with the air (Nitrogen, Oxygen, …)



- Alpha particles generated by traces of radioactive materials in the packaging materials



*CPH = count per hour

Soft Error Trend

- Voltage Effect
  - Lower voltage → increased sensitivity ↗
- Smaller devices
  - Lower target area → reduced sensitivity ↘
  - Smaller stored charge → increased sensitivity ↗
- Number of devices (SRAM cells, flip-flops)
  - More devices → increased total sensitivity ↗
- Transistor type
  - FINFETs show lower sensitivity than planar transistors ↘
- Increased awareness
  - Increased awareness results in more careful design ↘

Soft Errors in SSD

SSD Architecture

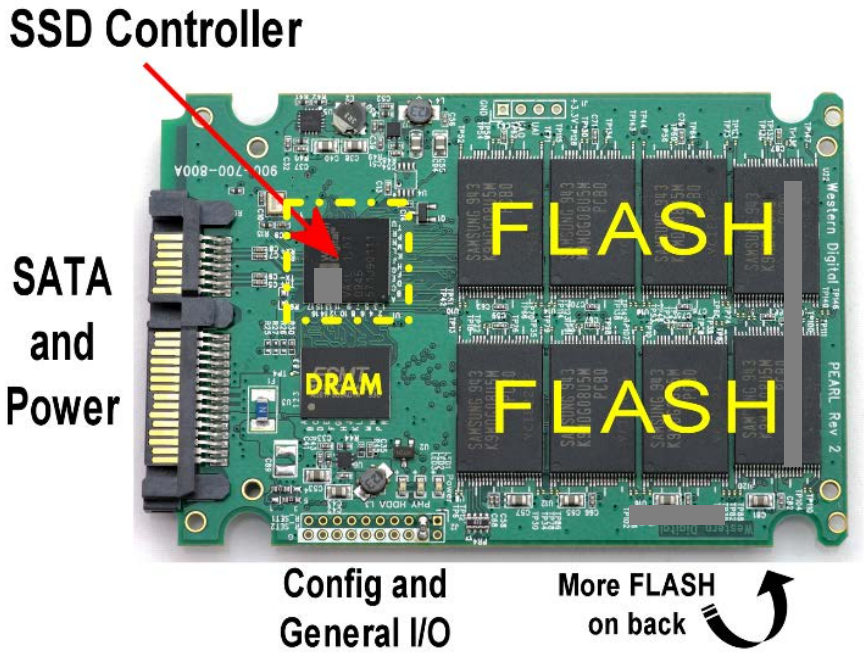


Image taken from http://webscopia.com/2011/10/what-is-an-ssd-solid-state-disk-basics-and-performance-measures/

Main SSD Components and Risk

Component	Type	Potential Risk
Mass memory	NAND Flash	Low sensitivity to SER
Controller	ASIC with SRAM and FF	Unprotected SRAM, FF: high sensitivity
Buffer/Cache	DRAM or SRAM	Unprotected SRAM: high sensitivity

Sensitivity by function

- Control path, pointer table: critical items (an error there might not be recoverable)
- Data path: less critical
- Risky time window: when data is transferred through the buffer before reaching NAND Flash (read/write)

NAND Flash

- Floating Gate Array: “0” pattern (programmed) is usually more sensitive
- Page Buffer → SEUs
- SEFIs:
  - Program errors: complex algorithm, more logic
  - Erasing errors: simple, apply a bias for a fixed amount of time
  - Read/write errors: block upsets, etc
- Impact on time spent on erasing/programming
- Charge Pumps failures: (program/erase affected)
  - Temporary, during irradiation, p/e fails
  - Permanent, p/e fails
  - Degradation, p/e completes but takes longer

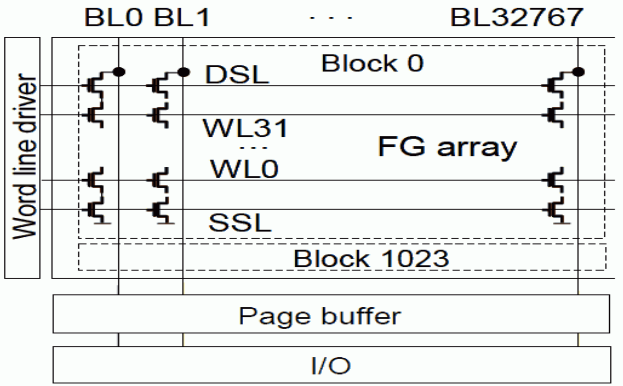
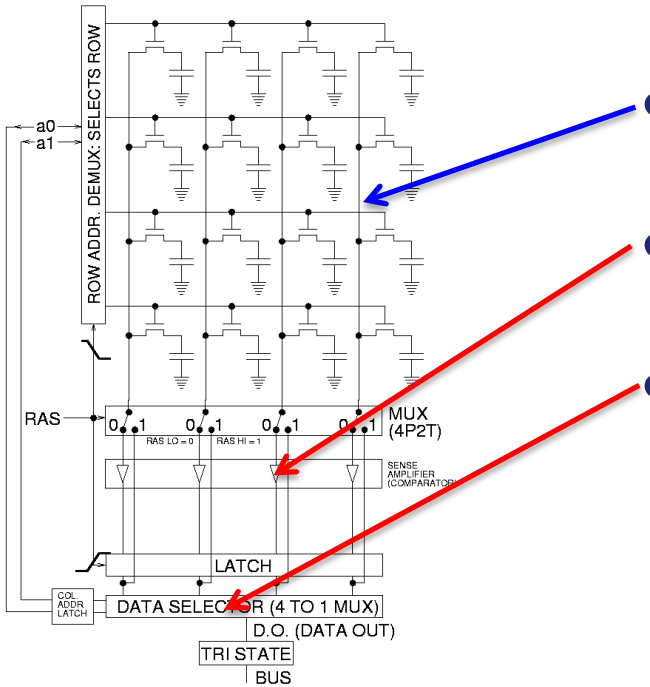


Image taken from Bagatin et all - Single Event Effects in 1Gbit 90nm NAND Flash Memories under Operating Conditions.pdf

DRAM



- Modify the charge stored in the cell capacitor
- Upset sense amplifier during access
- Upset various logic/control circuits

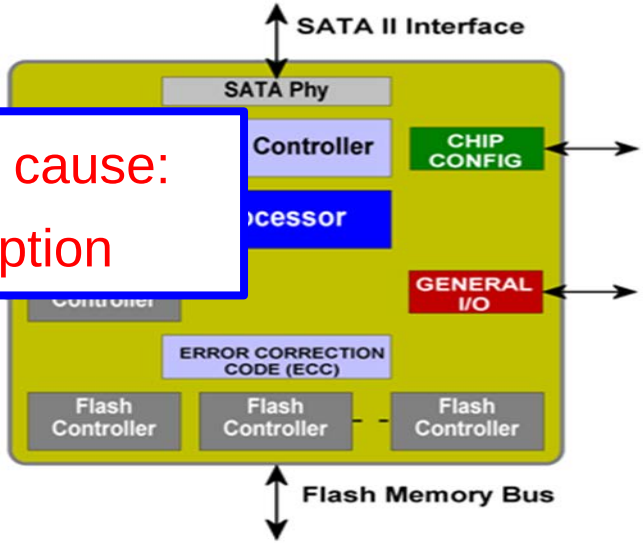
"Comparison of Accelerated DRAM Soft Error Rates Measured at Component and System Level", Borucki et all, IEEE CFP08RPS-CDR 46th Annual International Reliability Physics Symposium, Phoenix, 2008

Controller

- Functions
  - Error correction (ECC)
  - Wear leveling
  - Bad b
  - Read management
  - Read and write caching
  - Garbage collection
  - Encryption

Soft Errors affecting the Controller may cause:

device hang, brick and even data corruption



Reliability Requirements

System and chip-level requirements for the maximum acceptable rates of soft errors must be driven by standards (JEDEC JESD218) or customer imposed requirements (Bit Error Rate, QoS, SLA, MTBF …)

	FIT/SSD		
Number Deployed SSD	50	100	500
1000	0.036	0.072	0.36
5000	0.18	0.36	1.8
10000	0.36	0.72	3.6
50000	1.8	3.6	18
100000	3.6	7.2	36
500000	18	36	180
1000000	36	72	360

Errors per month

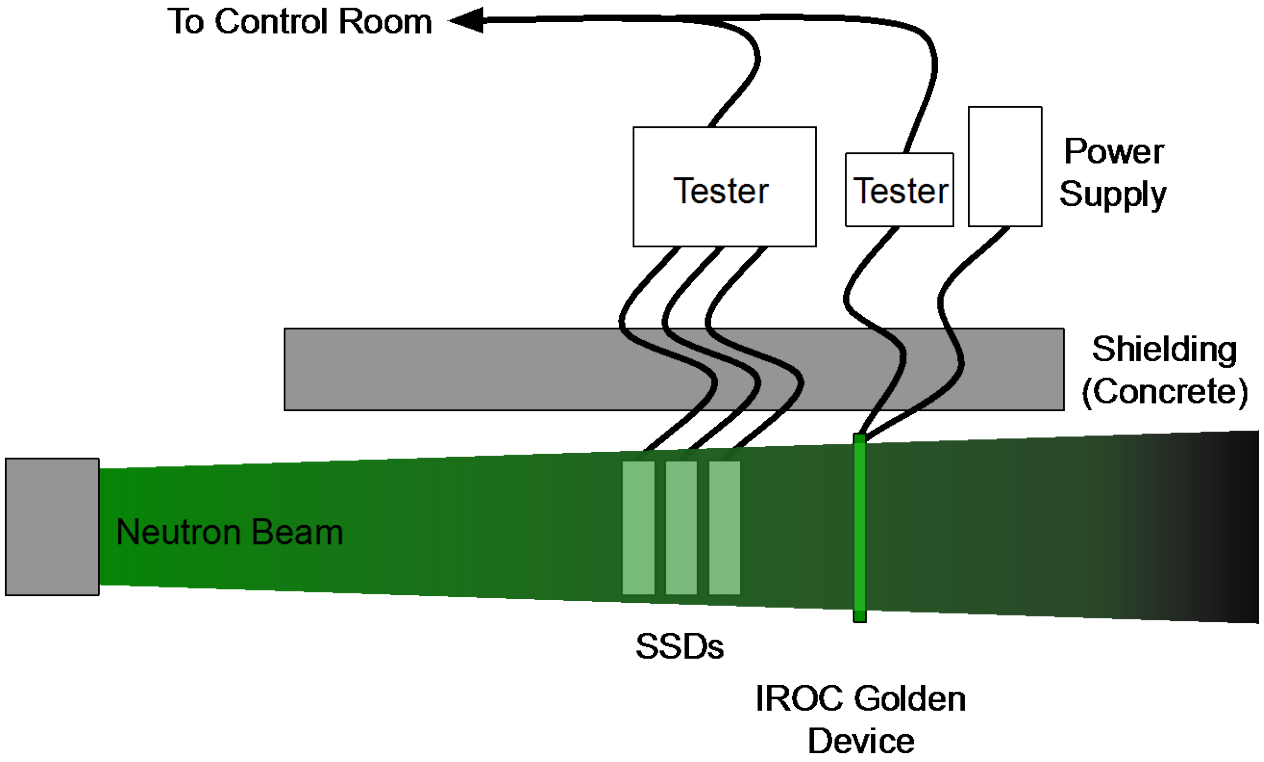
Radiation Testing

Radiation Testing

To evaluate the sensitivity of SSD

- 2 Radiation Test Campaigns were performed at TSL using the ANITA Beam Line (10 SDDs Tested)
- The ANITA beam line reproduces the natural neutron spectrum (neutron energy distribution) but with an higher flux
- Higher Flux → reproduce the effect of thousands of device hours in minutes

Test Setup


To Control Room
Tester
Tester
Power Supply
Shielding (Concrete)
Neutron Beam
SSDs
IROC Golden Device

Test Setup (cont.)

- SSD Tester
  - Workstation with Linux operating system
  - SSD accessed as blocks (2048 bits)
  - Allow detection of: brick, hang, flying write, bit errors, ….
- Golden Device
  - Measure beam attenuation and alignment
- Whole device irradiated
  - Dose effects in DRAM not evaluated
  - Collimated test on controller (next campaign)

Test Results

Device Under Test

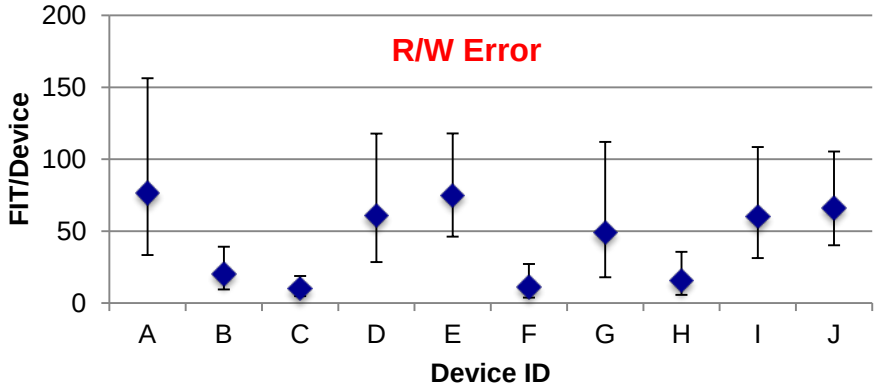
10 SSD Tested

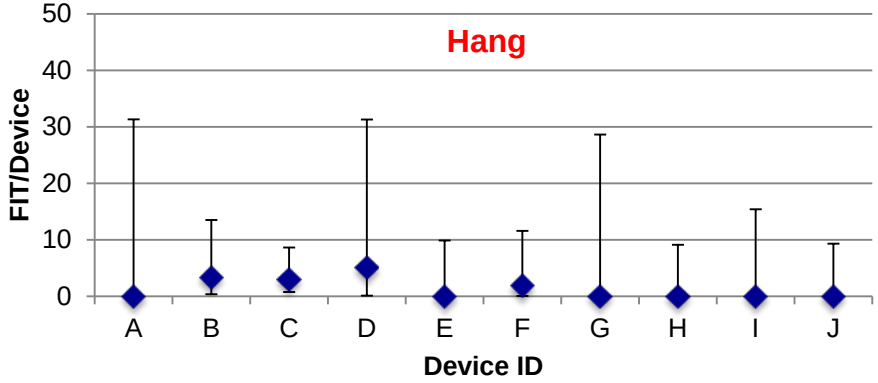
- 6 Manufacturers
- 60 to 256 GB
- SATA III Interface

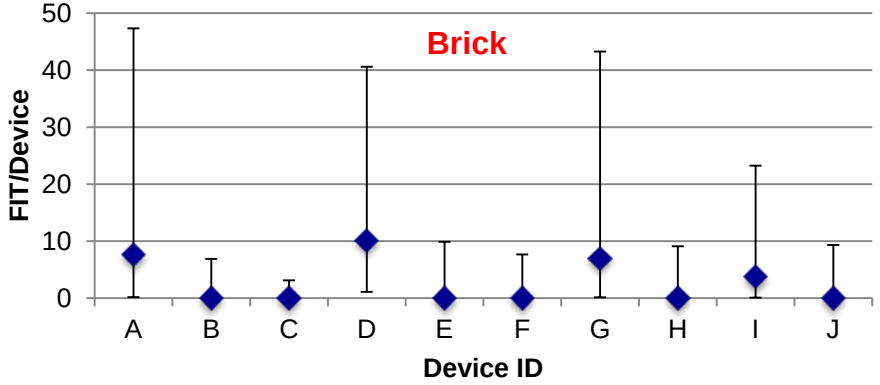
Failure Modes

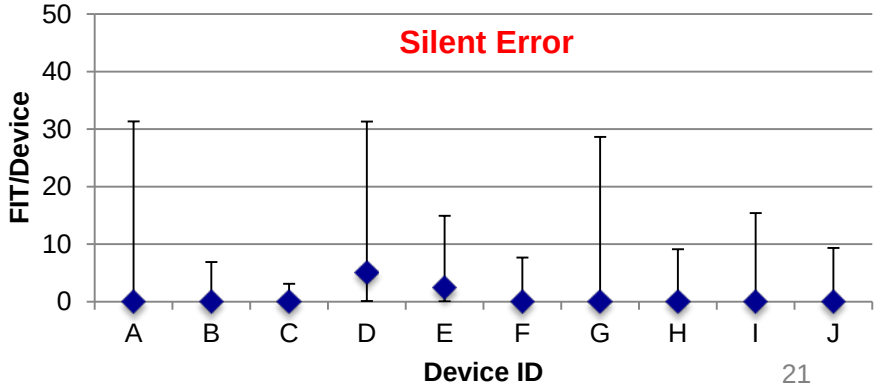
- Read/Write Error – error message returned by the kernel
  no data read or written from/in the device
- Hang – the device stop working, function resumed after power cycle
- Brick – the device stop working, function can't be resumed
- Silent Error – error detected by the tester but not reported by the kernel

Radiation Test Results









In the Field

FIT/SSD

Deployed SSD	10	50	100	500
1k	0.0072	0.036	0.072	0.36
5k	0.036	0.18	0.36	1.8
10k	0.072	0.36	0.72	3.6
50k	0.36	1.8	3.6	18
100k	0.72	3.6	7.2	36
500k	3.6	18	36	180
1M	7.2	36	72	360
5M	36	180	360	1800
10M	72	360	720	3600

ERROR per Month

Complex Failure Modes

- Persistent failing block (write error)
  - Most of the time fixed after secure erase
- Write operation longer than normal (in some cases lead to a brick)
- Flying write: data written at the wrong location (considered Silent Error)

Early Reliability Analysis

Reliability Analysis

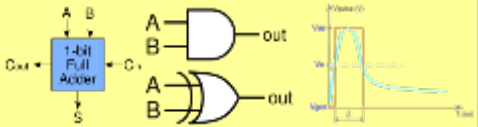
Radiation testing is useful for validation and qualification purposes but…

…requires the device to be manufactured

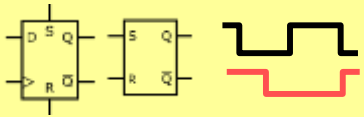
During the design phase – simulation tools are needed

ASIC Level Analysis

Single Event Effect



Single Event Transient

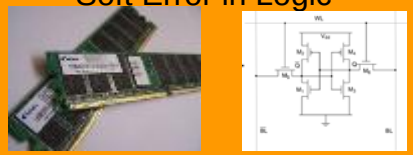


Single Event Upset

DERATING

Soft Error

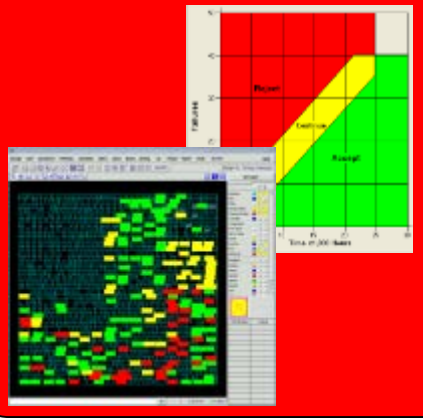
Soft Error in Logic



SEU in memory = Soft Error

DERATING

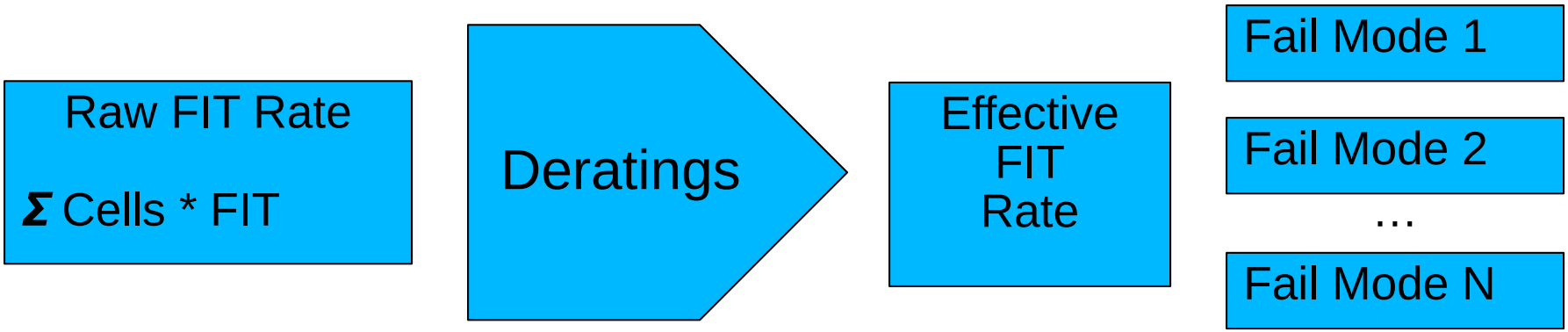
Functional Failure



ASIC Level Analysis (cont.)

- Not all SEEs manifest themselves as faults
- Derating factors are significant (often only 1%..10% of SEUs have an observable effect)
- Controller level:
  - TIFT evaluates the sensitivity of the technology
  - SOCFIT accurately calculates derating factors
- SSD level: FMEA approach using database of SER results and experience (and test results)

Reliability Analysis



Example

1000 FIT (raw)

160 FIT (derated)

Fit by Effect

SDC : 15 FIT

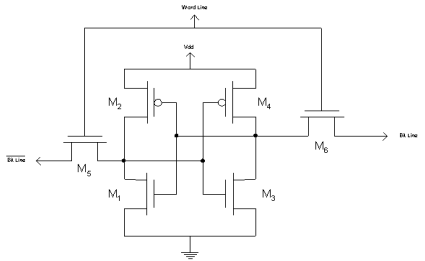
DUE : 50 FIT

(NO EFF : 95 FIT)

Simulation Approach

Process Response model

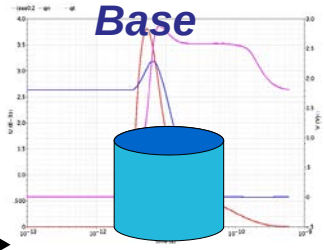
SPICE NetList



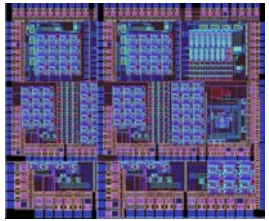
Layout GDS2

TFIT

SER Data Base



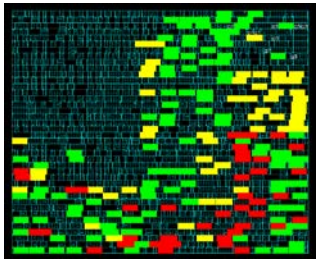
SoC RTL/Netlist



Application

SOCFIT

Analyzed ASIC design



De-rating Analysis

Design optimization

Conclusion

Conclusion

- Test results prove the importance of rigorous testing
  - Accurate SER data to integrate in the reliability datasheets and to report to customers
  - Prove successful fulfillment of design targets
    - Standards: JEDEC JESD218
    - Requirements: Bit Error Rate, QoS, SLA, MTBF
  - Suggest recovery actions to improve the overall system reliability
  - Ultimately … discover vulnerable or critical issues before customers do

Conclusion (cont.)

- Testing needs the manufactured device
  - During the design phase – simulation tools are needed
    - TFIT → Cell level
    - SoCFIT → Chip level
    - FMEA → System level
  - Simulation allows to understand test results

Contact

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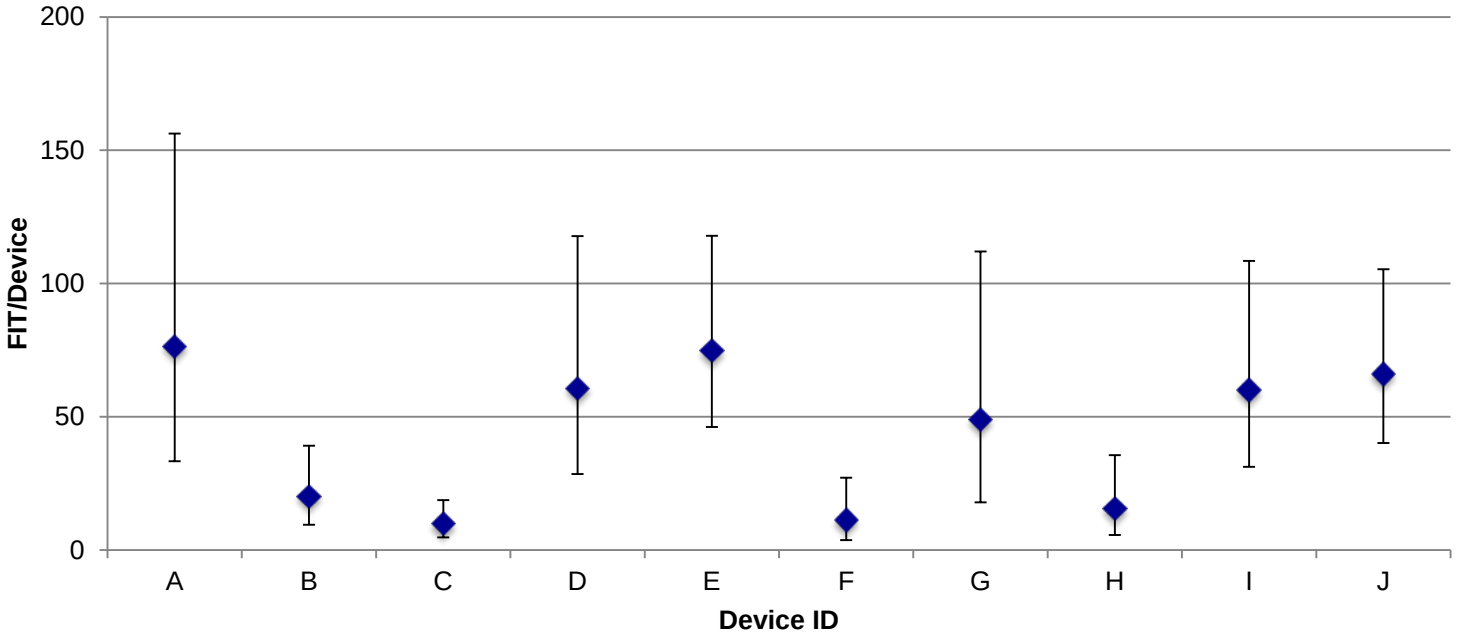
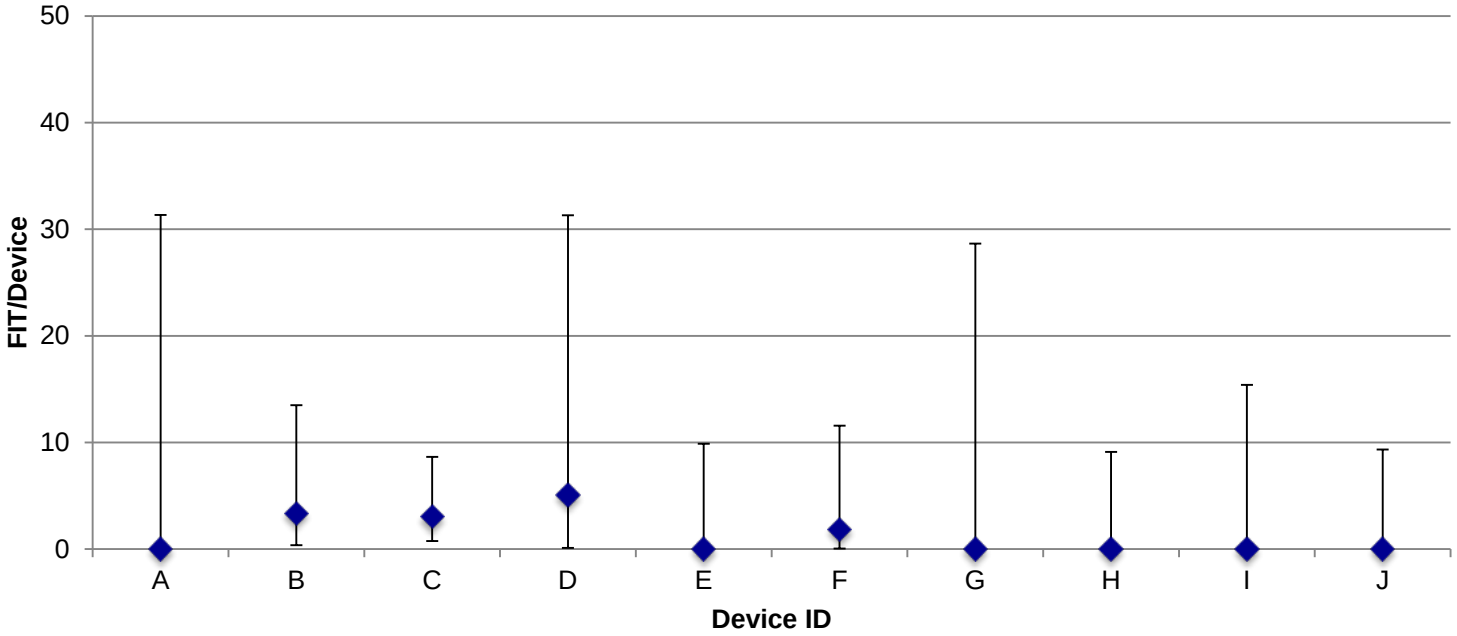
Backup Slides

Radiation Test Results

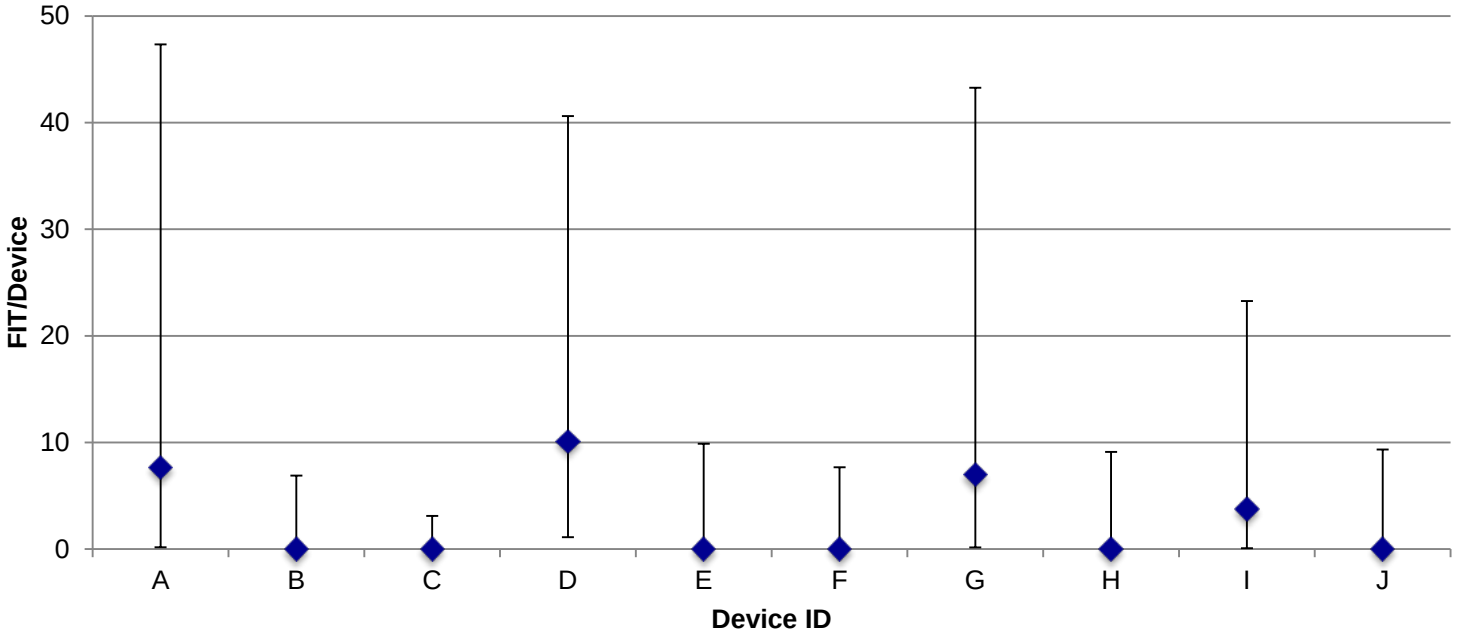
Read/Write Errors (detected)



Radiation Test Results
Hang



Radiation Test Results
Brick



Radiation Test Results
Silent Errors