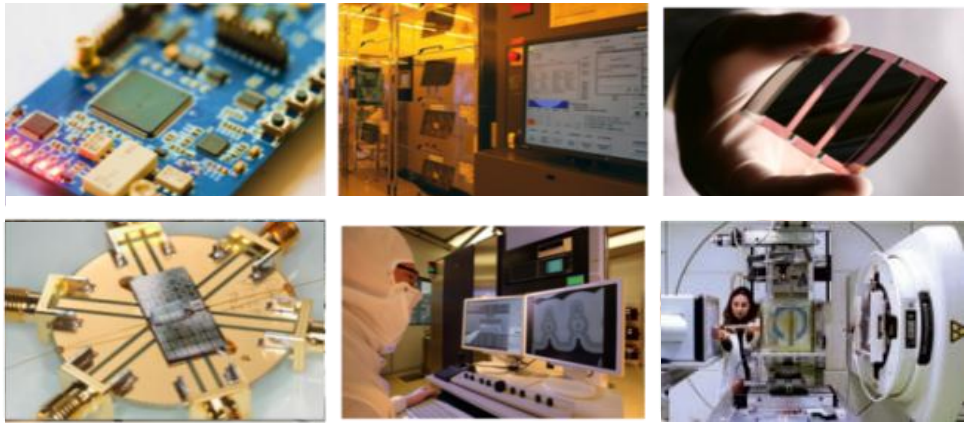
FROM RESEARCH TO INDUSTRY

cea tech

leti



New Advanced Non Volatile Memory Prototyping Services

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http://www.cea.fr/cea-tech

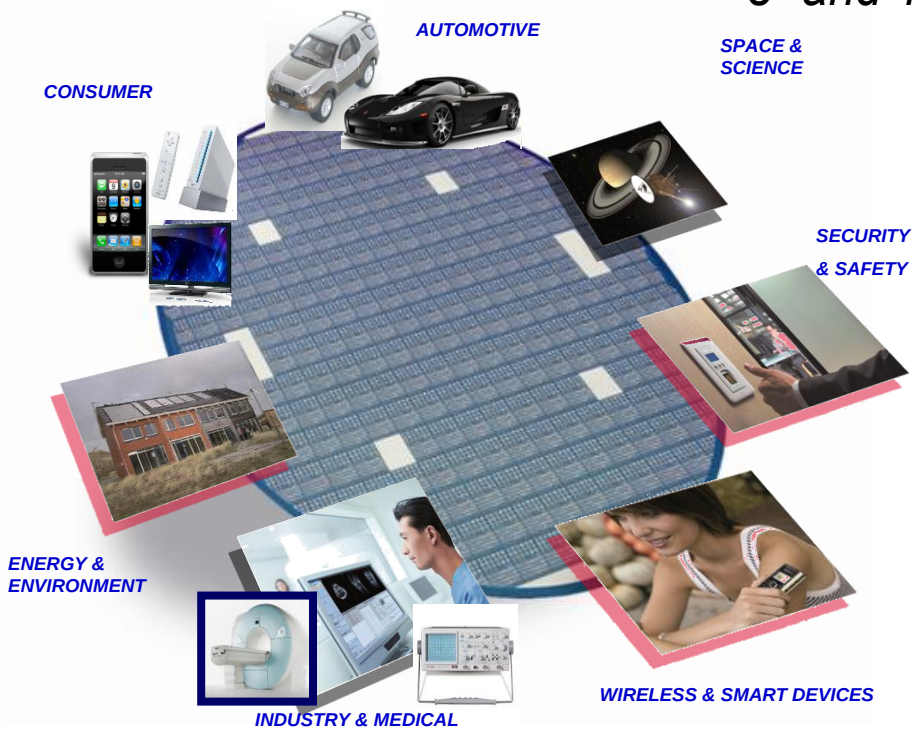
R&D in Micro & Nano technologies on state of the art industrial tools

8" and 12" technology platforms

1 800 researchers
1 300 on LETI payroll

300 M€ budget
~ 40 M€ CapEx

~300 patents / year
Portfolio > 2,200 patents
40 start-ups



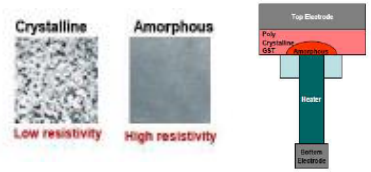
Unique capabilities for prototyping :

- > FDSOI CMOS (beyond <28 nm node)
- > 3D Integration & chip stacking
- > Silicon Photonics
- > Mems
- > IC Design

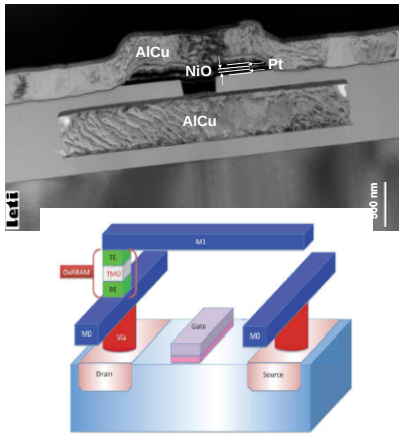
- Applications (medical devices, telco/IoT, automotive, security, ….)

A proven record of international successful partnerships

Phase-Change Memories



OXide-Resistive RAM



Customize materials

Innovative design

Material Analysis

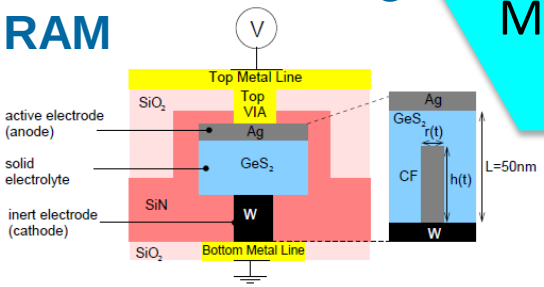
Future solutions for NVM

TCAD & Modeling

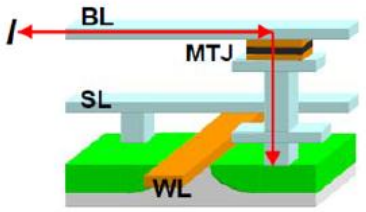
Critical module devlpmt

Specific Electrical Test

Conductive-Bridge RAM



STT-RAM

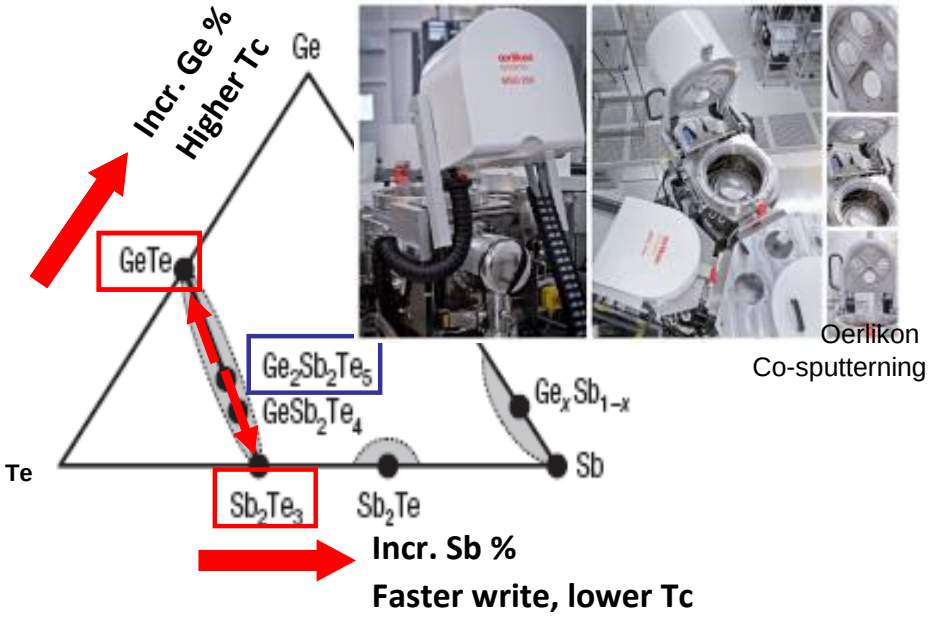


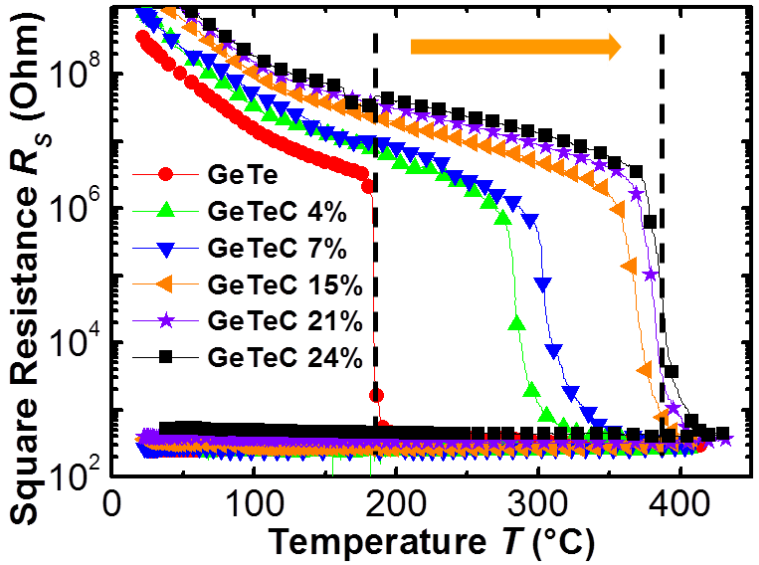
spintec
SPIN IN ELECTRONICS

A wide tool box which enables a **customized** research with **our partners** and a **benchmark** between different technological solutions

PCM: Memory stack Engineering for High-Temperature specs

Improving Data-retention @ High Temperature → soldering reflow & automotive specs (LETI/ST-Microelectronics collaboration)





L. Perniola et al., IEDM 2012

G. Navarro et al., IEDM 2013

Retention time comparison:

85°C — 110°C — 127°C — 154°C

data retention of 10 years at :

$Ge_2Sb_2Te_5$
- electrical contrast > 10^2
- endurance > 10^6 cycles
- SET speed ~ 100ns

$Ge_{50}Te_{50}$
- electrical contrast > 10^3
- endurance > 10^6 cycles
- SET speed < 30 ns

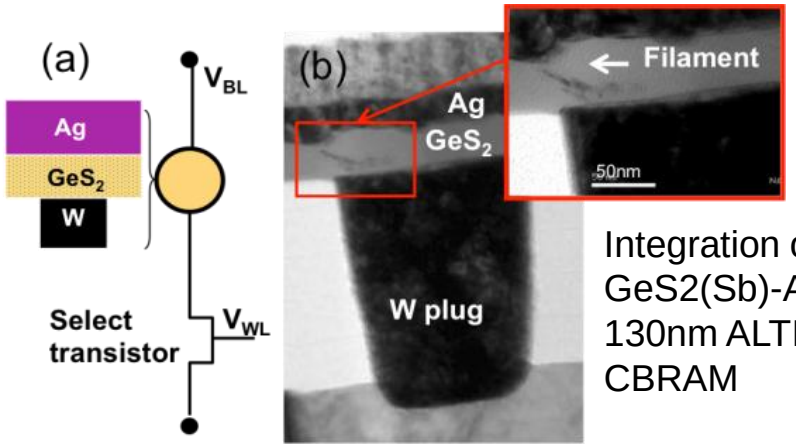
C(10%)-GeTe
- 30% I_{RESET} reduction / GST

$Ge_{30}Te_{70}$
- 25% I_{RESET} reduction / GST
- SET speed ~ 100-1000ns

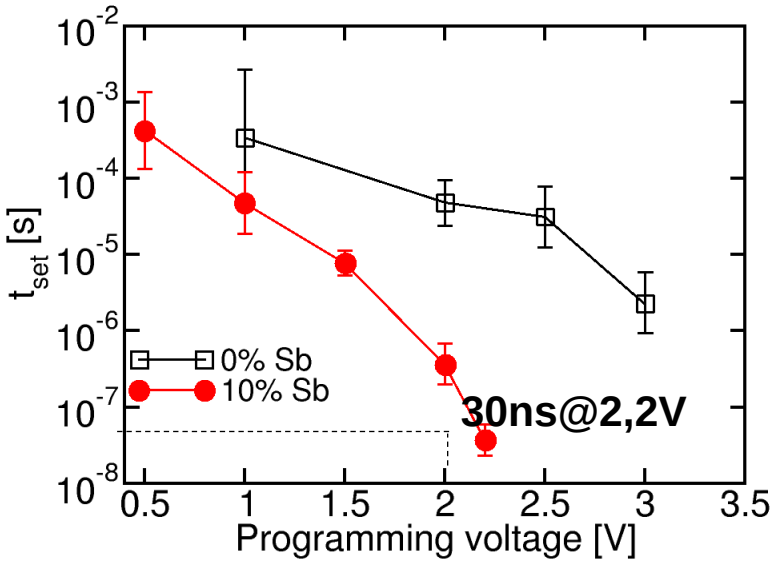
N(2%)-GeTe
- electrical contrast > 10^2
- SET speed < 50 ns
- data ret. automotive spec.
- ~~GeTeN2% good for SMPS~~ soldering (245°C for 30s)

Target : Improve SET/RESET speed & thermal stability (LETI/ALTIS collaboration)

	SET / RESET	Consumption
GeS_2	SET: 30µs @ 2.5V RESET: ~100ns @ -1.5V	**1nJ @ 2.5V**
GeS_2 (Sb10%)	**SET: 30ns @ 2.2V** **RESET: ~100ns @ -1.5V**	**0.66pJ @ 2.2V**

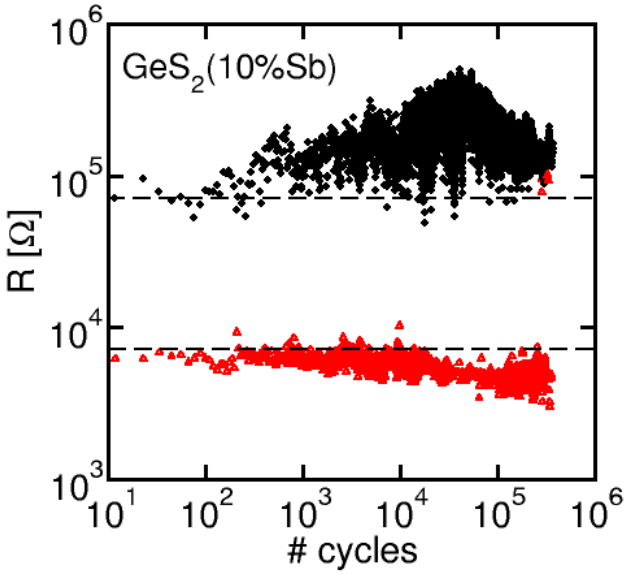


Integration of GeS2(Sb)-Ag 130nm ALTIS CBRAM



10%Sb doping → **t_{sw}=30ns@2, 2V** (~3 decades less than GeS_2)

Endurance

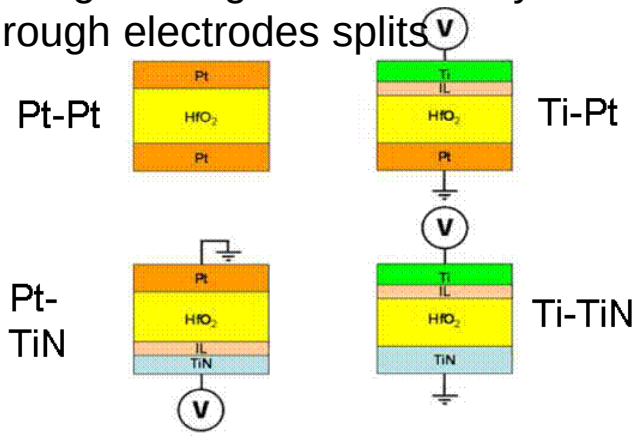


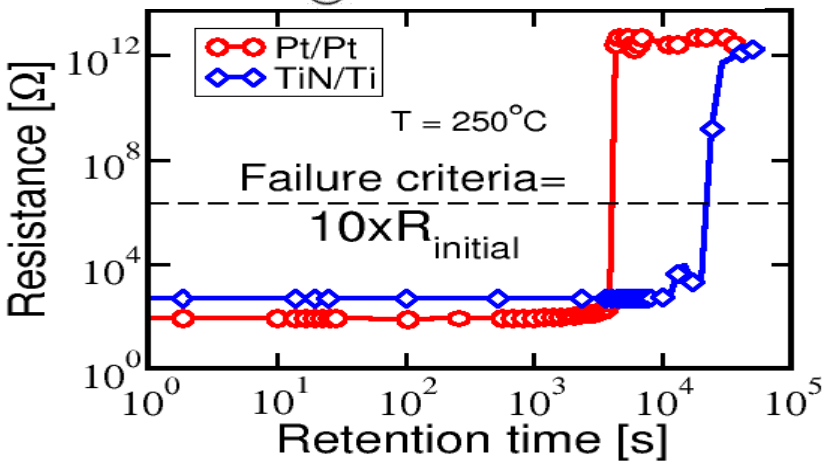
E.Vianello et al., IEDM 2012

OxRAM: Memory stack Engineering for variability reduction

- **Memory stack variation**

→ Engineering the O-vacancy content through electrodes splits

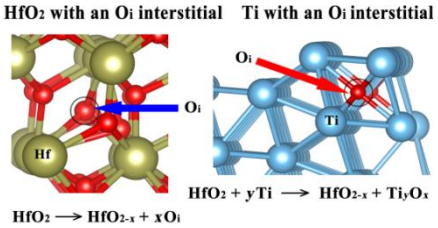




- **Experimental results**

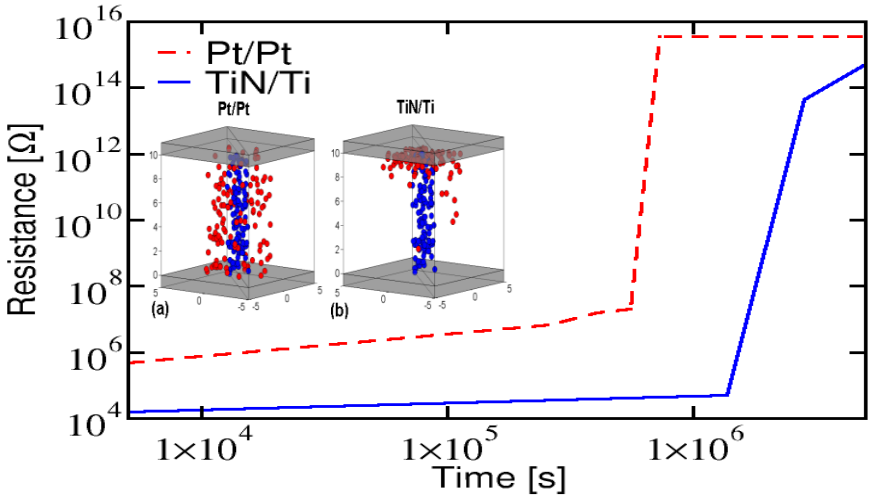
→ Retention improvement with Ti wrt Pt top electrode

B. Traore et al., IRPS 2013
C. Cagli et al, IEDM 2011



- **Ab initio calculations**

→ Ti acts as an O gettering layer during filament formation. Lower concentration of V(O) around the filament



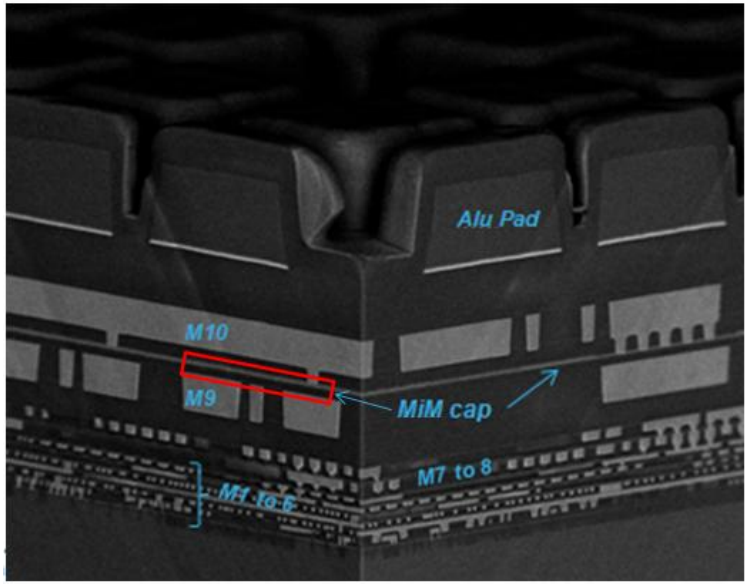
- **Physical device modeling**

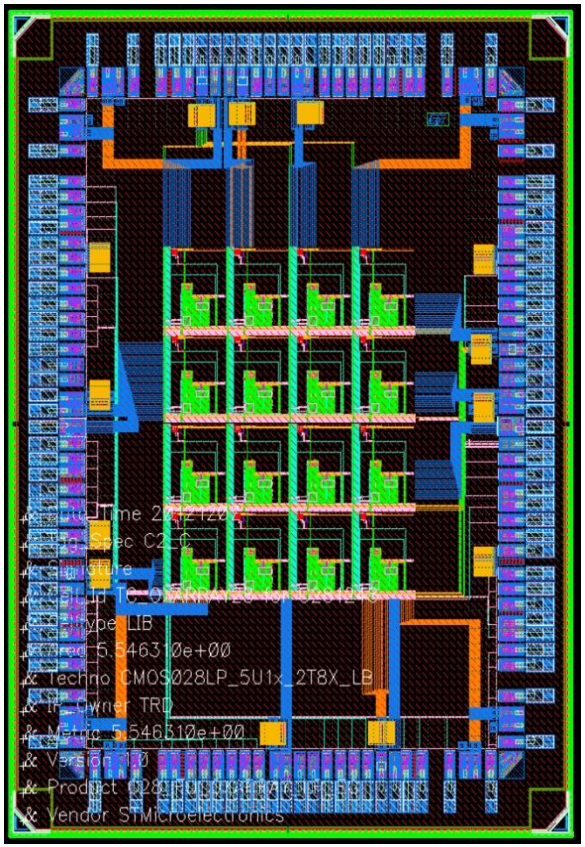
→ Improved filament stability and retention due to lower V(O) concentration in the HfO2 resistive layer

OxRAM last achievement

→ 16 kbit in ST 28 nm node test vehicle

- Back end integration (MIM 2 masks).
- Low number of process steps.
- 16 CUTs of 1kb/28 nm each are integrated into a digital testchip designed by ST



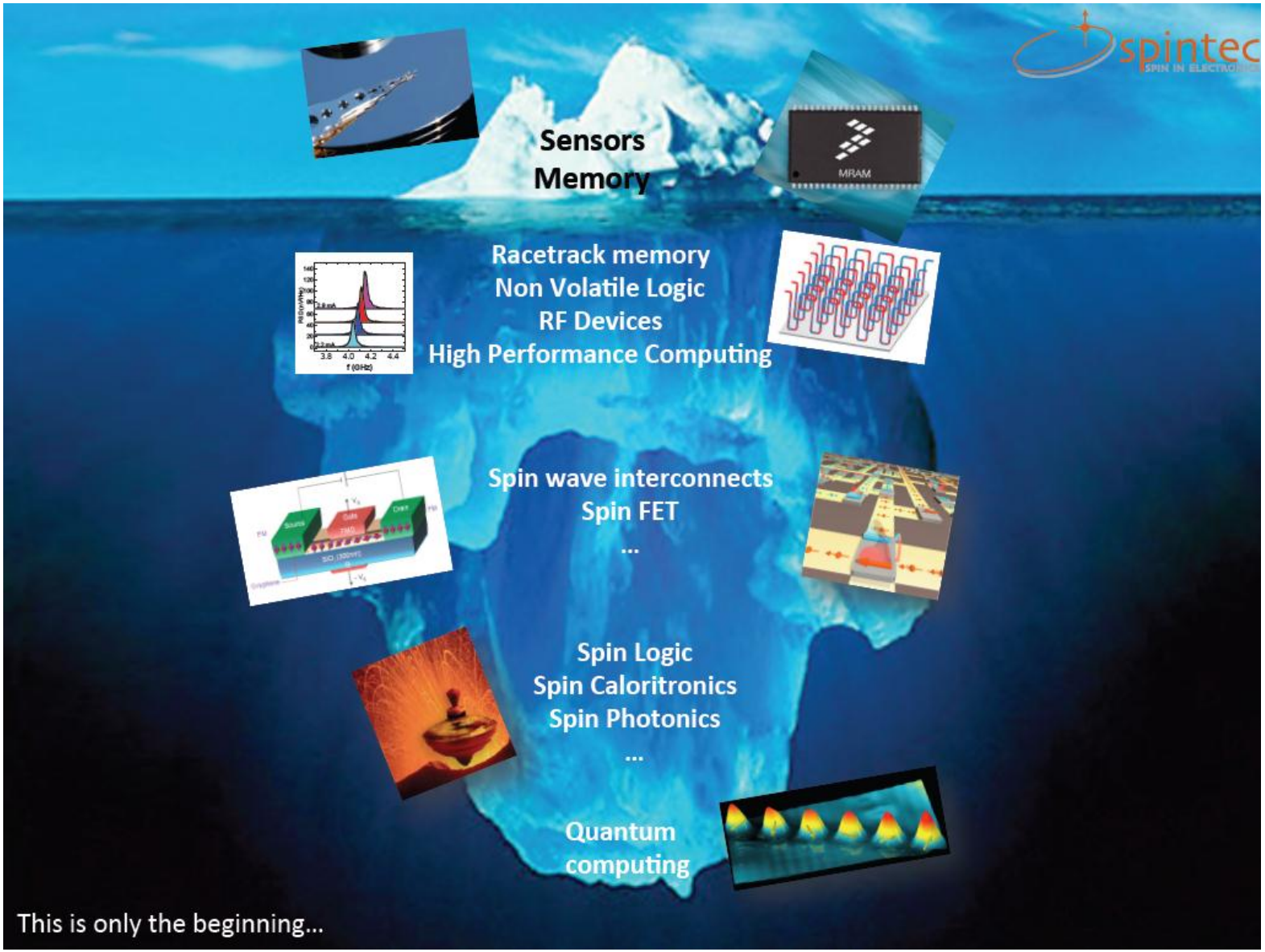


Wafer exchange:

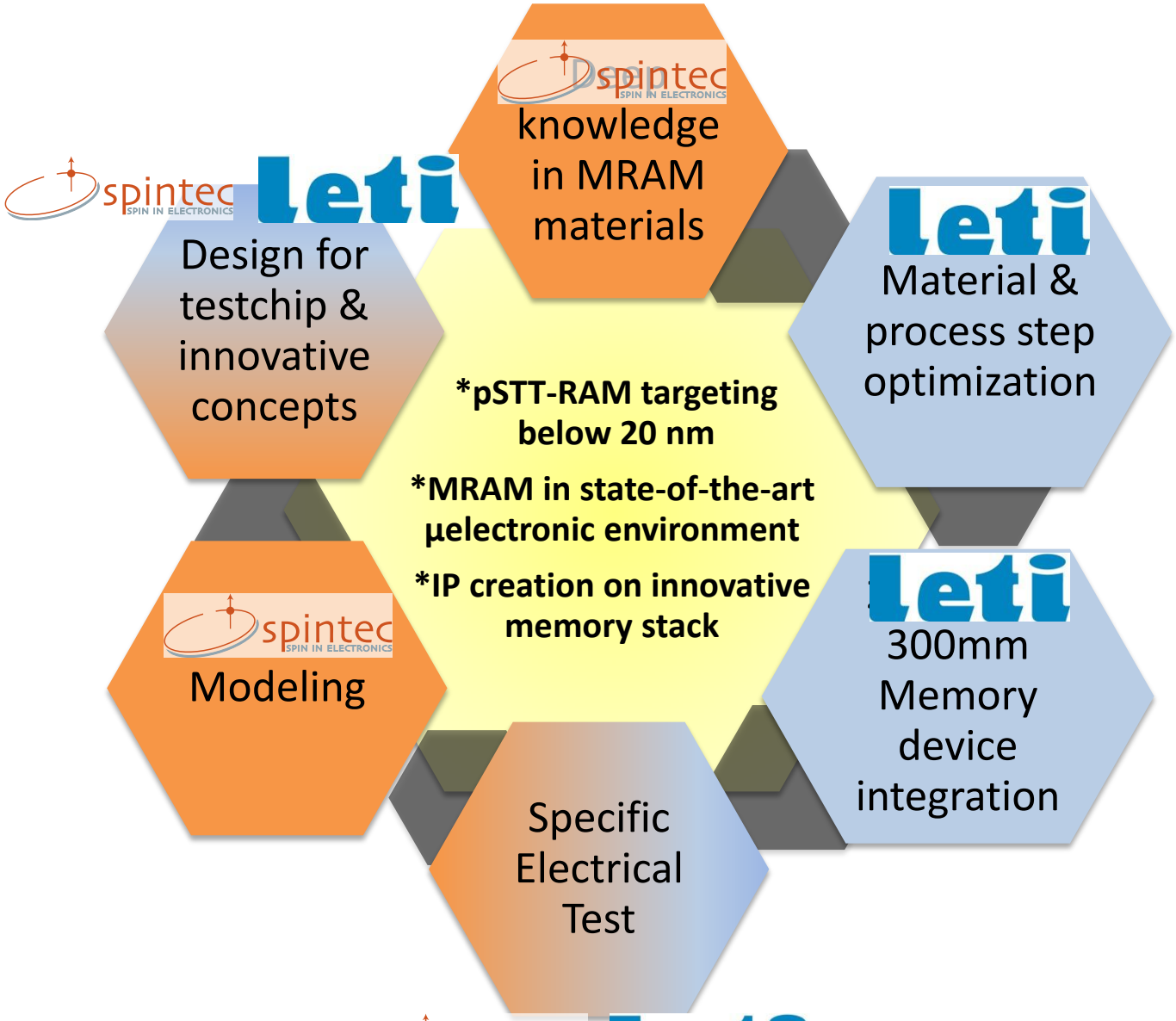
- Basewafers with CMOS 28 nm fabricated in ST
- LETI deposition of HfO2/Ti/TiN stack
- ST finishes BEOL up to pads

Courtesy of P. Candelier, Leti Memory Workshop 2014

COOPERATION WITH SPINTEC



LETI SPINTEC PARTNERSHIP



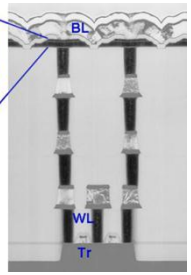
« MEMORY ADVANCED DEMONSTRATORS » → MAD

Design complexity

Versatility (different selectors, voltage/current/time variations…)

Single Cell 1T1R

- Material/ interfaces assessment
- NVM module analysis
- « Tailored » electrical tests



Small arrays & Crossbar (ex: 8x8)

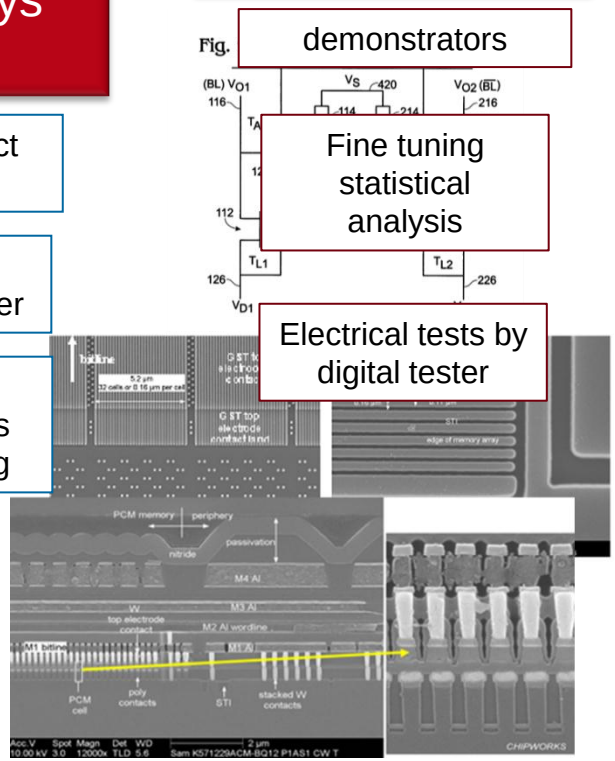
- Neighbors effect deep investigation
- Direct NVM access
- « Tailored » electrical tests

Large arrays (~Mb)

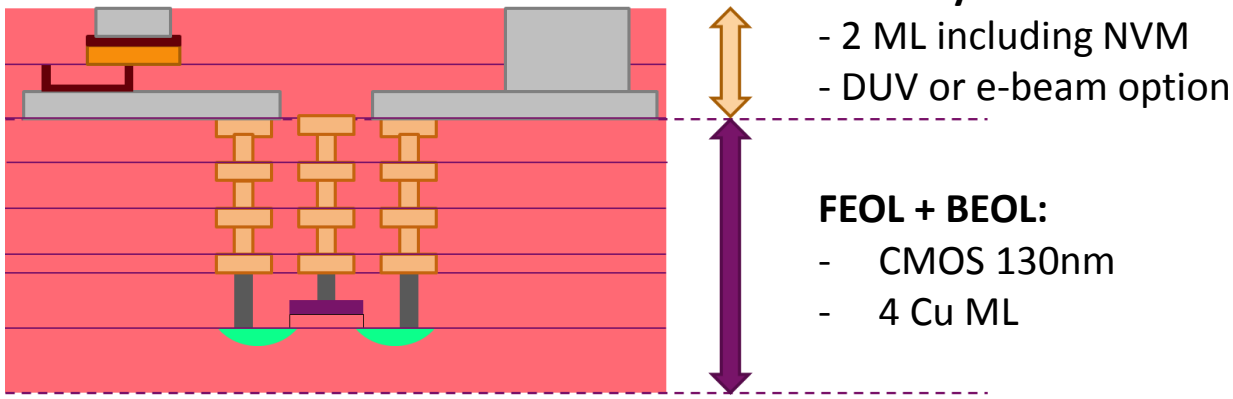
- Statistical effect acquisition
- NVM access through decoder
- « tailored » electrical tests after decoding

Complex memory circuits (Auto-test,…)

- Fig. demonstrators
- Fine tuning statistical analysis
- Electrical tests by digital tester



Reliable test vehicle for fast material screening for all major RRAM families (CB-OxRAM, MRAM, PCRAM)



Memory module:
- 2 ML including NVM
- DUV or e-beam option

FEOL + BEOL:
- CMOS 130nm
- 4 Cu ML

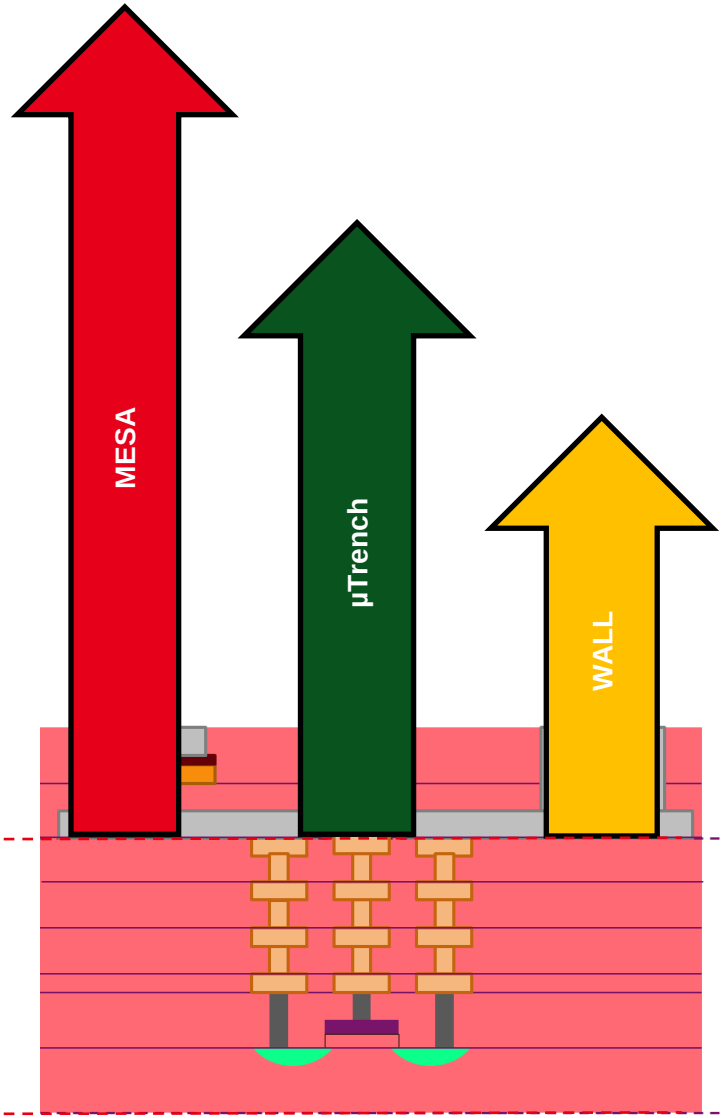
✓ 4 copper interconnects: possibility to make complex routing for complex design

Possibility to have Mb memory arrays to accumulate statistics

✓ FEOL features NMOS and PMOS with high yield

✓ Cycle time depending on priority: down to ~9 weeks in P1

MAD integration flows tailored for OxRAM, CBRAM, MRAM and PCRAM



Different ReRAM integrations

same CMOS

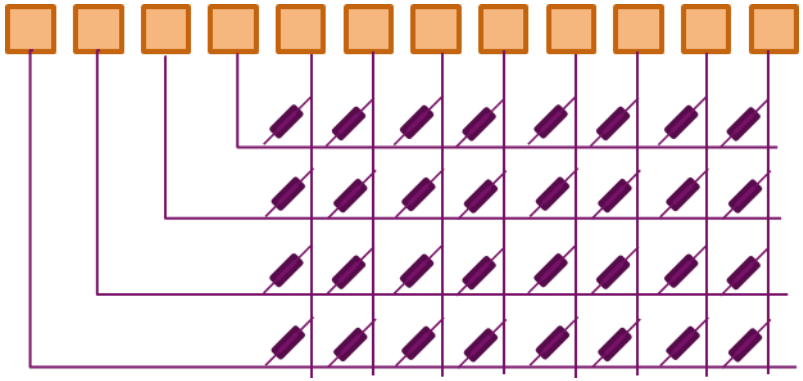
Memory module:
- 2 ML including NVM
- DUV or e-beam option

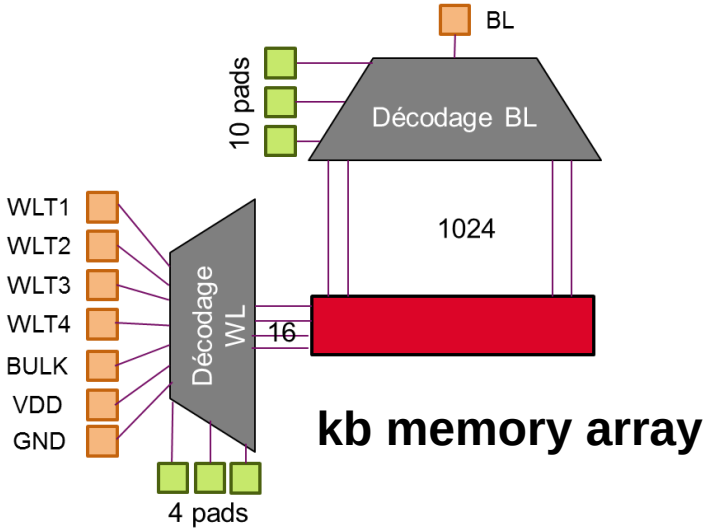
FEOL + BEOL:
- CMOS 130nm
- 4 Cu ML

MAD exemples & specifications

Exemples

4x8 crossbar selector-less

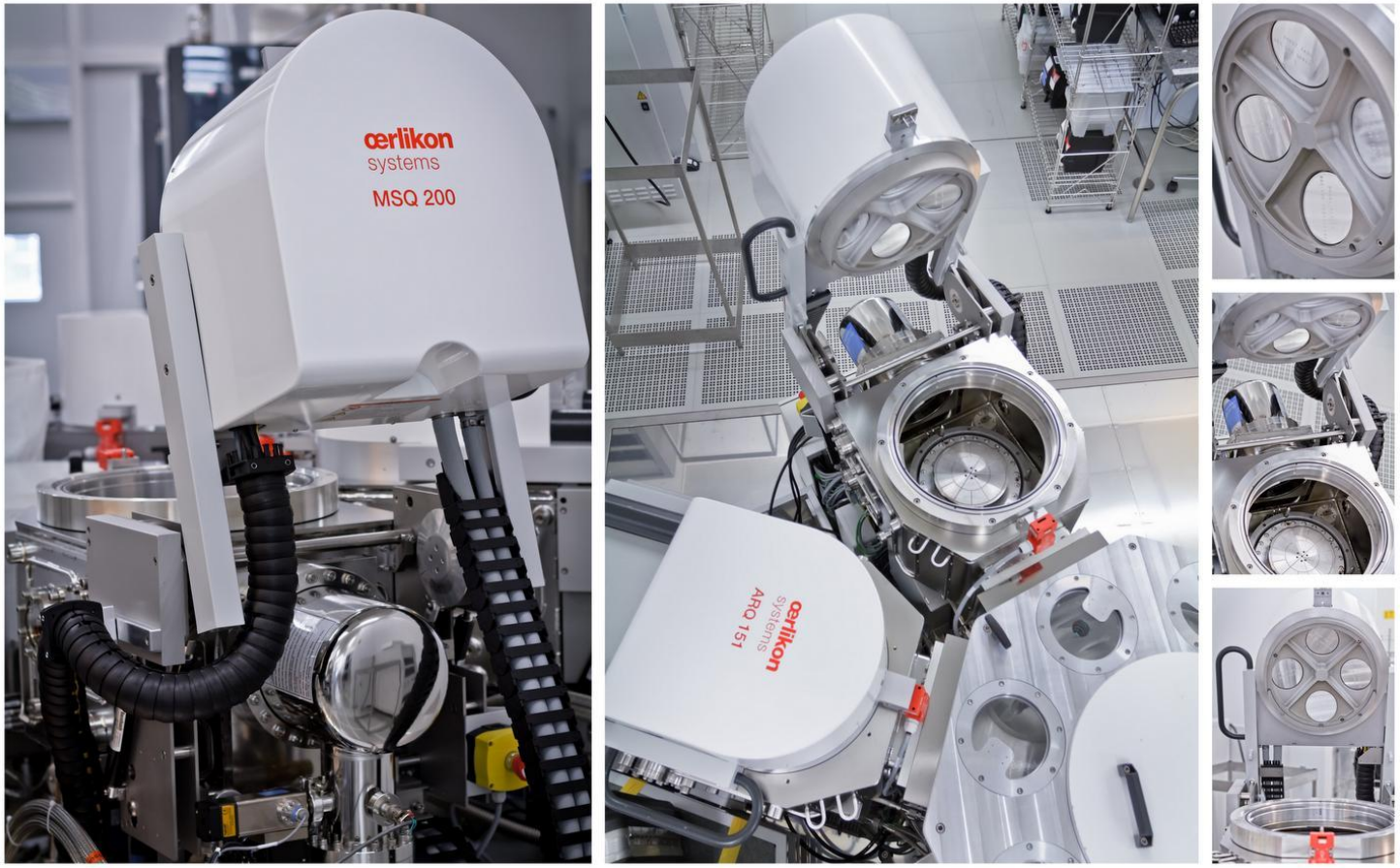




kb memory array

TECHNOLOGY:	**CMOS 130nm**
Spec. process char.:	**Gate length : 130nm (drawn), 130nm (effective)** **Triple Well** **Power supply : 1. 2V for Digital, 4.6V for Analog application** **Multiple Vt transistor offering (Low Power, Analog)** **Threshold voltages (for 2 families above) : VTN = 700/697mV, VTP = 590/626mV** **Isat (for 2 families above) : TN : 280/658uA/um; TP : 104/333uA/um** **4 Copper metal layers in standard** **Fluorinated SiO2 Inter Metal dielectrics** **2 specific implant levels : NDRIFT & PDRIFT** **Double gate oxide for analog features**

Oerlikon Cluster Line 200mm (CLN200)



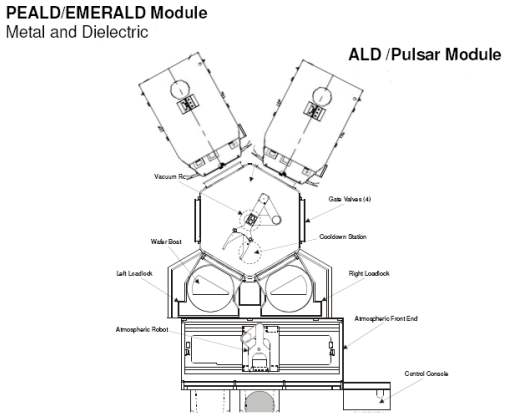
Courtesy of V.Baret - LETI

- Tool delivered & qualified end of october ’11 @LETI
- Material engineering for memories applications (CBRAM, PCRAM, OXRAM)
  - Co-sputerring capability
  - Standard planar PVD module for capping, electrodes …

300 mm ALD & PEALD tools for OxRAM

- **Equipment cluster ASM POLYGON1 – 2 deposition reactors**
  - ALD reactor (Atomic Layer Deposition)
  - PEALD reactor (Plasma Enhanced Atomic Layer Deposition)

  - Capability 300mm wafers - wafers 200mm : samples on adaptors



Precise composition of the films

Good uniformity <2% (300mm)

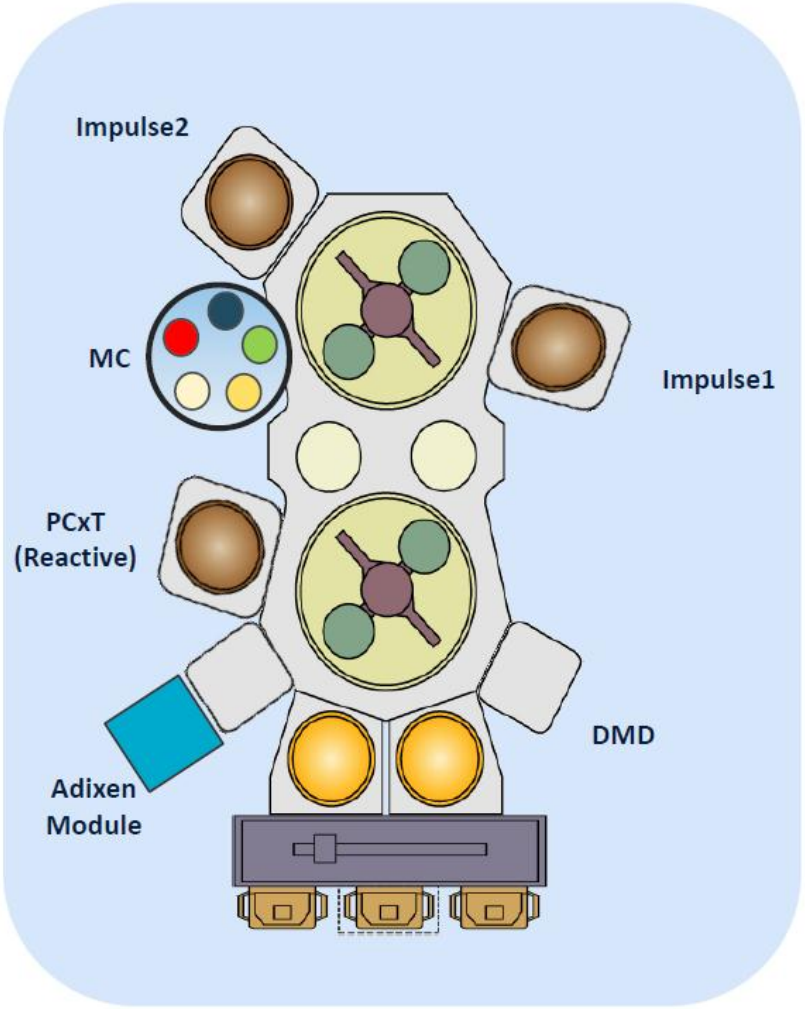
Excellent repetability

HfO_2, Al_2O_3, nanolaminates, HfAlO (ALD)

ZrO_2, Ta_2O_5, SiO_2 (PEALD)

TaCN (PEALD)

300 mm PVD Endura platform



Tool configuration

- ✓ 1 Degassing module (DMD) up to 400°C
- ✓ 1 Preclean system (ICP soft etch)
- ✓ 1 Multi-Cathode chamber (5 cathodes with RF, DC, pDC generators) – O2, N2 reactive processes. Up to 3 target co-PVD
- ✓ 2 pDC chambers (Impulse) – O2, N2 reactive processes
- ✓ Vacuum transfer module for plugging the Adixen vacuum carrier

Objectives

Conventional Impulse PVD chambers → electrodes & fixed composition memory element.

300mm CoSputtering chamber for memory material engineering and flexibility

➔ **Composition fine tuning, material screening**

➔ **Cost Of Ownership** : smaller targets (easier to manufacture), longer life time for desired targeted compo, etc.

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THANKS!

QUESTIONS?