How to Extend 2D-TLC Endurance to 3,000 P/E Cycles

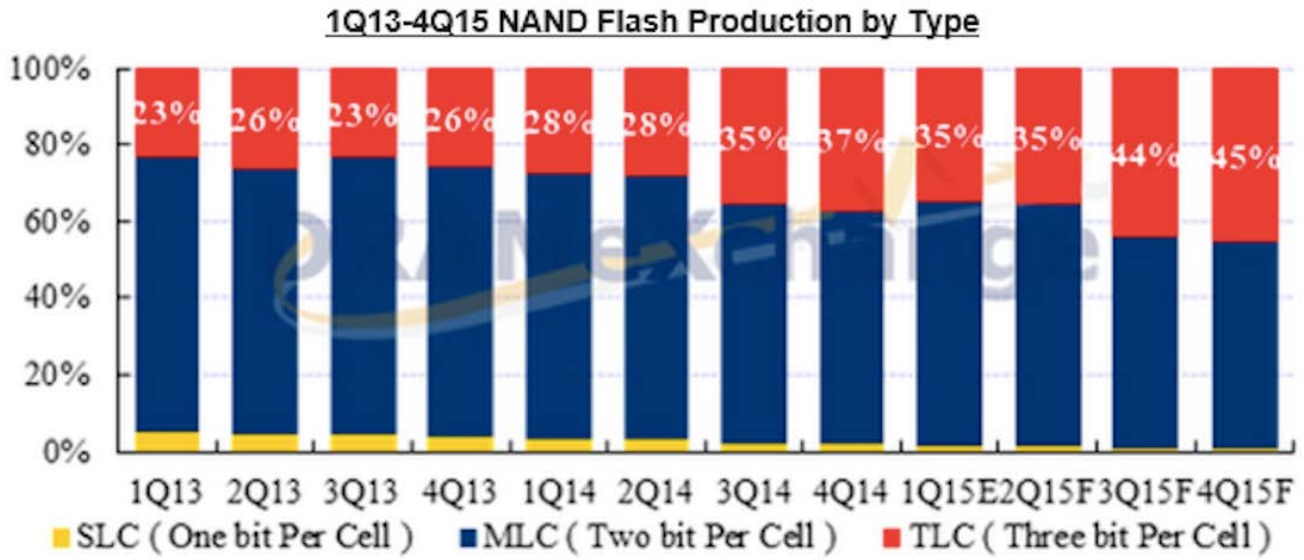
Federico M. Benelli

CTO, NandExt

Outline

- TLC Market
- TLC challenges
- TLC^{10} Technology Platform:
  - Best In Between (BIB)
  - Page-based CLAP-LDPC
  - ThermoNAND
- Summary

TLC Market



(Source: DRAMeXchange, March 2015)

- Because Flash technology shrink has slowed down during the last few years (3D push out!), migration to TLC has recently gained a lot of traction in the market.

TLC Challenges

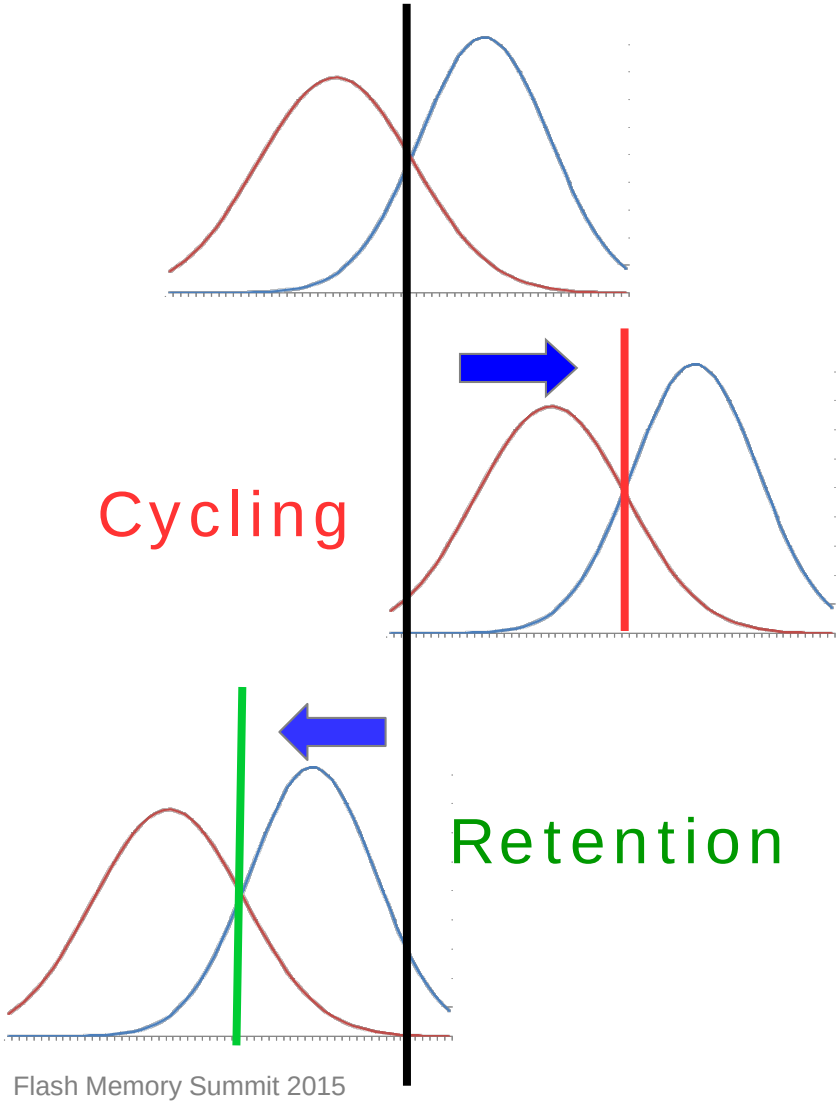
- TLC reliability prevents its adoption in systems where more than few hundreds of Program/Erase (P/E) cycles are required.
- In essence, consumer TLC targets read-intensive applications.
- More attractive applications, like Data Centers, need MLC-like reliability, i.e. 3,000 P/E cycles.

Flash Memory SUMMIT

TLC^{10}

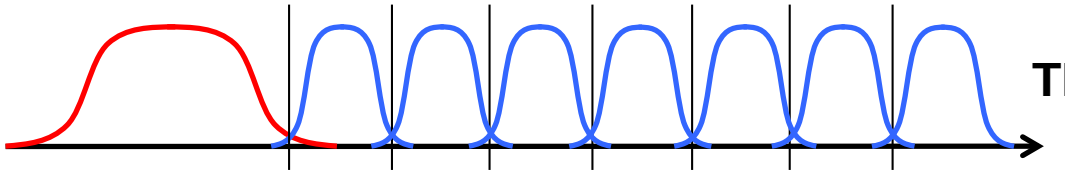
- TLC^{10} Technology Platform is a suite of proprietary NAND reliability enhancement technologies.
- TLC^{10} extends TLC reliability by 10x, from 300 to 3,000 P/E.
- At FMS ‘15 we introduce the following features:
  - Best In Between (BIB)
  - Page-based CLAP-LDPC
  - ThermoNAND

BIB – Best In Between



- Flash vendors suggest Vt-shifts values (sometimes called read retry).
- Problem is that these values target 300 P/E cycles.
- At 3,000 P/E cycles reference voltages should be in a completely different place.

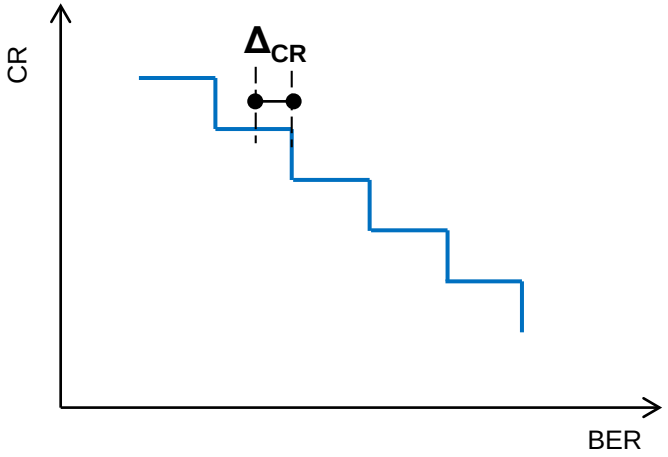
BIB – Best In Between

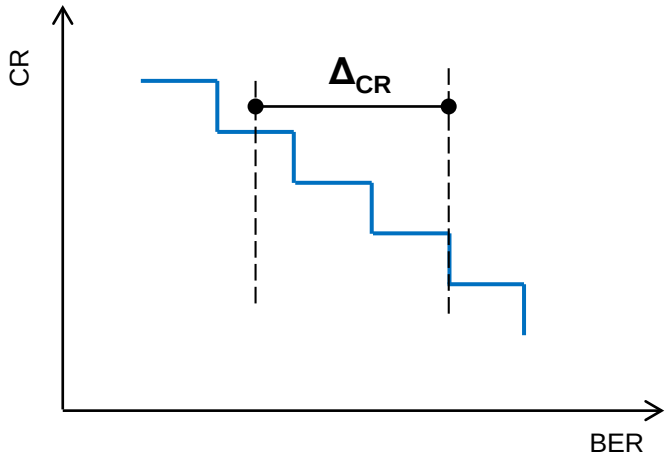


- Finding the right spot for each reference voltage is not trivial, because the number of combinations, given the 7 reference voltages, is huge.
- In order to tackle this problem, we developed a tool that allows a quick and reliable definition of the right Vt-shift strategy, based on NAND silicon characterization data.

Multi Code-Rate LDPC Challenge

- LDPC w/ Multi Code-Rate (CR) is a great solution to reduce capacity consumption
- Multi-CR works fine in theory, but "switching margin" Δ_{CR} is a killer
- Δ_{CR} burns capacity sooner than needed
- Some Flash controllers provides a lot of CRs, but most of them fall within Δ_{CR} and can't be used

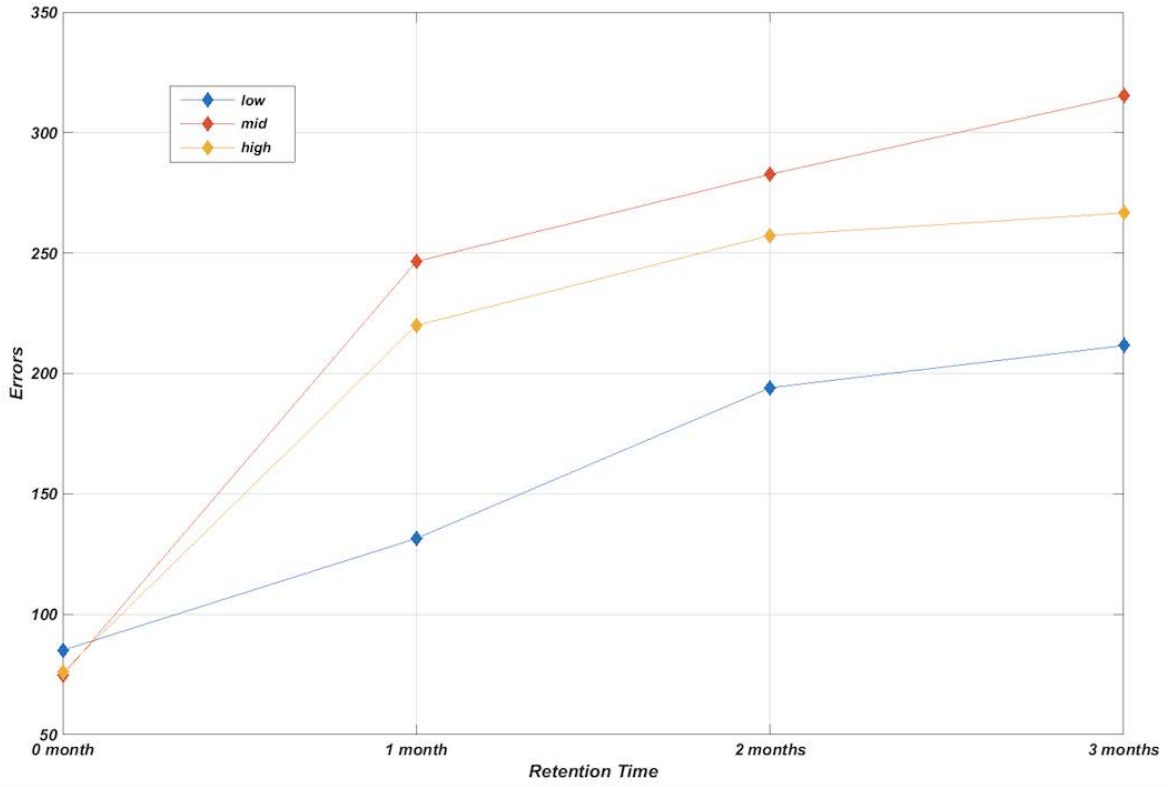




CLAP-LDPC

- In order to exploit the full benefit of Multi-CR LDPC, at FMS ‘14 we introduced CLAP-LDPC (CLosed Abstracted Proactive LDPC)
- CLAP-LDPC implements advanced decoder / H matrix
- “Closed” -> decisions are based on decoding parameters -> switching margins are strongly reduced
- “Abstracted” -> first order, it doesn’t depend on a specific NAND technology
- “Proactive” -> it automatically triggers the CR change

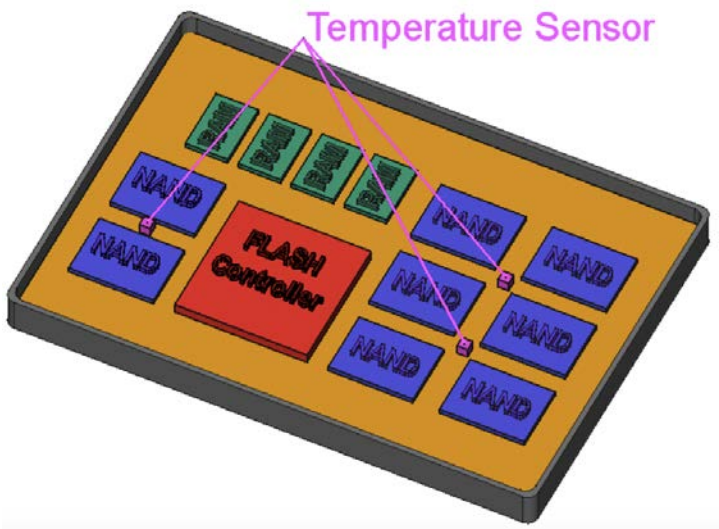
Page-based CLAP-LDPC

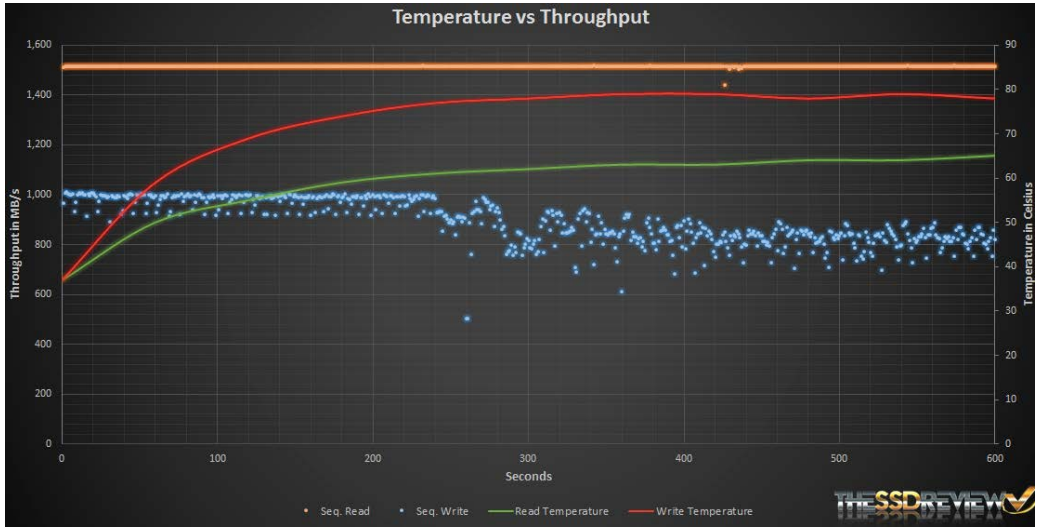


- Low/Mid/High pages don't exhibit the same BER, under the same ageing conditions
- We optimize Code Rate per page category.
- CLAP-LDPC is independently applied to Low/Mid/High pages

NAND raw BER vs. Temperature

- NAND raw BER is strongly influenced by NAND Tcase.
- Standard solution is to add Temp sensors to SSDs for real time monitoring





ThermoNAND

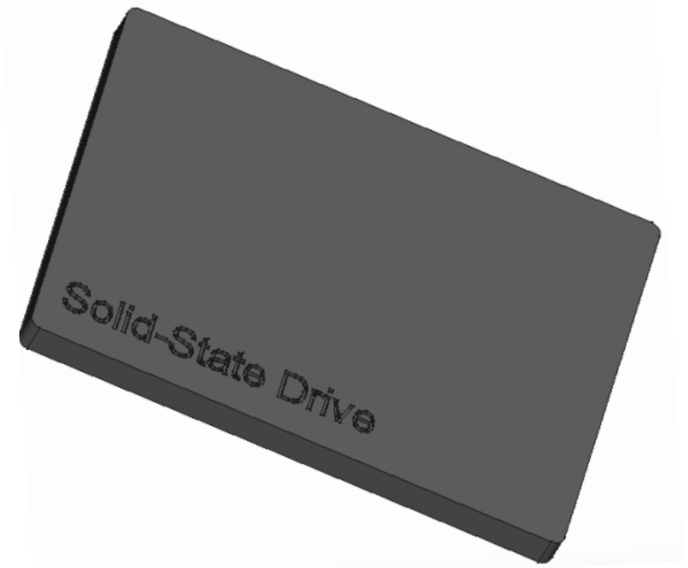
TLC10

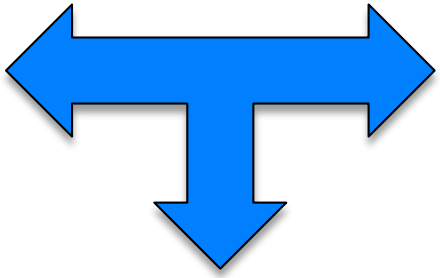
- NAND management algorithms need to keep NAND Temp into account.
- Does a Temp variation over 1s affect reliability? How about 1 minute?
- If Temp changes of 20° C in a “short” period of time, what is the “effective” temp that we should consider?
- ThermoNAND answers all these questions and more… It basically outputs the right NAND Temp for Retention algorithms.

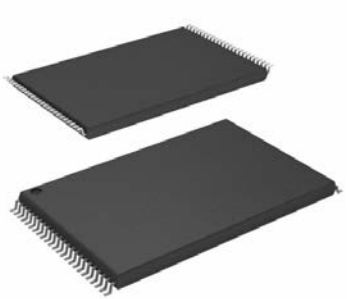
ThermoNAND

TLC10

- In order to come up with the right recipe, we had to run a lot of correlation experiments between SSDs and raw NANDs.







ThermoNAND

Summary

- TLC^{10} can extend TLC's lifetime by 10x
- TLC^{10} is a suite of proprietary NAND reliability enhancement technologies.
- Today we introduced 3 technologies:
- Best In Between (BIB)
  - to properly select the right reference voltages over life
- Page-based CLAP-LDPC
  - to optimize LDPC for Low/Mid/High Pages
- ThermoNAND
  - to identify the "effective" NAND Tca

TLC[10]

federico@nandext.com

Thank You