NAND Controller NFS

The changing world of Memory

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Altera Corporation

NAND trends

System Requirements

Memory, Storage Controller Overview

Controller Advantages

NAND Changes Many times in a Silicon Cycle

- The constant change in NAND processing makes it difficult to keep up at the controller level.
- The average SSD controller release is between 18 and 30 months.
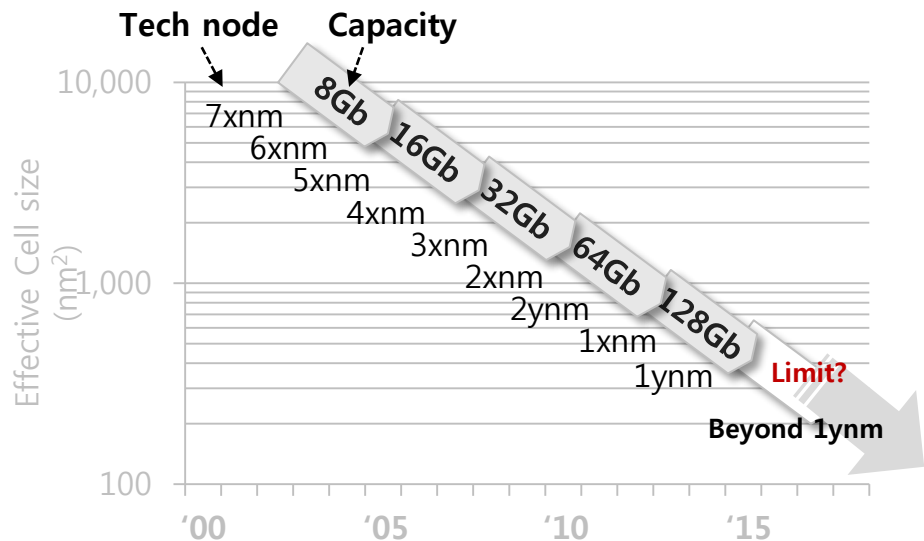- Error corrected NAND can limit performance.
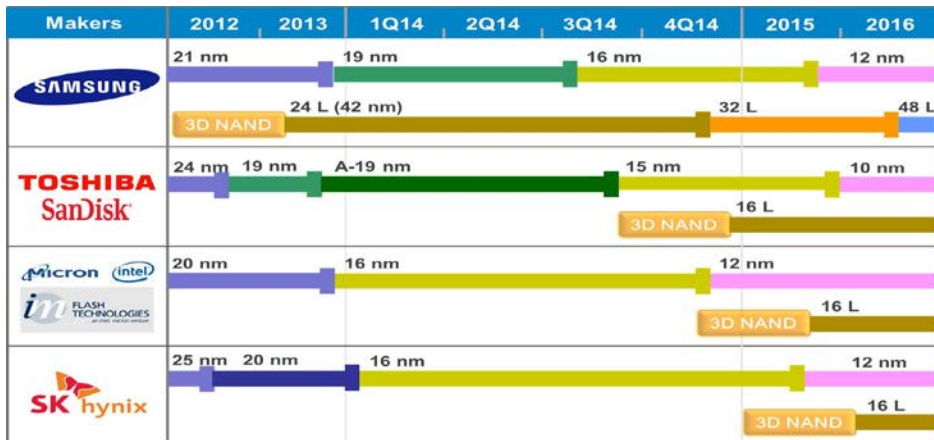
SanDisk NAND Memory Roadmap

- 1Y PRODUCTION IN 2013
- MAKING PROGRESS ON 1Z NAND, …
- AGGRESSIVE POST NAND RESEARCH AND DEVELOPMENT

SanDisk   ANALYST DAY || FEBRUARY 16, 2012   SLIDE 176
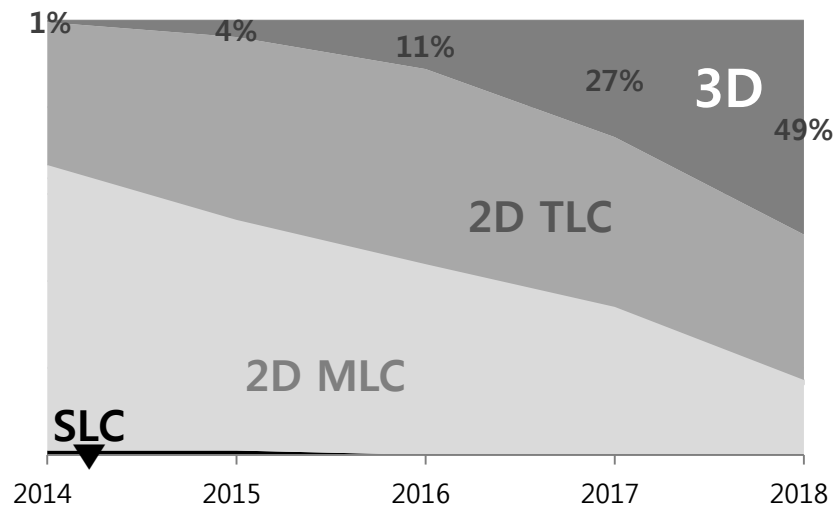
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NAND Technology Innovation

NAND Flash faces challenges to satisfy cost and capacity, another approach required to overcome technical limitations
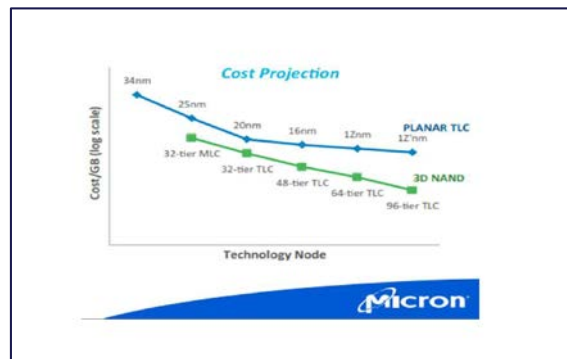
NAND Technology Trend

Tech node   Capacity

Effective Cell size (nm²)

10,000

7xnm
6xnm
5xnm
4xnm
3xnm
2xnm
2ynm
1xnm
1ynm

8Gb
16Gb
32Gb
64Gb
128Gb

Limit?

Beyond 1ynm

1,000

100

'00   '05   '10   '15

3D Portion Trend

[Unit : % of Total GB]

1%   4%   11%   27%   **3D**   49%

2D TLC

2D MLC

SLC

2014   2015   2016   2017   2018

Source : Gartner, Q1'15
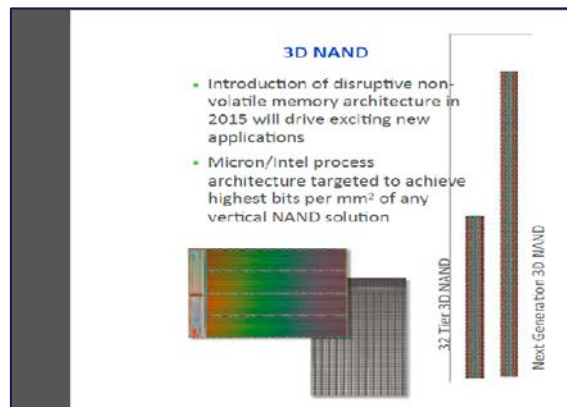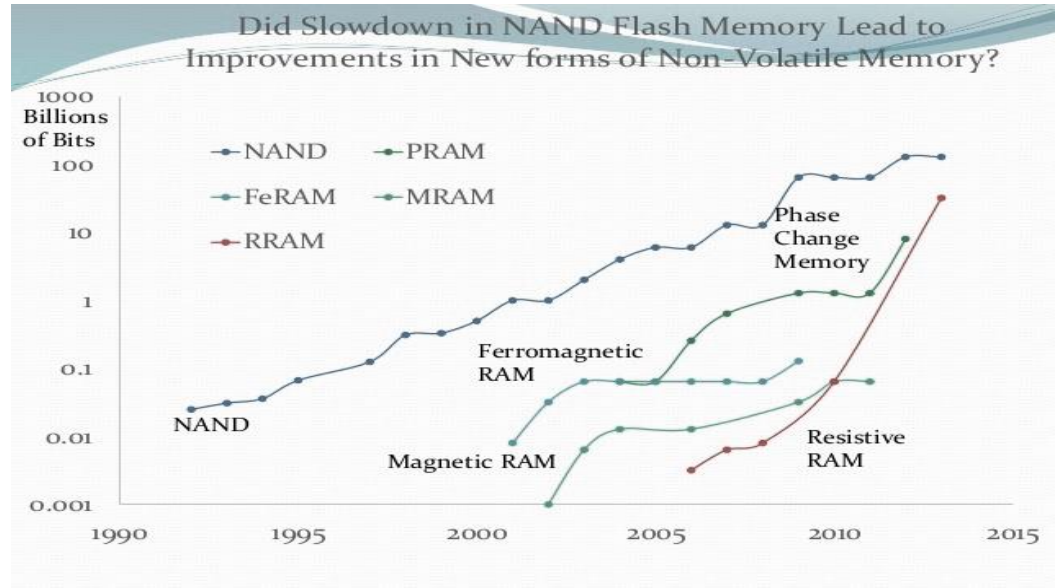
Storage The next Generation

The Biggest Memory/Storage Change in 10 years

- Micron Technology presented some new 3D NAND cost and road map information at the company's Analyst Day on Friday, February 13.
- **Large Capacities** –Three times the capacity of existing 3D technology[1]—up to 48GB of NAND per die—enabling three-fourths of a terabyte to fit in a single fingertip-sized package.

Samsung started delivery of 3D NAND SSD for consumer applications

- 3D NAND technology uses floating gate cells and enables the highest-density flash device ever developed—three times higher capacity[1] than other NAND die in production.
- Enables gum stick-sized SSDs with more than 3.5 terabytes (TB) of storage and standard 2.5-inch SSDs with greater than 10TB.

Change Causes Disruption

- Time to Market
- Early adoption
- Application Explosion

3D NAND

- Introduction of disruptive non-volatile memory architecture in 2015 will drive exciting new applications
- Micron/Intel process architecture targeted to achieve highest bits per mm² of any vertical NAND solution

32 Tier 3D NAND

Next Generation 3D NAND

Cost Projection

Cost/GB (log scale)

34nm
25nm
20nm
16nm
1Znm
1Z°nm   PLANAR TLC

32-tier MLC
32-tier TLC
48-tier TLC
64-tier TLC   3D NAND
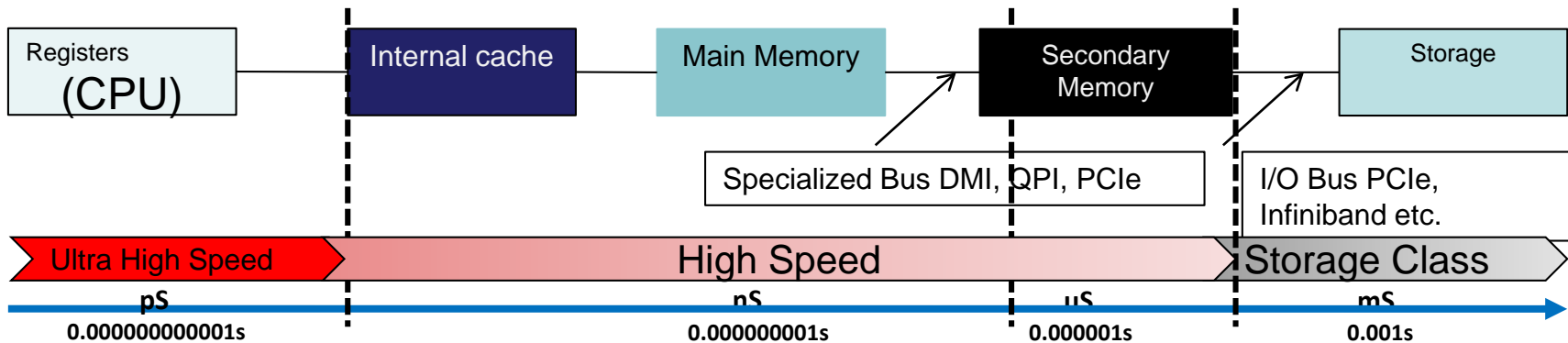96-tier TLC

Technology Node

Micron

Enter New Memory solutions (A new Dawn Awaits)

- Did the 14nm NAND delay drive these solutions to becomes next gen?
- Or did the need for more flexible memory and storage applications Drive this transition?
- New Memories are complementary to existing solutions
  - How to Adopt
  - Where do they go
- How do they fit in tomorrows Server/storage Architectures

Did Slowdown in NAND Flash Memory Lead to Improvements in New forms of Non-Volatile Memory?

— NAND — PRAM
— FeRAM — MRAM
— RRAM

Phase Change Memory

Ferromagnetic RAM

NAND

Magnetic RAM

Resistive RAM

Memory Hierarchy Design

More levels provide more opportunities

| Registers (CPU) | Internal cache | Main Memory | Secondary Memory | Storage |

Specialized Bus DMI, QPI, PCIe

I/O Bus PCIe, Infiniband etc.

Ultra High Speed | High Speed | Storage Class

| pS | nS | uS | mS |
| 0.000000000001s | 0.000000001s | 0.000001s | 0.001s |

- It is a tradeoff between Capacity, speed and and exploits the principle of locality.
- Attachment to CPU
 - Reduces OS awareness of I/O bus, fast large storage
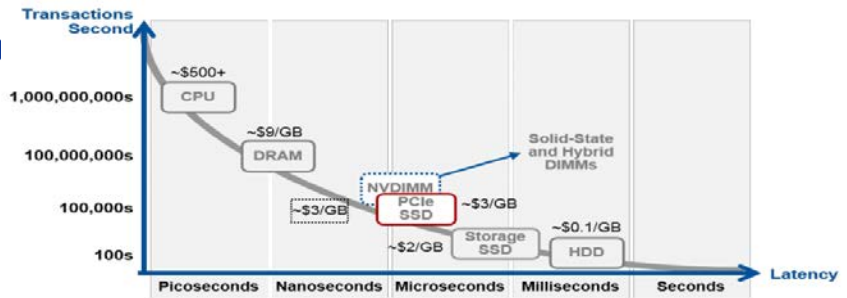
RAM Locality is King

- The cpu mostly waits for RAM
- Flash / Disk are
  100,000 …1,000,000
  clocks away from cpu
- RAM is ~100 clocks away
  unless you have locality (cache).
- If you want 1CPI (clock per instruction)
  you have to have the data in cache
    (program cache is "easy")
- This requires cache conscious
  data-structures and algorithms
  sequential (or predictable) access patterns
- Main Memory DB is going to be common.
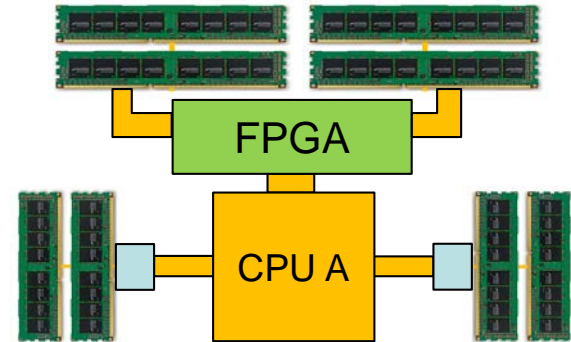
POC SSD Design
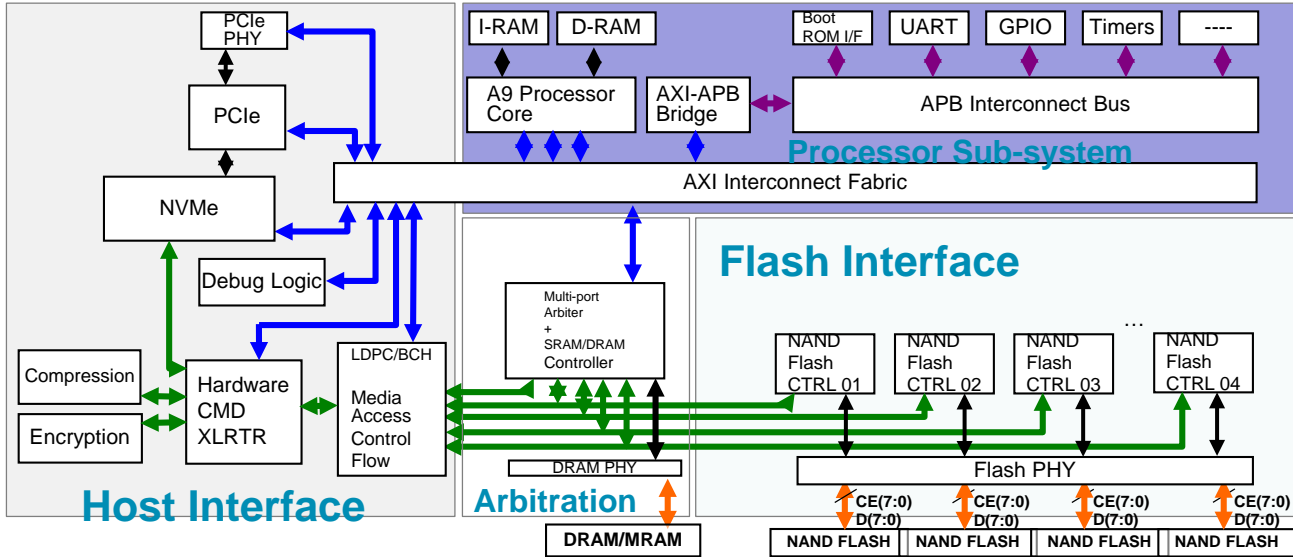
Arria 10 SOC the target devices would depend features can fit into arrays

• SX320 (Limited features, no compression or encryption)

• SX480 (with either compression or encryption)

• SX570 for full features

• New Nand Management scheme

Flexibility of the Design

- Number of NAND channels
- Compression, Encryption, ECC
- Optimized Commands
- NAND Command Q
- Packet transfer
- Processors functionality
- Memory use and function
- Optimized NAND access to system function
- DRAM and NVM memory support
- Performance tuning latency, Bandwidth etc.
- ROI based on new NAND technology and availability

Arria 10 HPS Block Diagram
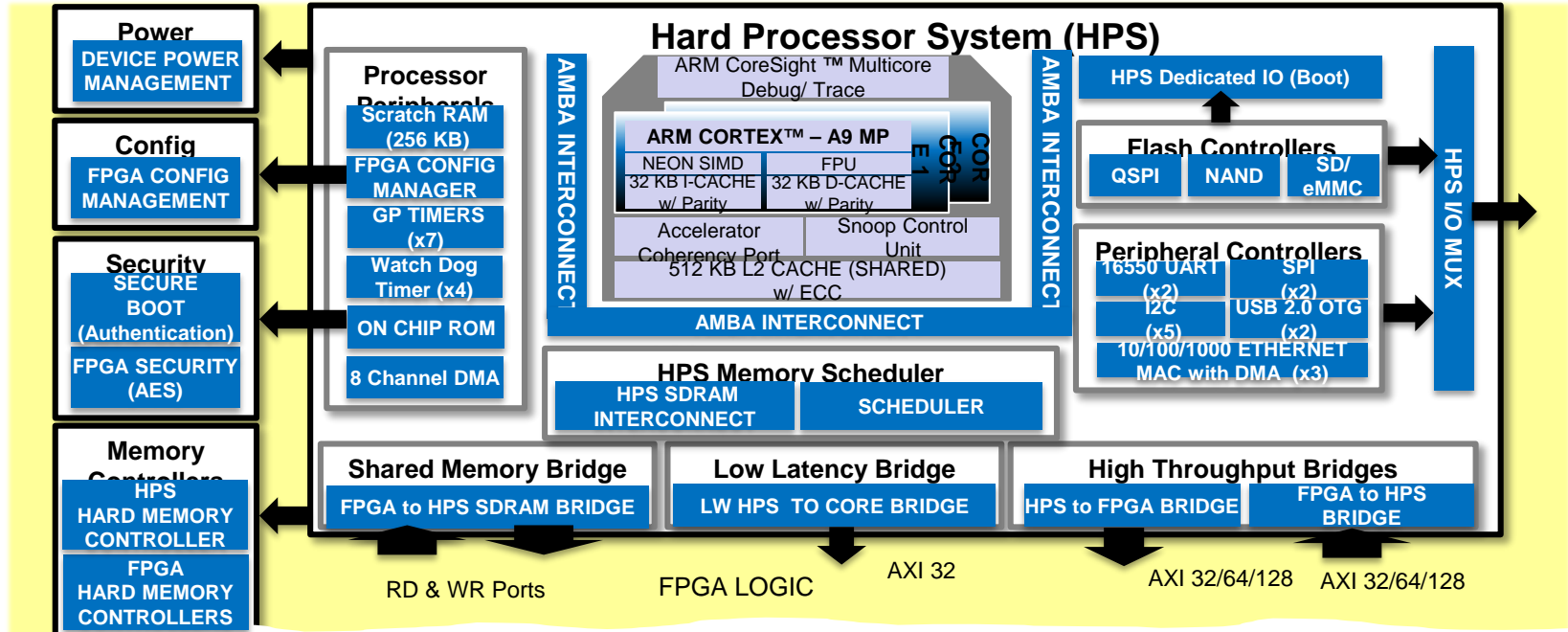
ECC vs NAND Management

Advanced NAND management for maximum Performance and Cost
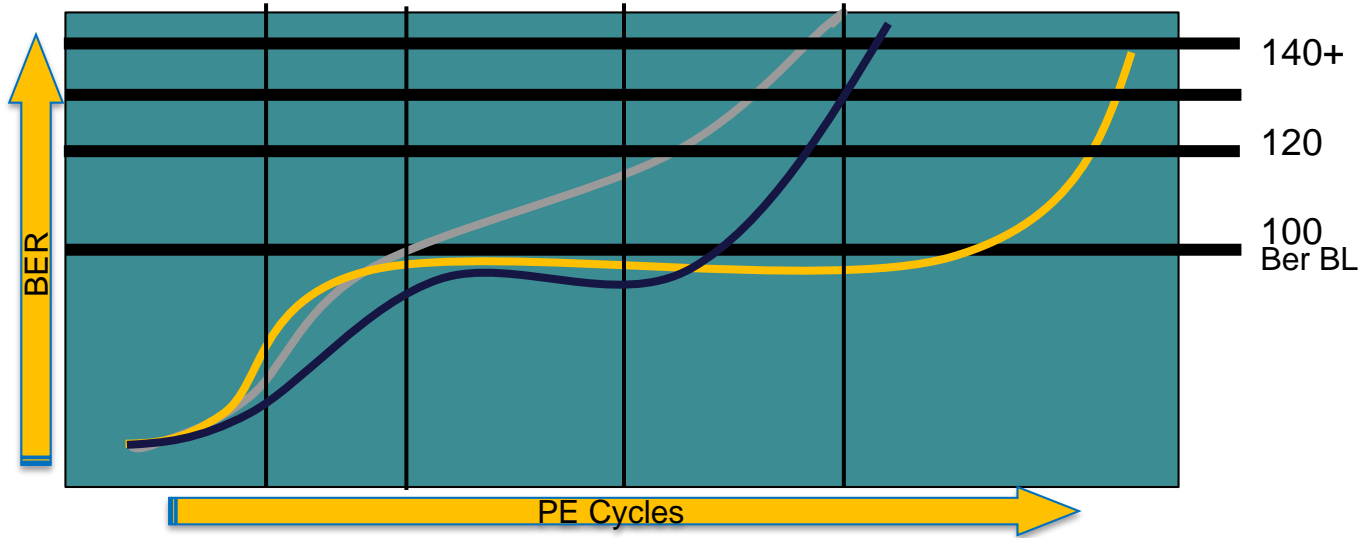
- Advantages
- Linear Read, Write performance
- No tail latency
- Low latency
- Predictable performance

Storage Technology Application Focus

- **NVME SSD**
  - Uses a new NAND management scheme that improves lifetime and
  - Improves Lifetime
  - Improves performance
- **Advanced Features can reduce system cost as well as Flash Array cost providing improved ROI.**

- **SSA (Solid State Array)**
  - Extended Lifetime of NAND Flash
  - Enables high bandwidth and better random access
  - Controls cost and improves ROI
- Companies Cannot develop an SOC for their volume they are stuck with commodity HW.
- An FPGA can enable a new level of performance and offering new capabilities for mixed memories

- **Direct Attach Storage/memory**
  - Latency reduction from all other suppliers
  - Extended lifetime
- New technology enablement to reduce storage latency and add in in Database memory capabilities for HPC
- Integrated single chip solutions along with new DRAM, MRAM memory arrays.

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Conclusion

- Memory Types and Capacity will challenge current sources to meet market changes.
- Application acceleration will need to be fine tuned to maximize performance.
- Dis aggration of data will have an impact on the storage architecture.
- FPGA's single chip solution can be cost effective in specialized applications and for times when memory is quickly advancing.
- NAND management system improves the performance and lifetime of NAND and there performance