3D XP: What the Hell?!!

Dave Eggleston

Making Sense of 3D XP

- WHY are you surprised?
- WHAT is it (really)?
- XP Array Limitations: The Litho Problem
- HOW will it be used?
- 3D XP strengths & weaknesses

Leading-Edge Technology Status

Source: S. DeBoer; Micron Analyst Day, Feb 2015

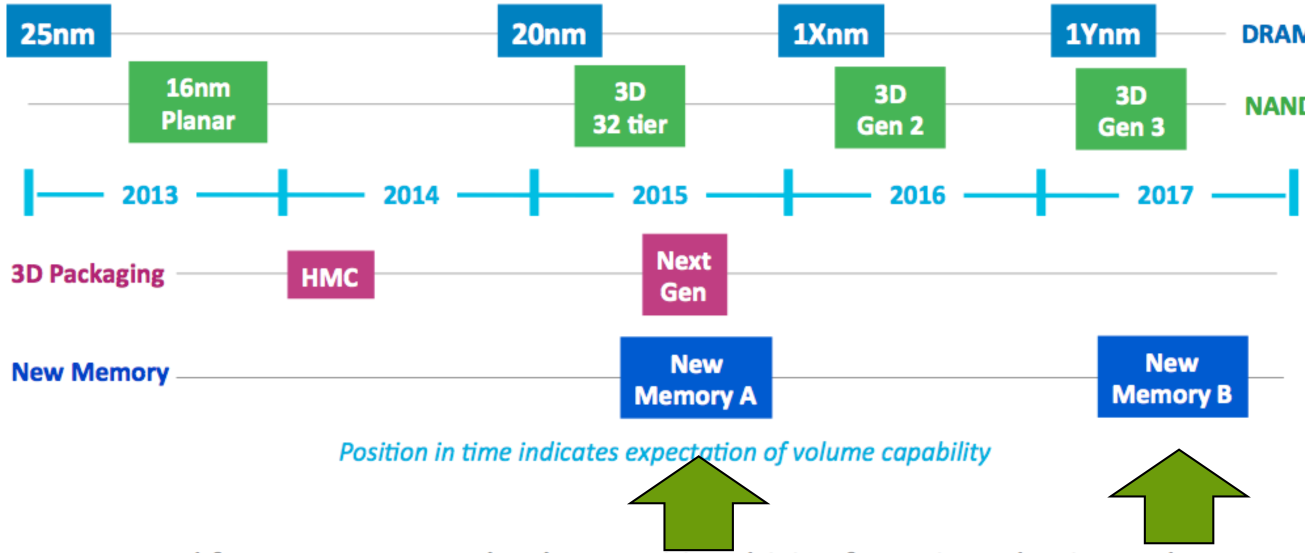
DRAM	*1Xnm DRAM*	• Continued strong progress for 20nm yield at Hiroshima and Inotera facilities • 1Xnm development underway in Hiroshima and 1Y/1Znm in Boise
NAND	*3D NAND*	• 16nm TLC NAND now ramping in Singapore • Micron 1st generation 3D NAND on track for production in Singapore mid 2015 • Second generation under development in Boise
Package Technology	*Hybrid Memory Cube*	• 3D NAND package technology continues to mature, currently manufacturing HMC generation 2 • R&D focus on HMC generation 3 enablement for even higher density and bandwidth
New Memory Technology	*Cross-point memory*	• Multiple paths under active development for storage class memory enablement • Targeting 2015 and 2017 for manufacturing introductions of next new memory technologies

Images are not to scale

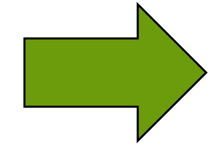
 ©2015 Micron Technology, Inc.

Innovation Roadmap

Source: S. DeBoer; Micron Analyst Day, Feb 2015



- Increased focus on DRAM technology position driving faster introduction cadence
- Enable volume 3D NAND manufacturing capability through 2015
- 3D NAND packaging technology enablement for multiple differentiated opportunities
- Establish disruptive new memory technology and position for ramp in 2016



Source: T. Pawlowski; Micron; ISSCC Memory Forum, Feb 2015

New Memory Technologies

- Replacement technologies are only one aspect
- Gap between memory and storage is another
- Need increased freedom to balance important system parameters

New Memory A is:

- DRAM-like
- Low latency
- Relatively high endurance
- Highly volatile(!)
- Relatively high cost

Switching Mechanisms

Source: M. Jurczak, imec, ISSCC 2015 Memory Forum

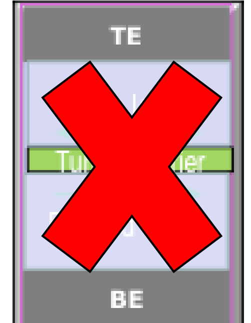
Filamentary ReRAM			Interfacial ReRAM	Bulk Transition		
Oxygen vacancy migration	Thermo-Chemical Fuse/ antifuse	Electro-Chemical ECM	Schottky or Tunnel Barrier	Phase Change PCM	Tunnel Magneto resistance	Electronic MIT (Mott)
TE / BE	TE / reduced / metal oxide / BE	Cation Source (Ag^+, Cu^+ or...) / Ag^+ / Cu^+ / METALIC FILAMENT / BE	TE / exchange layer / O vacancy,... / perovskite / BE	TE / Poly-crystaline / amorphous / BE	TE / Free layer / Tunnel barrier / Pinned layer / BE	TE / low-temp phase / high-temp phase / Monoclinic / Tetragonal / BE
BIPOLAR	UNIPOLAR	BIPOLAR	BIPOLAR	UNIPOLAR	BIPOLAR	UNIPOLAR
TMO: HfO2, TaO2	TMO: NiO2	CBRAM: Cu, Ag based	Memristor VMCO, PCMO, TiO2	Chalcogenide alloys: GST	STT RAM (CoFeB, MgO)	VO2, NbO2

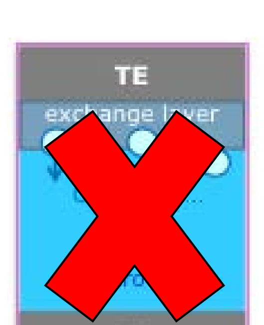
What is 3D XP?

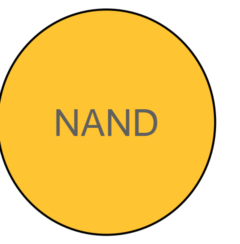
Source: Intuitive Cognition Consulting estimates

ST-MRAM | PCMS | ReRAM

DRAM







3D XP is *NOT* ST-MRAM because:

- Can't build ST-MRAM in a XP array (1T-1R)
- Can't achieve 128Gb with ST-MRAM ($30F^2$)
- ST-MRAM more expensive than DRAM

Fast — Latency — Slow

Long — Endurance — Short

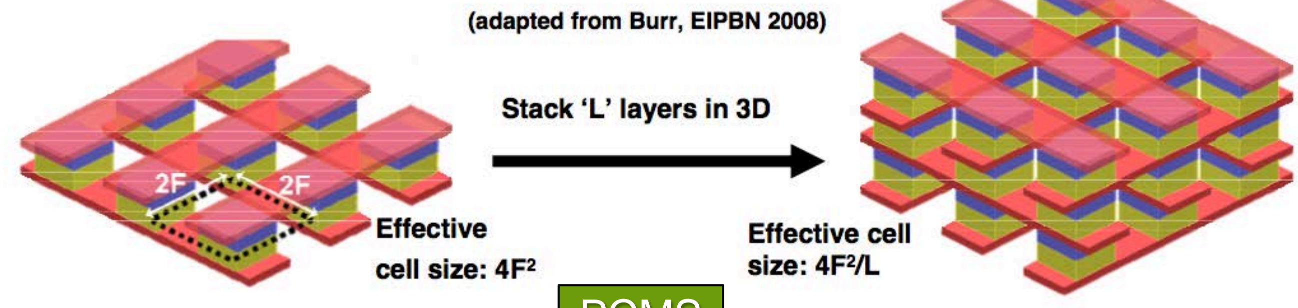
Big/$$$$ — Cell Size/Cost — Small/$

3D XP is *probably NOT* ReRAM because:

- ReRAM Latency is too slow for application
- ReRAM endurance may be too short for the application
- ReRAM is much more likely New Memory B (Cost focused)

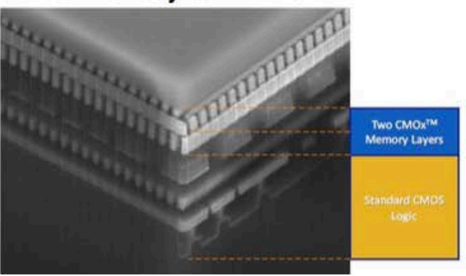
Crosspoint resistive memory

Source: R. Shenoy, IBM, IMW May 2013



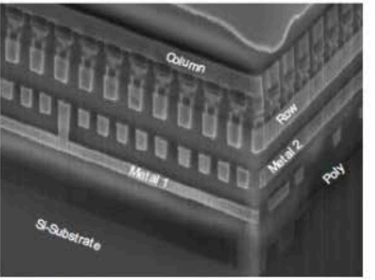
PCMS

Ref: D. Eggleston,
Flash Memory Summit 2011



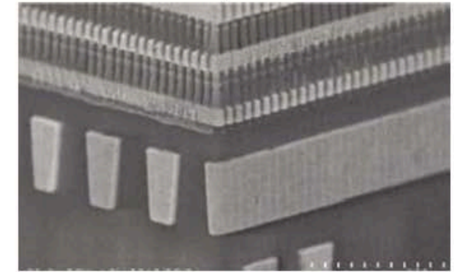
Unity Semiconductor 2 layer Conductive Metal Oxide RRAM

Ref: D. Kau, IEDM 2009



Intel/Numonyx 64Mb PCM+OTS selector

Ref: T-Y. Liu, ISSCC 2013

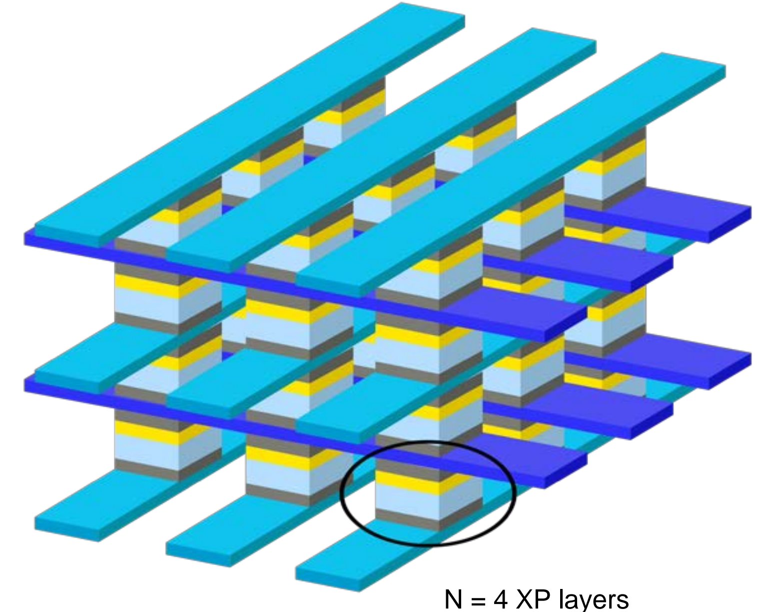


Sandisk/Toshiba 32Gb 2 layer MeOx ReRAM crosspoint in 24nm technology

3D multilayer stacked crosspoint arrays → path to low cost memory

WRONG!

XP Arrays: The Litho Problem



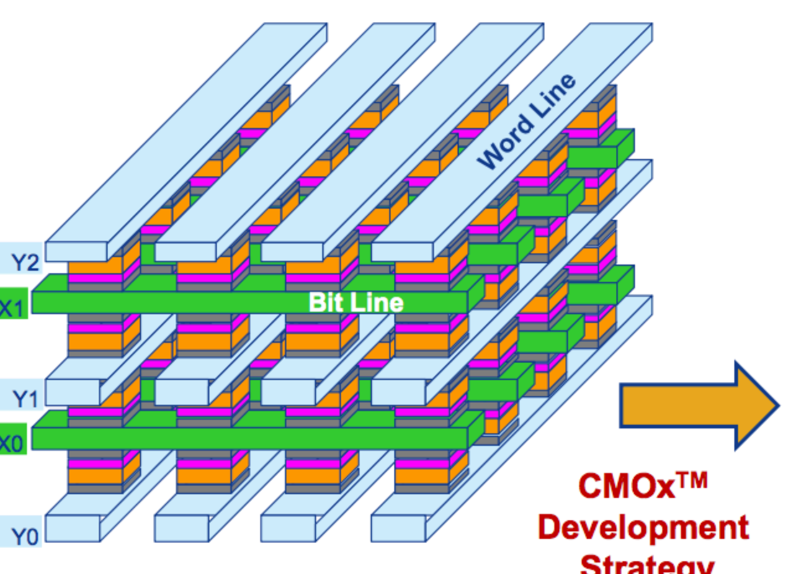
N = 4 XP layers
N+1 = 5 masking steps

Cell size of $4F^2$
Effective cell size $1F^2$

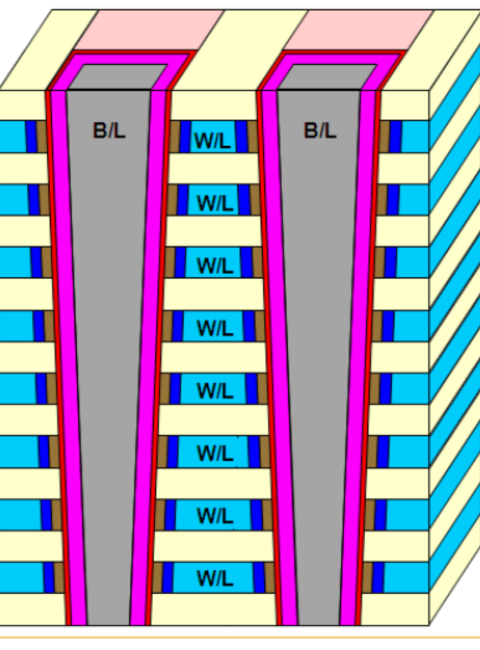
- ❑ XP array with shared layers requires multiple masking steps:
  - N+1 masking steps to form WL/BL
  - i.e. 4 XP layers requires a minimum of 5 masking steps
- ❑ XP cell size $4F^2$ determined by WL/BL lithography:
  - To achieve sub 20nm F requires triple or quad critical layer patterning
  - i.e. 4 XP layers ➔5 critical masking steps➔ x4 quad patterning ➔ 20 times through the stepper at sub 20nm!!!
- ❑ **XP arrays will never be the lowest cost memory solution!**

Source: C. Chevallier, Unity, CEATEC 2011

Planar CMOx™



Vertical CMOx™



CMOx™ Development Strategy (NO EUV Required)

Current Major Costs of Planar CMOx™:
- Multiple immersion patterning or EUV lithography
- Fine line interconnect very challenging

Vertical CMOx™ (VXPA):
- Extension of vertical NAND
- Low cost lithography
- Fine line interconnect not required
- Earlier, Cost effective option

Reuse of the 3D NAND architecture and processing is the way forward for lowest cost RRAM.

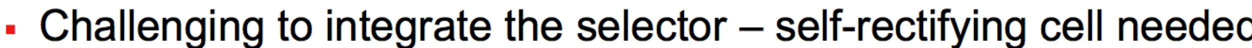
© Unity Semiconductor Corporation

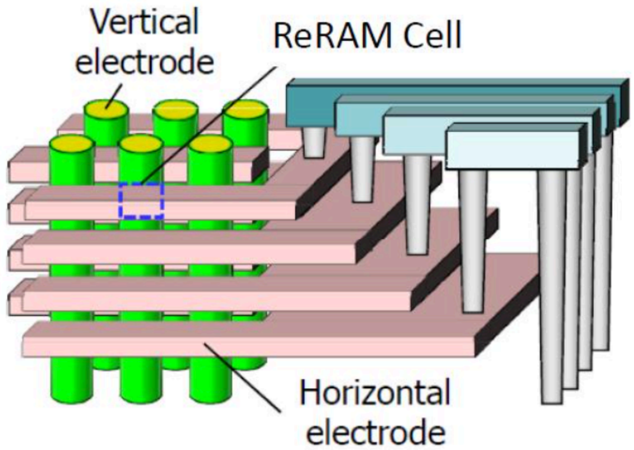
Vertical ReRAM (VRRAM)

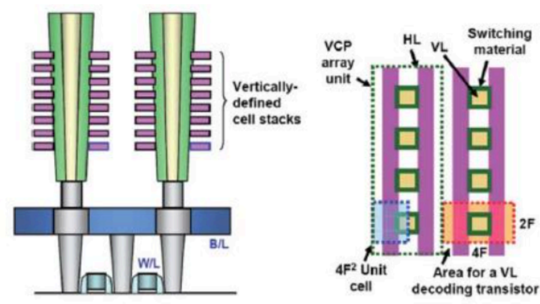
Source: T. Liu, Sandisk, IMW May 2013

BUT, to do so requires a built-in selection capability. This is DIFFICULT!
See you in 2021!

- No. of critical masks is not increasing with added memory layers
  - Multiple layers are formed at the same time







Reference:
S. Kim, LETI Memory Workshop 2012
I. G. Baek et al., IEDM 2011
H. S. Yoon et al., VLSI 2009

But WHAT 3D XP is doesn't really matter…

…HOW will 3D XP be used?

How 3D XP will be used

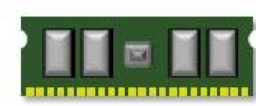
Source: The Platform, “Intel Lets Slip Broadwell, Skylake Xeon Chip Specs”, May 2015

Purley: Biggest Platform Advancement Since Nehalem

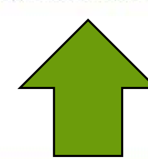
PERFORMANCE FOR RANGE OF WORKLOADS

- Better performance/Watt
- 1.5X memory bandwidth
- AVX-512 new instructions

ALL NEW MEMORY ARCHITECTURE



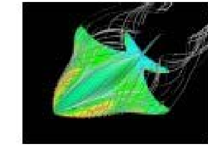
- Up To 4X capacity & lower cost than DRAM
- 500X faster than NAND
- Persistent data



INTEGRATED NETWORK / FABRIC

- 1/10G Ethernet
- 100G OmniPath™

OPTIONAL INTEGRATED ACCELERATORS



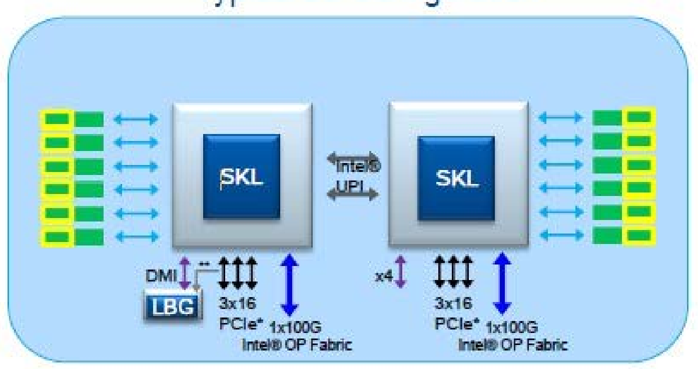
- QuickAssist™ encryption and compression offloads
- Skylake + FPGA
- Cannonlake graphics & media transcode

7

How 3D XP will be used

2S Purley Platform Configuration Example

Typical 2S Configuration



DDR4 DIMMs
DDR4/Apache Pass
Optional PCIe* uplink connection for Intel® QuickAssist Technology and Intel® Ethernet
Example DIMM population shown; please look up Apache Pass customer collateral for specific rules on DDR4/Apache Pass DIMM populations

"Apache Pass" DDR4 DIMMs supported in Purley.

Platform Ingredient Options

Fabric: Storm Lake Integrated, Storm Lake PCIe* card

Storage: SATA: Downieville, SATA: Youngsville, PCIe*: Coldstream, PCIe* Cliffdale

Software: Analytics, Efficiency, Performance, Secure Access, Tools

Networking: Lewisburg as 4x10GbE Integrated Network Solution with PHY, Fortville 4x10/2x40GbE (Controller), Sageville 2x10GBASE-T (Controller), Springville (1x1GBASE-T), Powerville (4x1GBASE-T)
Core Ingredients: Coppervale 10GBASE-T, Jacksonville GbE PHY

Accelerators: Intel® QuickAssist Accelerator Technology with Compression and Encryption, Lewisburg can also be used as PCIe* add-in card in end point mode

Intel® Xeon Phi™ Product Family: Knights Corner/Landing Coprocessors and Processors

FW/Bios: Manageability, Node Manager, Intel® RSTe, ME11, Intel® Trusted Execution Technology and Intel® Platform Protection Technology with Boot Guard

Source: The Platform, "Intel Lets Slip Broadwell, Skylake Xeon Chip Specs", May 2015

Intel Near/Far Memory Hierarchy

MEMORY/STORAGE HIERARCHY 140

CACHE 150
- PROCESSOR CACHE 150A — LEVELS 0-N
- NEAR MEMORY (NM) AS CACHE FOR FM (MSC) 150B (E.G., CACHES 106-109 IN FIG. 1)

NEAR MEM MODE X (E.G., SCRATCHPAD) 192

NEAR MEM MODE Y (E.G., WRITE BUFFER) 193

SYS. ADDR. SPACE B 191

CORE(S) 101-104

CACHE(S) (E.G., SRAM) 101A-105

I/O SUBSYSTEM 115

SYS. ADDR. SPACE A 190

BIOS FLASH MEMORY 170

FIRMWARE MEMORY 153

NEAR MEMORY (E.G., DRAM) 144

NEAR MEMORY CACHE (MSC) CONTROL 124

SYSTEM MEMORY 151
- NEAR MEMORY AS SYSTEM MEMORY 151A
- FAR MEMORY (FM) 151B (WHEN NEAR MEMORY IS PRESENT)

NVRAM SYSTEM MEMORY 174

NVRAM MASS STORAGE 152A

BIOS NVRAM 172

TPM NVRAM 173

NVRAM (E.G., PCM) 142

MASS STORAGE 152

FLASH/ MAGNETIC/ OPTICAL MASS STORAGE 152B

FIG. 2

Intel projects use of PCM memory as "Far memory"; uses DRAM as a "Near memory cache". Consolidation of system memory, storage BIOS and TPM in PCM.

Source: Intel US patent, R. Ramanujan et al, "Dynamic partial power down of memory-side cache in a 2-level memory hierarchy" US 20140304475 A1

Intel PCM-Based DIMMs

Transactional protocol over DDR bus handles non-deterministic behavior of PCM.

PCM DIMMs and DRAM DIMMs both reside on DDR Transactional bus.

Fig. 4G

Source: Intel US patent, R. Ramanujan et al, "Dynamic partial power down of memory-side cache in a 2-level memory hierarchy" US 20140304475 A1

Intel PCM-Based DIMM Controller

PCM DIMM 519

PCM Controller
521

Wear Mgmt
555

PDT
565

Far Memory
Control I/F
548

SPA->
PCM
Map 556

Scheduler
557

PCM
Protocol
Engine
558

PCM
I/F

Data
Buffers
561

ECC
562

Flush
Support
560

Persistent
Write Buffer
559

Address Indirection
563

PCM Device 530a

PCM Device 530b

PCM Device 530c

PCM Device 530d

PCM Device 530e

PCM Device 530f

PCM Device 530g

PCM Device 530h

PCM Device 530i

Writes are persistently buffered in the PCM controller to mask write latency.

FIG. 5E

Source: Intel US patent, R. Ramanujan et al, “Dynamic partial power down of memory-side cache in a 2-level memory hierarchy” US 20140304475 A1

Speculation on Intel usage of 3D XP

Source: Intuitive Cognition Consulting estimates

- Server memory DIMMs:
  - In-memory compute, Real time analytics applications
  - Coincide with Purley platform launch in 2017
  - DDR4 bus with transactional protocol (non-JEDEC)
  - Read is PCM native latency (50-200ns)
  - Write is buffered in PCM controller (latency hidden)
  - 100's of GBs per DIMM (3x-4x DRAM capacity/DIMM)
  - Trouble meeting 12W power window (PCM energy)

Strengths/Weaknesses 3D XP

Source: Intuitive Cognition Consulting estimates

- Strengths
  - Brand new memory type brings new capabilities
  - Semi-Persistent memory arrives!
  - Server memory target competes with DRAM cost
  - Read/write performance near full DRAM speed
  - Full system approach
- Weaknesses
  - 3D XP cost will be high:
    - DRAM $8/GB, 3D XP $4/GB, 3D NAND $0.2/GB
  - Sole sourced from Intel/Micron
  - Requires major hardware and software changes
  - >12W Power requires server thermal re-design
  - Non-JEDEC standardized DDR4 transactional interface

Making Sense of 3D XP

- WHY are you surprised?
- WHAT is it (really)?
- XP Array Limitations: The Litho Problem
- HOW will it be used?
- 3D XP strengths & weaknesses