Scalable Flash Architectures Meet "Instant On"

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Explosion of More Intelligent and Connected Devices

2003

6.3B people

Many devices connected to the Internet

2008

6.7B people

More connected devices than people on earth

2020

7.7B people

50 – 70 billion connected devices; ~7x the number of people on earth

In 2013, there were 23M connected cars.
In 2015, 20% of vehicles sold will be connected.
By 2020, there will be 152M connected cars sold globally. Source: IHS

Explosion of Connected Autos

Cypress + Spansion = No. 3 in Automotive Memory & MCUs

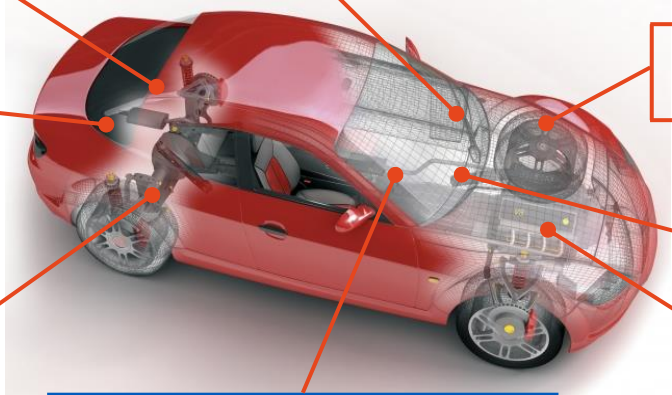
Flash | MCU | Analog | SRAM | PSoC

Chassis
- Power Steering (M)
- Antilock Brake (M)
- Steering Sensor (M)
- Stability Control (M)

Safety/ADAS
- TPMS (M)
- Air bag (M)
- Telematics (F M S P)
- Rearview Camera (F S)
- Multi-Camera (F S)

Body Electronics
- Body Control (F M A)
- Gateway Control (M A)
- Wiper (M A)
- Window (M A)
- Lights (M)
- Mirror (M)
- Seats (M)
- Doors (M P)

Driver Information
- Head-up Display (S)
- Instrument Cluster (F M A S)



Infotainment
- GPS and Navigation (P S)
- Satellite Radio (F M A S)
- Blue-ray/DVD
- Audio Systems (F M S P)
- Central Information Display (F M A P)
- Rear-Seat Entertainment (F M S)

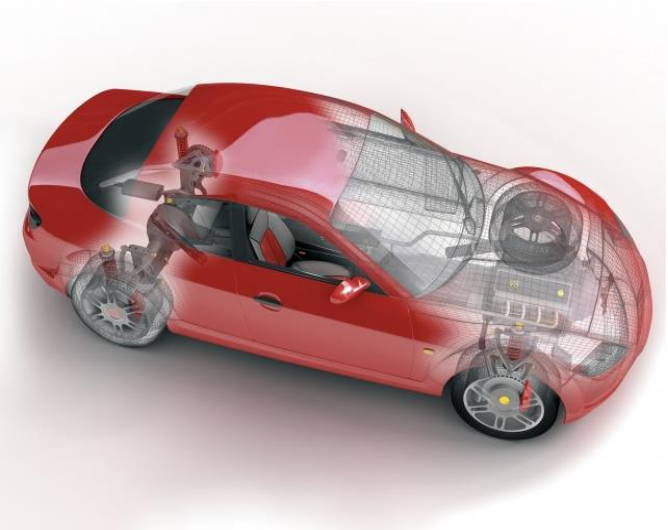
Voice Recognition (F)

Touch and Character Recognition (F M P)

Climate Control / HVAC (F M A P)

Power train
- Fuel Injection (M)
- Motor Control Unit (HV/EV) (M F S)
- Battery Charging Control (HV/EV) (M)
- DCDC Control (HV/EV) (M)
- Alternator (M)

High Performance Automotive Requirements



Auto-Cluster

Infotainment

TFT replacing mechanical
Instant on

Traditional architecture insufficient
Fast boot
Graphics recall

Larger screen and higher resolution
Complex graphics
Motion graphics
More instant on functionality

Flash NOR Flash for
Boot, Code, and Graphics

Cypress HyperBus™: A Better Solution

HyperBus™ Interface

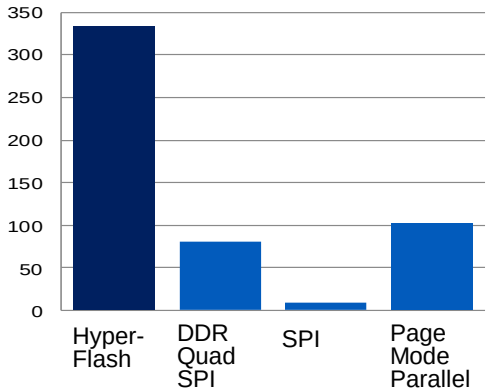
A high-bandwidth, 12-signal interface that transfers information over 8 I/O signals at double data rate (DDR), delivering up to 333 MBps

HyperFlash™ NOR Flash Memory combines the industry's **highest Read Bandwidth...**

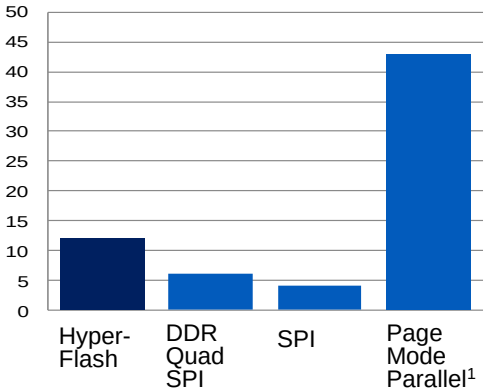
With one of the **lowest-pin-counts available**...

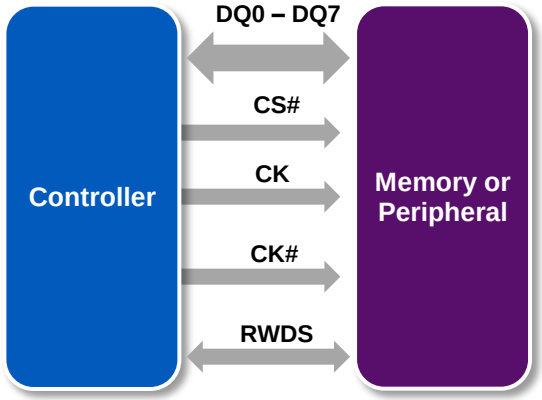
HyperBus™ Interface (12 pins)

Read Bandwidth (MBps)



Pins for Data Transfer (# of Pins)





HyperBus™ and HyperFlash™ Memory

Industry's fastest NOR Flash Memory for the highest-performance systems

Problems Designers Face	HyperFlash™ Solves These By:
The highest-performance systems for fast boot with graphics display	A DDR mode with up to 166-MHz with 333-MBps Read Bandwidth
Low-pin-count interfaces to reduce system cost	A standard 24-ball package sharing a common footprint with Quad SPI and Dual Quad SPI simplifies board layout
They must have high system reliability	On-chip ECC to provide a FIT rate <0.1 FIT per device
High temperature ranges	An extended operating temperature range of -40ºC to +125ºC

To enable demanding high-performance systems

Example:
Automotive Instrument Cluster

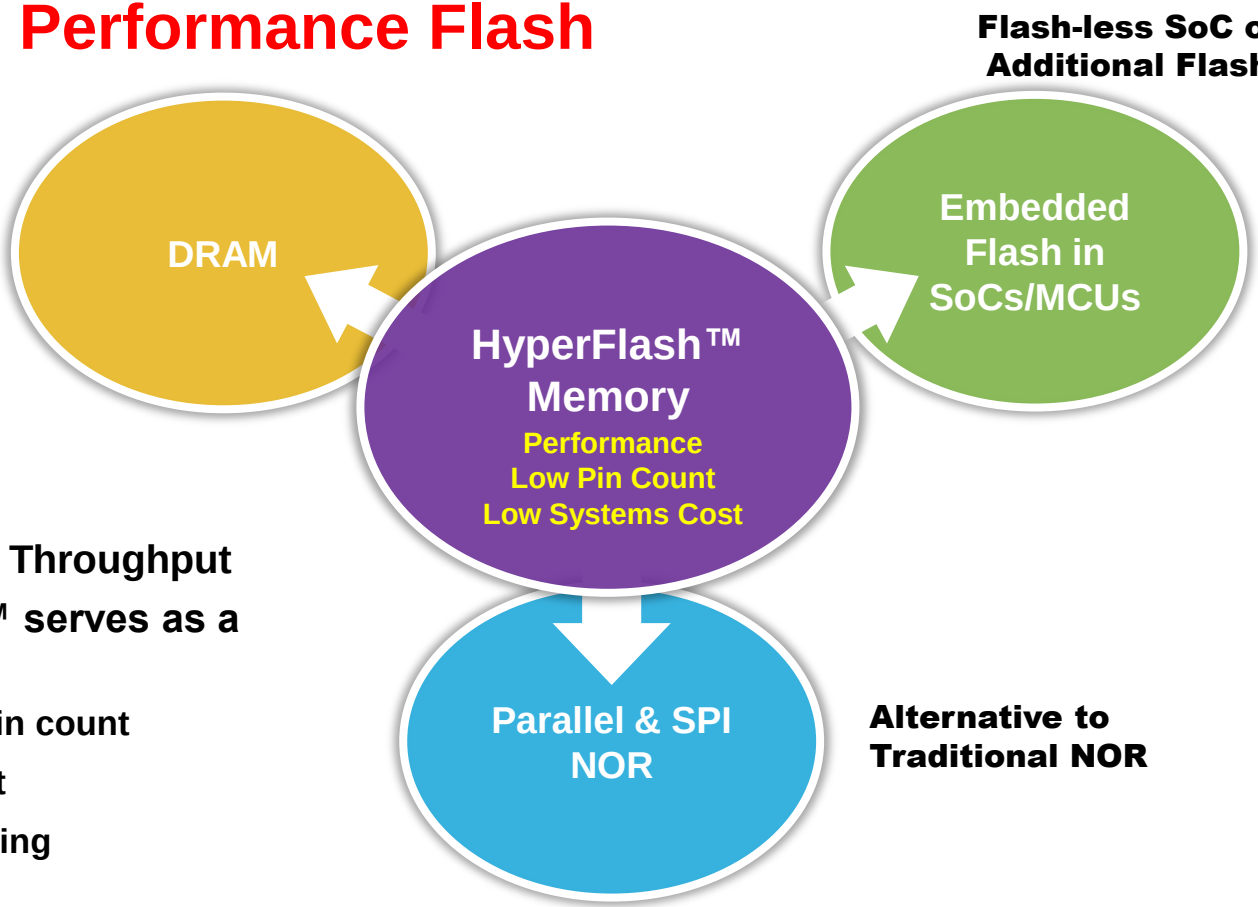
HyperFlash™ vs. Traditional Flash

Feature	S26KS Family	2 x S25FS Family	S25FS Family	SPI
				Other
Interface	HyperBus	2 x Quad SPI	Quad SPI	Quad SPI
I/O Pin Count	8	8	4	4
Clock Rate (DDR)	166 MHz	80 MHz	80 MHz	54 -66MHz
Read DDR Bandwidth (max)	333 MBps	160 MBps	80 MBps[1]	54 - 66 MBps[1]
Program Time (512B)[2]	0.475 ms	0.475 ms	0.475 ms	1.0 ms[3]
Sector Erase Time (256KB)[2]	930 ms	930 ms	930 ms	1400 ms[4]
Chip Erase Time[2]	110 s	120 s	120 s	240 s
Temperature Range	-40ºC to +125ºC	-40ºC to +105ºC	-40ºC to +105ºC	-40ºC to +85ºC
	Best	**Better**	**Good**	**Ok**

Faster Boot, Bigger Display, Higher Resolution, Fancier Graphics, Smoother Motion

[1] Calculated using DDR clock rate
[2] Conditions: 25ºC and V_{CC} 3.0 V, 100k minimum endurance
[3] Parts do not support 512B Programming. Program time is calculated using two 256B Program operations.
[4] Parts do not support 256KB Sector Erase. Erase time is calculated using four 64KB Sector Erase operations.

Other Implications for High Performance Flash



- Fast Initial Access
- High Sustained Read Throughput
- Cypress HyperRAM™ serves as a companion RAM
  - Reduced controller pin count
  - Simplified PCB layout
  - Space-saving packaging