Fully Integrated SSD-NAND Characterization Flow

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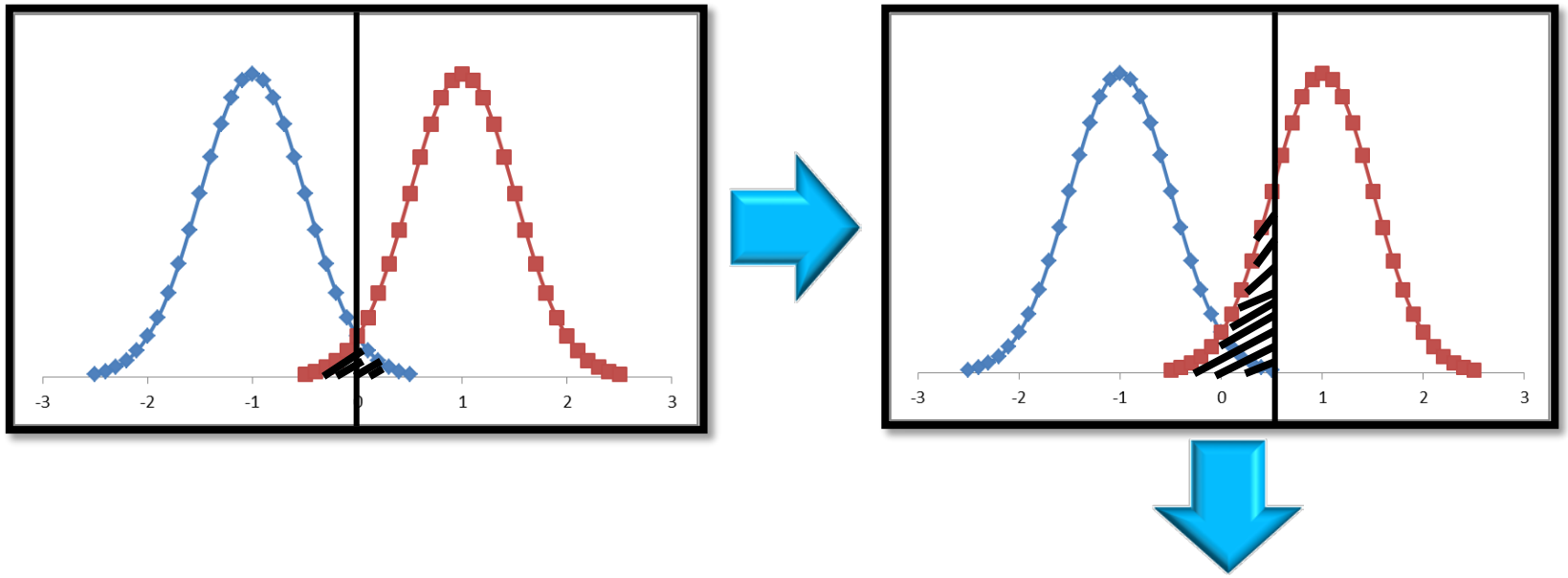
NAND reliability & read oversampling

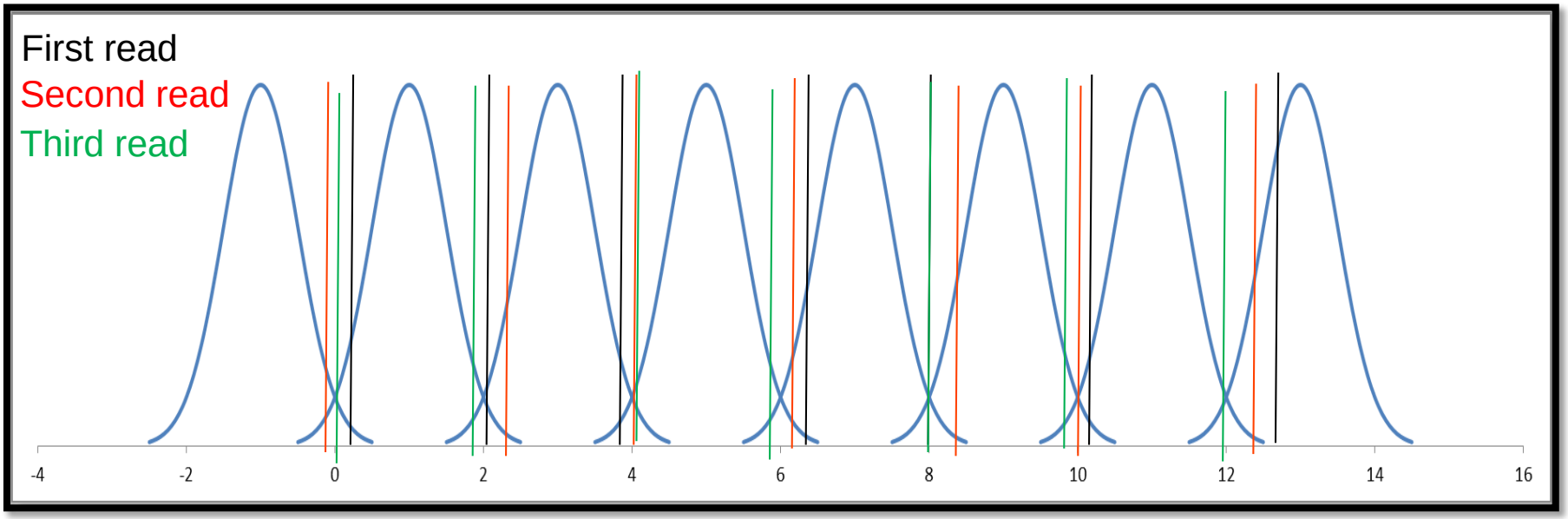
- NAND process technology shrink and multi-bit per cell storage reduce $/GB but increase NAND raw BER
- Vt-shift (Read Retry) techniques and LDPC ECC are well known ways to limit BER growth
- Vt-shift and soft LDPC require read oversampling and they may impact SSD's QoS
- NAND silicon characterization data can be coupled to an SSD simulator to predict QoS

Vt–shift Technique



- During life, Vt distributions move
- Vt-shift is used to re-center the read reference voltage

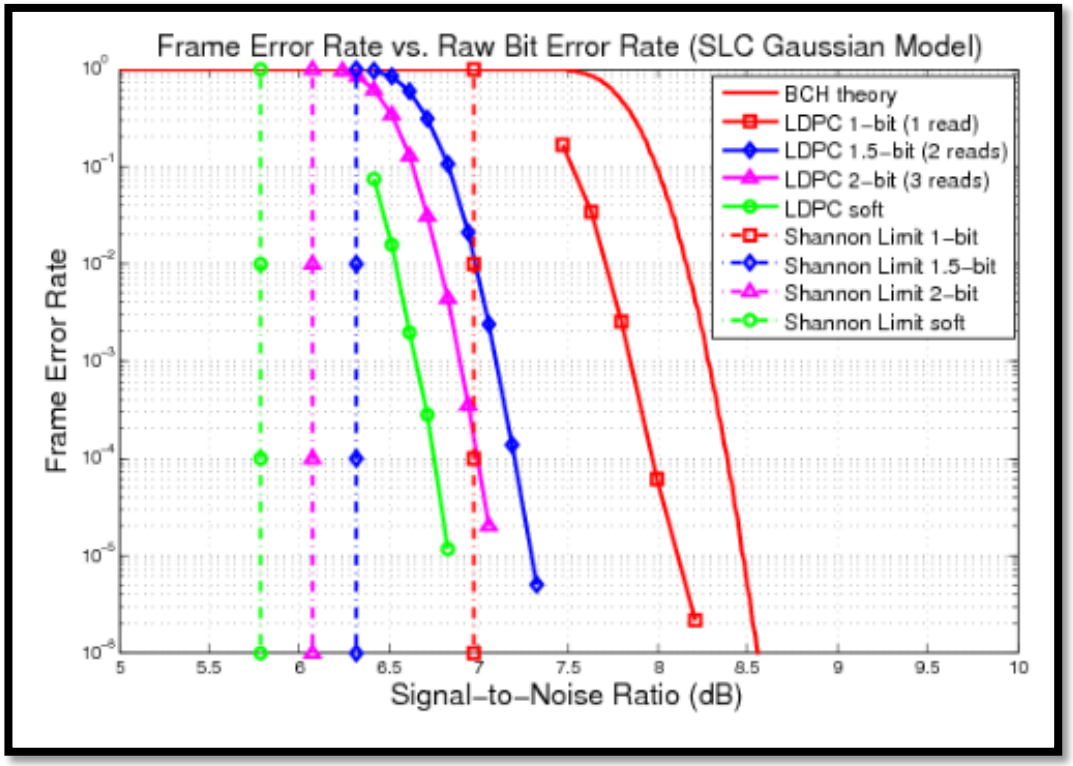
Vt-shift combinations



- Number of Vt-shift combinations is huge
- Finding the right combination can take a long long time -> QoS degradation

Soft LDPC

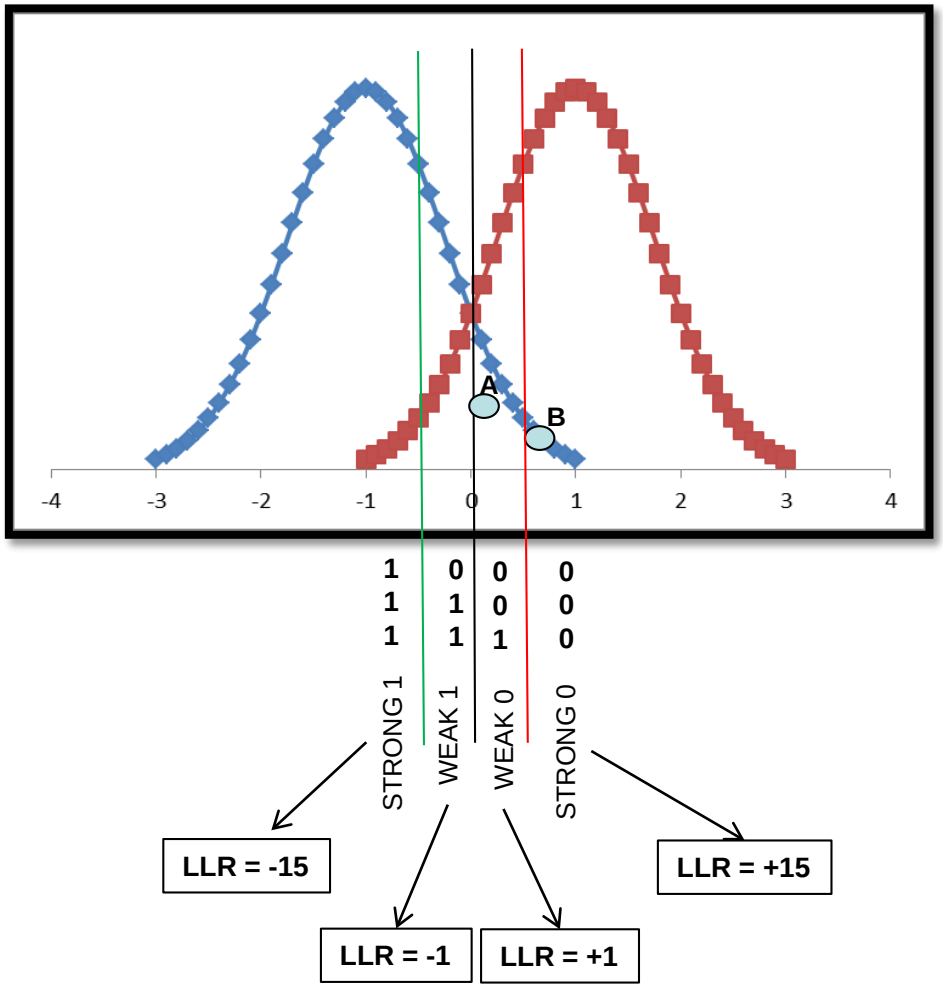
- Soft information is used to move the Shannon limit of a specific channel



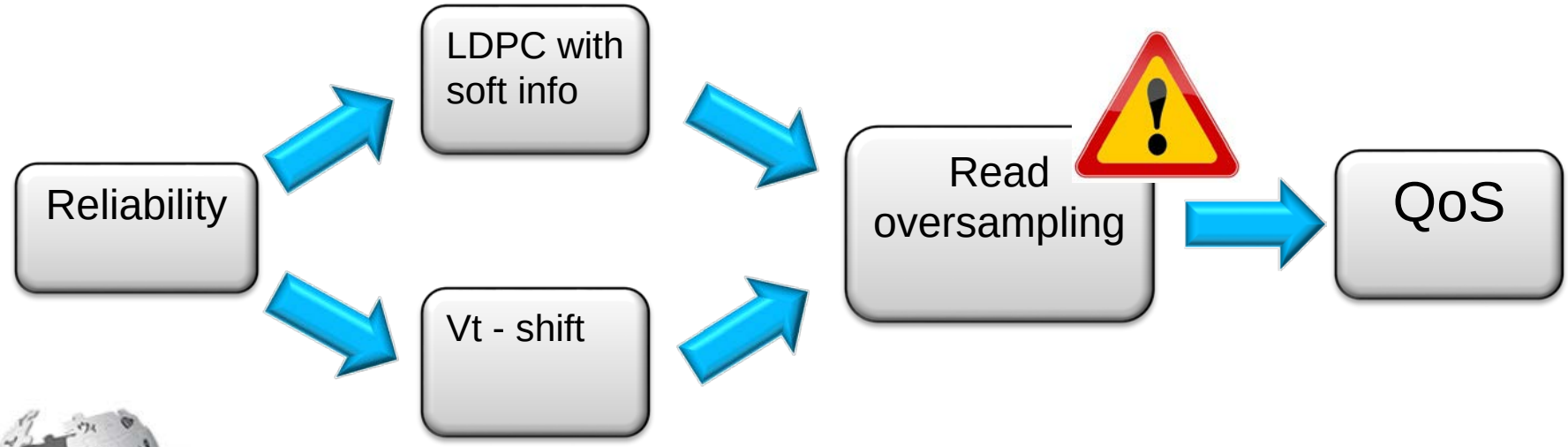
[1] Wang Jiadong et al., "Enhanced Precision through multiple reads for LDPC Decoding in Flash Memories" in *IEEE Journal on Selected Areas in Communications,* May 2014

Soft Reads

- Point A is more likely to be in error than point B
- Soft LDPC uses LLRs to measure reliability
- The overlap region between Vt distributions is scanned by using additional reads



QoS

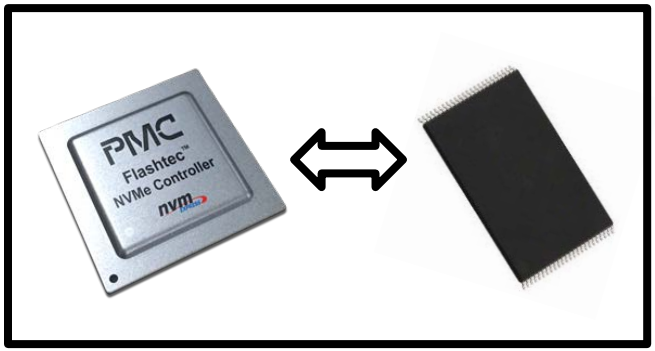


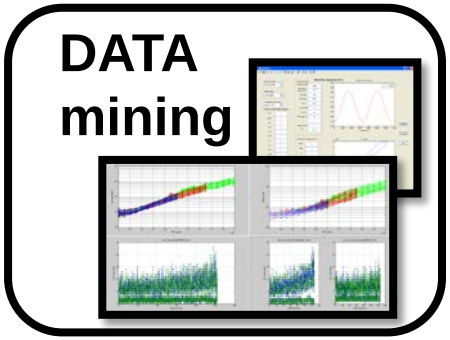
WIKIPEDIA
The Free Encyclopedia

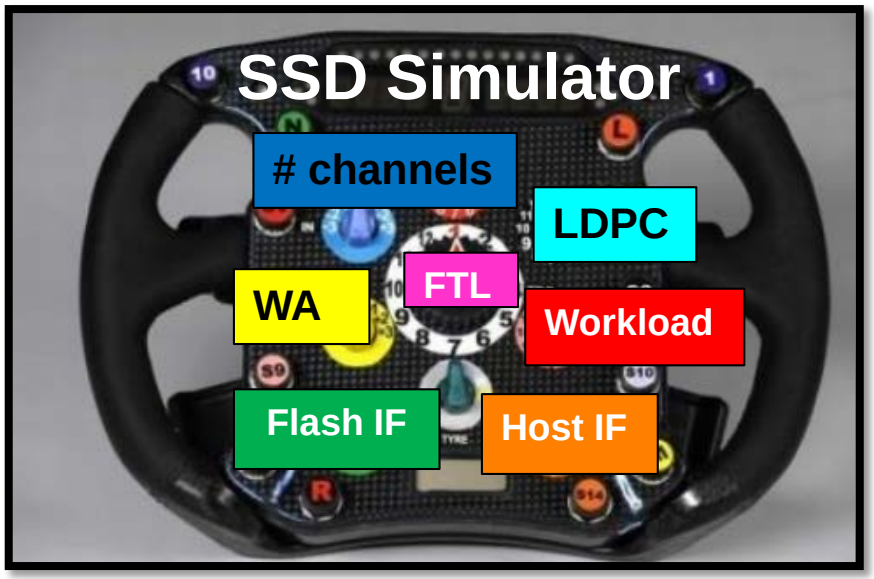
Quality of service (**QoS**) is the overall performance of a telephony or computer network, particularly the performance seen by the users of the network.

To quantitatively measure quality of service, several related aspects of the network service are often considered, such as error rates, bandwidth, throughput, transmission delay, availability, jitter, etc.

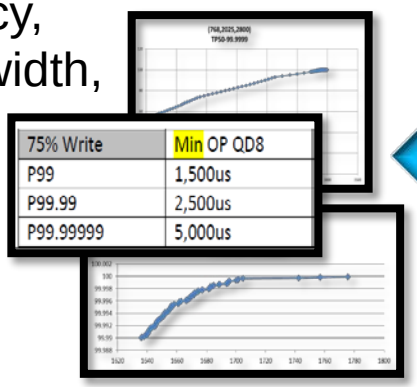
Fully Integrated SSD-NAND Characterization Flow







Latency,
Bandwidth,
IOPS

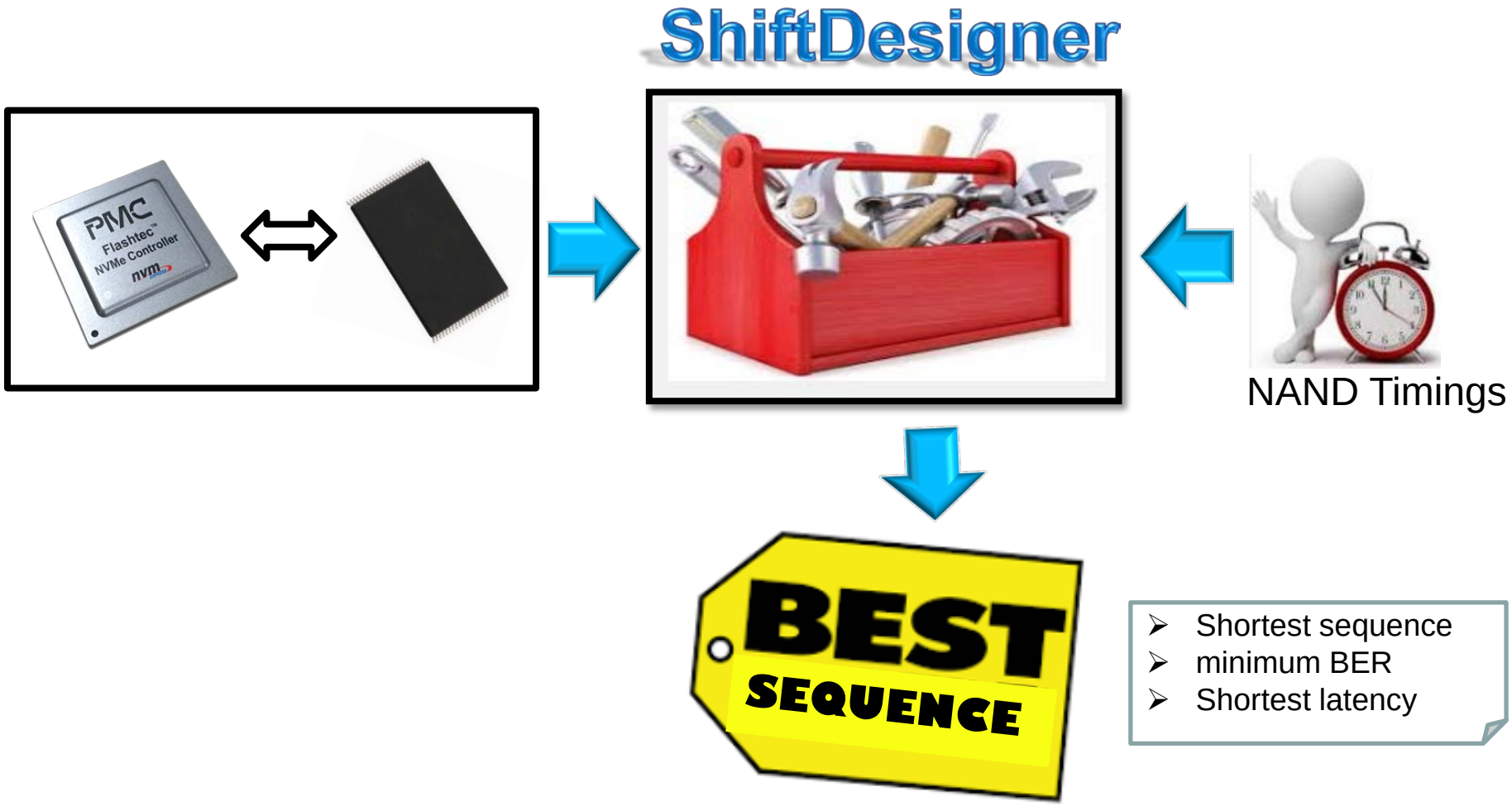


75% Write	Min OP QD8
P99	1,500us
P99.99	2,500us
P99.99999	5,000us

Read Oversampling: Mitigation Techniques

- “ShiftDesigner” is a custom developed tool that minimizes NAND BER by applying the shortest sequence of Vt-shifts
- LDPC: an FPGA network is used to identify the best trade-off between hard decoding and 1-bit or 2-bit soft decoding

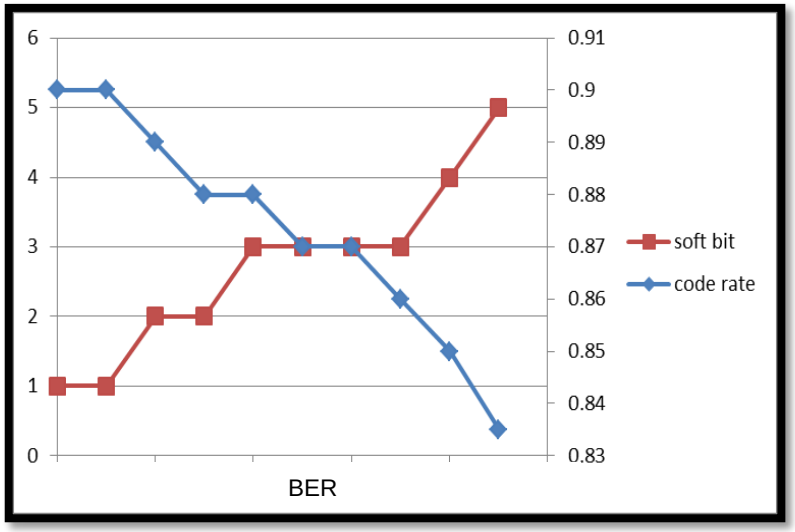
ShiftDesigner

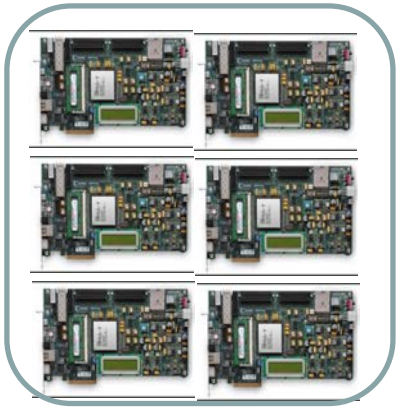


- Shortest sequence
- minimum BER
- Shortest latency

LDPC: Hard vs. Soft

- Code Rate and the number of soft bits can be used to reduce FER
- Lower Code Rate means cheaper
- Higher number of soft bits translates into longer read latency
- LDPC HW/SW co-simulation can find the best compromise between latency and cost

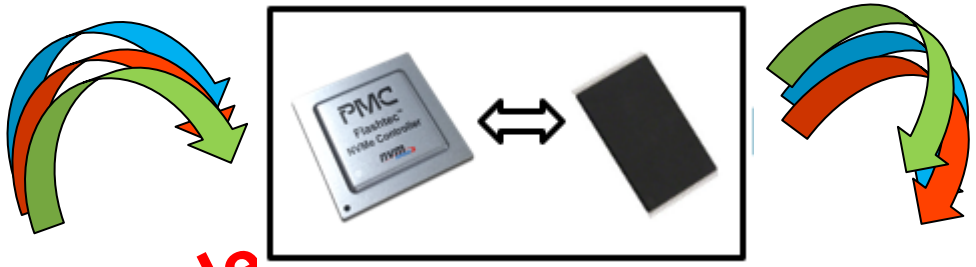




R. Micheloni, P. Graumann, “Hardware/Software co-simulation for Error Floor detection in LDPC” - *Flash Memory Summit* 2014

SSD-NAND: lifetime simulations

Change parameters & re-loop until QoS targets are met



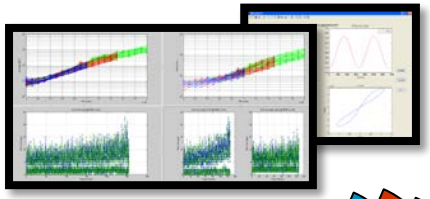
Latency, Bandwidth, IOPS

unacceptable

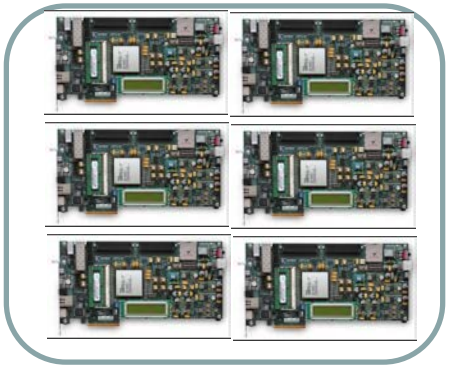
500 P/E

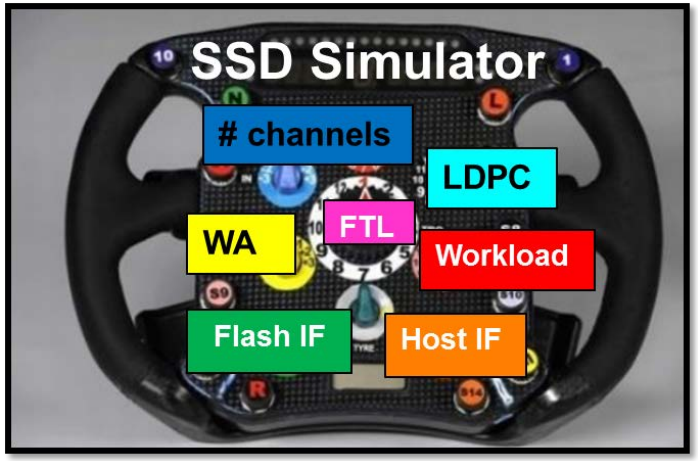
6h Retention

Data Mining



LDPC HW Co-Sim





Live Demo

- Live Demo of the “Fully Integrated SSD-NAND Characterization Flow” can be seen at PMC Booth # 213
- The simulation engine of this demo is SSDExplorer
  - ssdexplorer.azurewebsites.net
- More details about this tool in Forum F-21, “SSDExplorer: a virtual platform for SSD simulation”

Conclusions

- Vt-shift and soft information LDPC can be used to decrease NAND raw BER
- Both techniques impact QoS, because of the additional reads
- NAND silicon characterization can be coupled to an SSD simulator to predict and optimize SSD's QoS
- "ShiftDesigner" is a custom developed tool that minimizes NAND BER by applying the shortest sequence of Vt-shifts
- LDPC HW/SW co-simulations are used to find the best compromise between Hard and Soft decoding

Thank You!

See us in booth # 213

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