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Logic based ReRAM assisted by self-adaptive circuit for embedded applications

Prof. Yinyin Lin

ASIC and System Key Lab,

Fudan University, Shanghai, 201203, China

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Outline

- Motivation
- Self-adaptive FS-DSUR Write Algorithm
- Self-Adaptive Read Mode(SARM)
- Demonstration of emRRAM in SOC chip for Information Security
- Conclusions
- Acknowlegements

Requirements of emNVM

- Scalability:
  - Current embedded NVM solutions are difficult to scale down with logic because of high voltage process: EEPROM/emFlash
- Cost:
  - Easy to integrate with process simplicity
- Reliability:
  - Retention and endurance
  - Ensure read and write function under PVTA variation

Advantages of emRRAM

- Simple cell structure on back-end of line (BEOL)
- High scalability
- Good logic process compatibility
- No high voltage

Some Published RRAM Test Chips

	Media	Process	Cell	Cap.	Key Points
Unity (ISSCC2010)	CMO_X CB	0.13um	cross- point	64Mb	R/W circuits for cross-point array
Panasonic (ISSCC2012)	TaO_X	0.18um	cross-point	8Mb	novel array architecture for multi-layer cross-point array with bidirectional selection diode
Qimonda (JSSC2007)	GeSe CB	90nm	1T1R	2Mb	R/W circuits for high speed
Sony (ISSCC2011)	CuTe CB	0.18um	1T1R	4Mb	R/W circuits for high bandwith
ITRI (ISSCC2011)	HfO_2	0.18um	1T1R	4Mb	parallel-series reference-cell for high read yield; dynamic V_{BL} for faster read
NTHU (ISSCC2012)	HfO_2	65nm	1T1R	8Mb	body-drain-driven Current SA to keep enough read margin at low VDD

Less statistical testing and yield results are addressed.

Some Published RRAM Test Chips

	Media	Process	Cell	Cap.	Key Points
Sandisk & Toshiba (ISSCC2013)	MeO	24nm	1D1R	32Gb	read/write circuit techqiques for high density
Panasonic (ISSCC2013)	Ta2O5/ TaOx	0.18μm	1T1R	512Kb	forming/write circuit techniques for high endurance
NTHU & ITRI (VLSI2013)	HfO	0.18μm /65nm	1(parasitic BJT)1R	1Mb/2Mb	temperature-aware BL bias in current sensing for fast read
Micron & Sony(ISSCC2014)	CuTe	27nm	1T1R	16Gb	High-speed interface, sense amplifier and column redundancy
NTHU & TSMC (ISSCC2014)		28nm	1T1R	1Mb	Low-VDD read and self-boost write-termination

Less statistical testing and yield results are addressed.

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Motivation of this work

- Aiming at the key issues for emRRAM pratical appliations, develop circuit assisted optimization methodology
  - Read/write yield under PVTA
  - Retention/endurance yield
  - Power consumption

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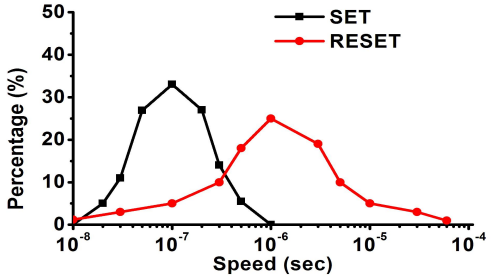
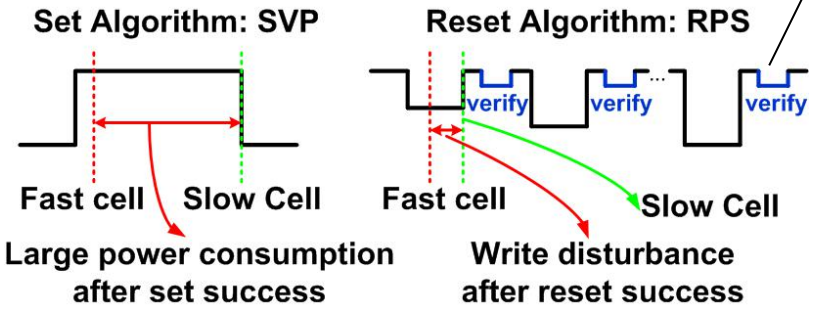
Issues of fixed pulse



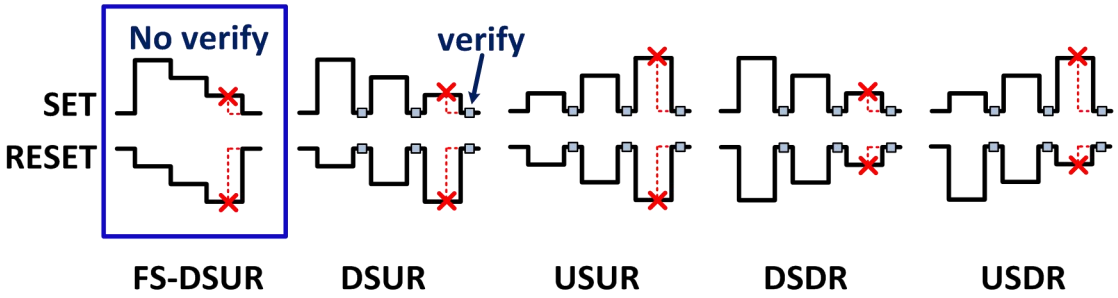
Wide Set speed: 10ns-100ns
Wide Reset speed: 10ns- 60 μ s

Verify: additional time and energy consumption



SVP: single voltage pulse
RPS: ramped puslse series

FS-DSUR Algorithm

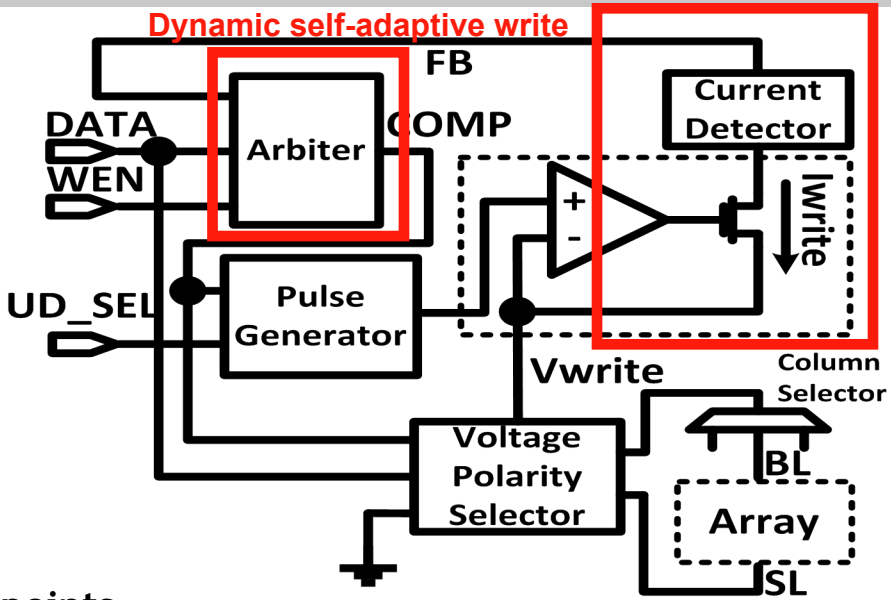


Proposed	FS- DSUR	fast speed DSUR without verify
	DSUR	step-down set and step-up reset
	USUR	step-up set and step-up reset
	DSDR	step-down set and step-down reset
	USDR	step-up set and step-down reset

- Key points of FS-DSUR:

✓ Dynamic self-adaptive write
✓ Step down set pulse series
✓ Skip read verify process

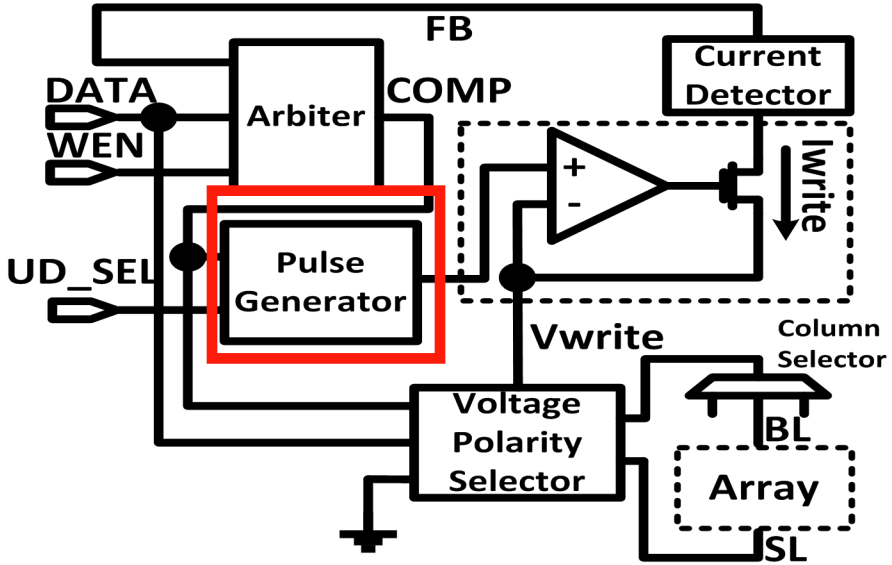
Write driver circuit of FS-DSUR



Key points

- Current Detector senses the write current I_{write} to judge the resistance switching point. Whenever set or reset is successful, FB signal will be enabled.
- Arbiter determines whether to cut off the write stimulus based on the feedback signal FB.

Write driver circuit of FS-DSUR



Key points

- step-up and step-down pulse series generator

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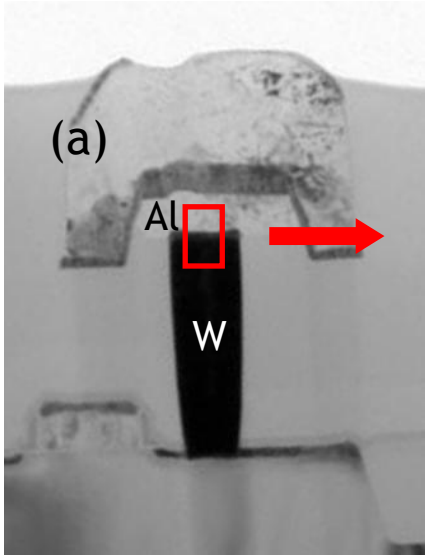
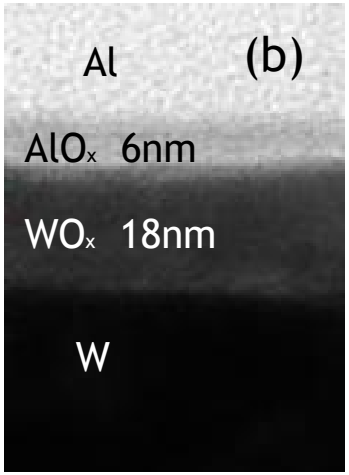
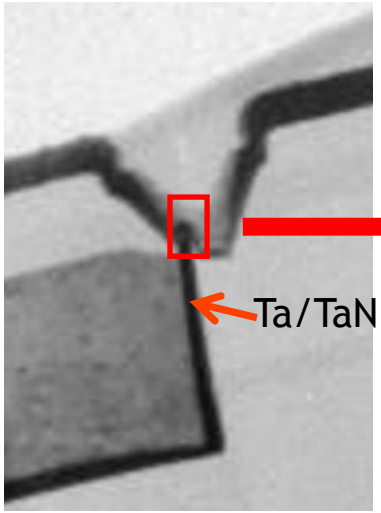
Verification on 0.18 μm(Al BEOL) and 0.11 μm(Cu BEOL) standard logic process respectively







Feature:

- fabricated by standard logic process
- logic friend material/structure
- yield and reliability assist by circuit and algorithm

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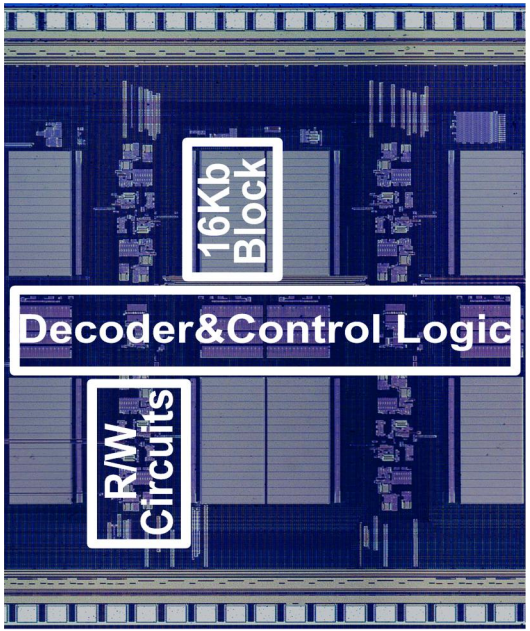
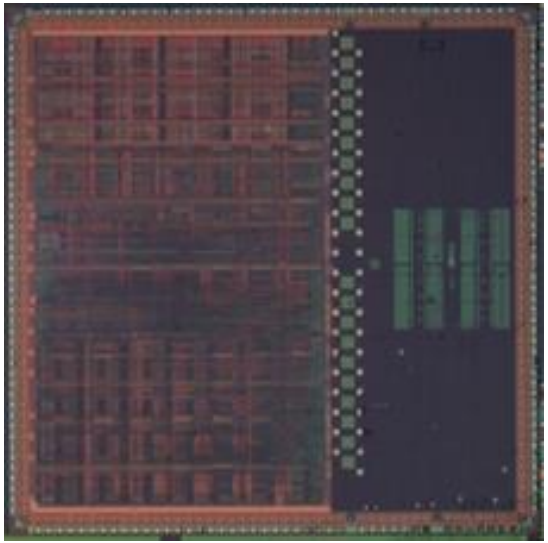
Verification on Chip by 0.18 μ m(Al BEOL)and by 0.11 μ m and 0.13 μ m(Cu BEOL) logic process respectively



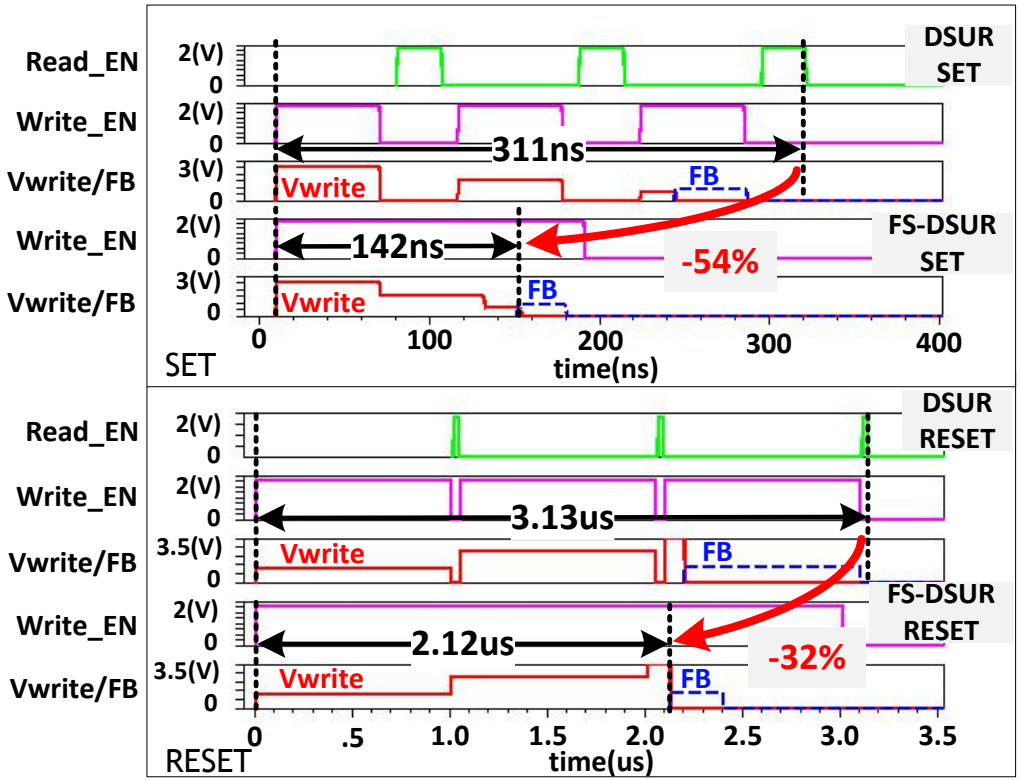
128kb AlO_x/WO_x RRAM test chipChip based on 0.18μm logic Al BEOL
Meausred results are shown in the following Slides



256Kb RRAM IP embedded in CPU test chip based on 0.13μm logic Cu BEOL

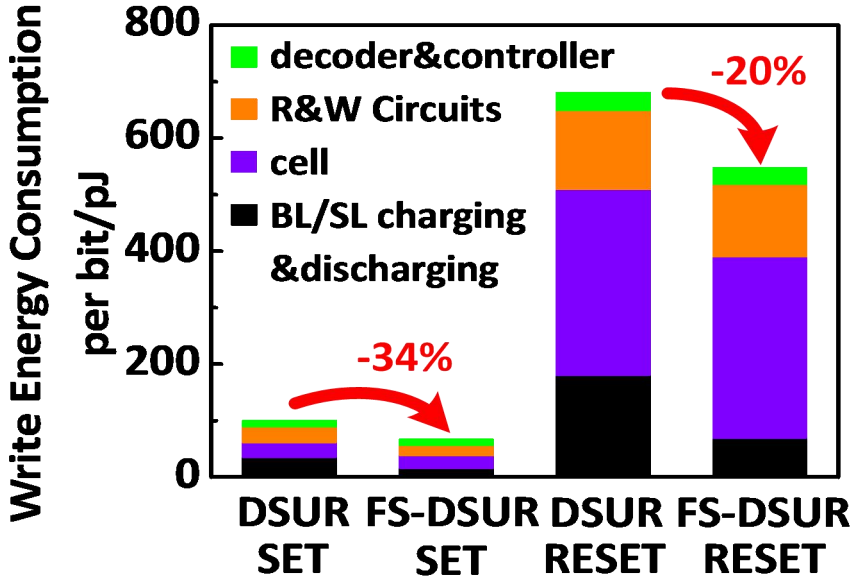
FS-DSUR reduces set/reset access time

due to skip of read verify



FS-DSUR reduces set/reset energy

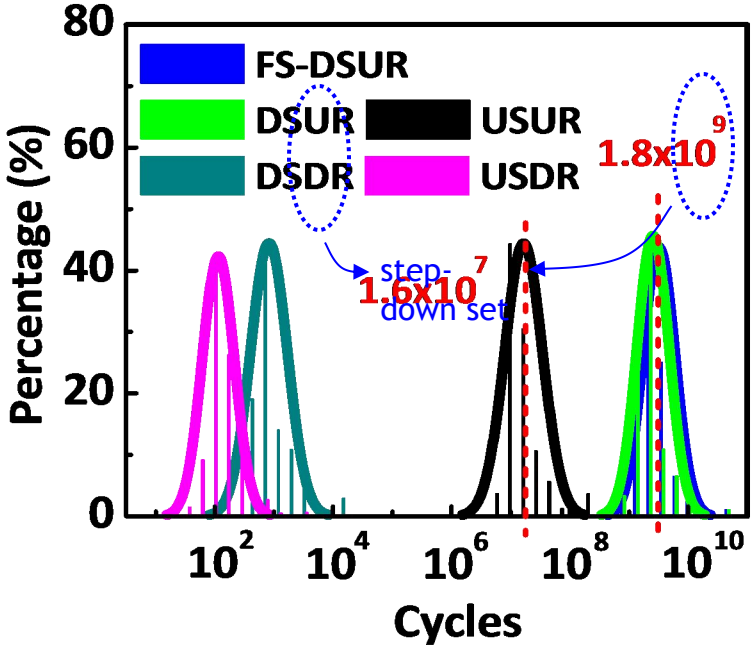
due to skip of read verify



✓Charging/discharging energy consumption of BL/SL decrease significantly.

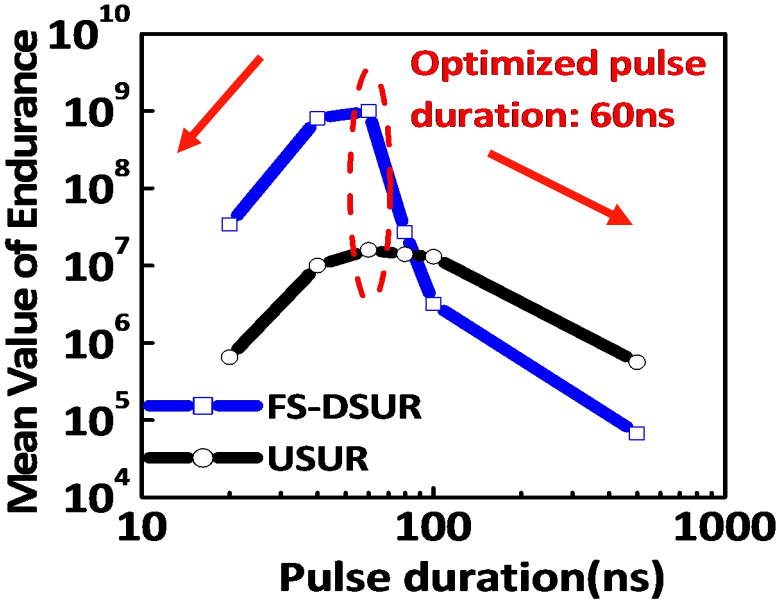
Endurance enhancement with FS-DSUR

- Set/Reset pulse duration: 60ns/1us
- Statistic result based on the same 128Kb test macro



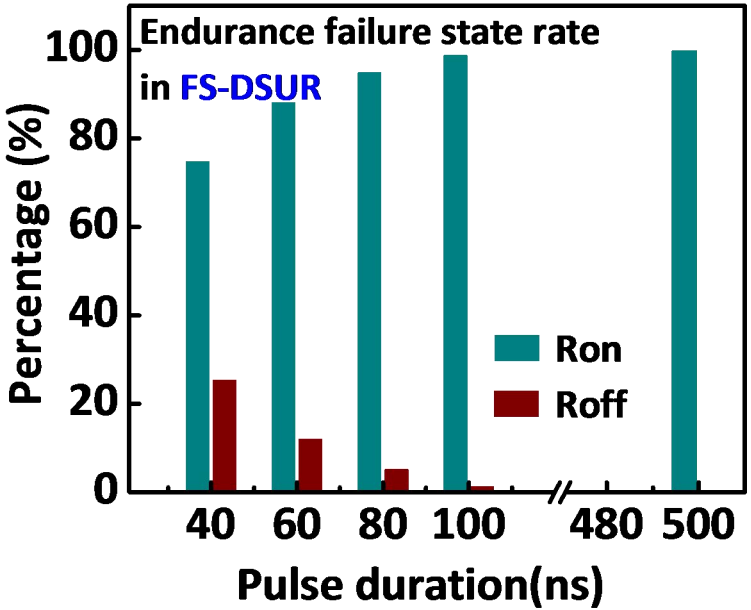
- ✓ Endurance enhanced about 2 orders by FS-DSUR compared with USUR
- ✓ Step-down set improves endurance obviously !
- ✓ Step-down reset significantly decrease endurance !

Endurance vs. Set pulse duration



✓ Too small and too large set pulse duration both decrease endurance
✓ FS-DSUR makes endurance more worse than USUR in large set pulse duration

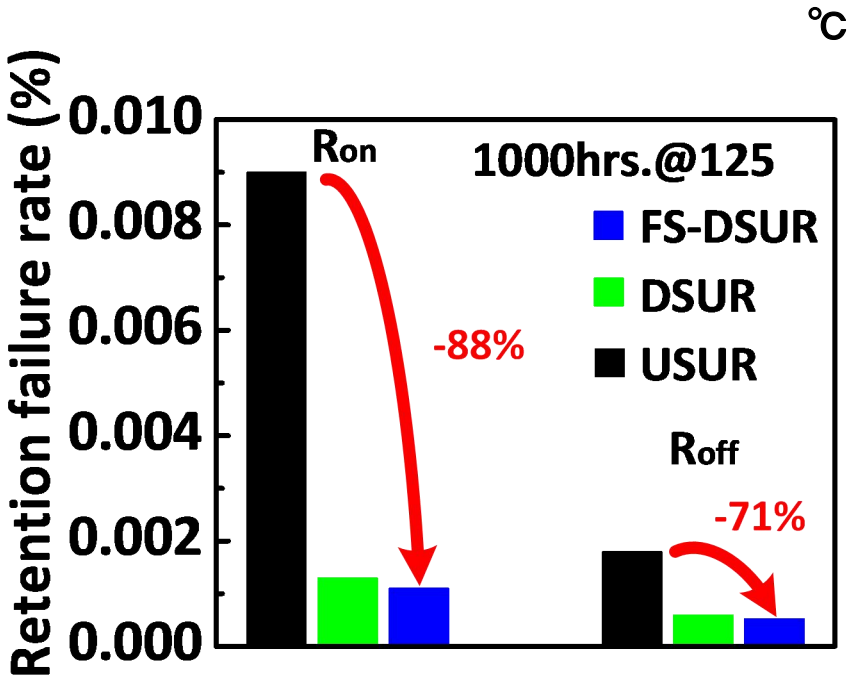
Endurance failure state rate in FS-DSUR



✓ More than 90% of endurance failure happens at R_{on} state (reset fail)
✓ The longer the set pulse duration, the higher the endurance failure rate at R_{on} state, the more difficult for reset

Retention failure rate reduced by FS-DSUR

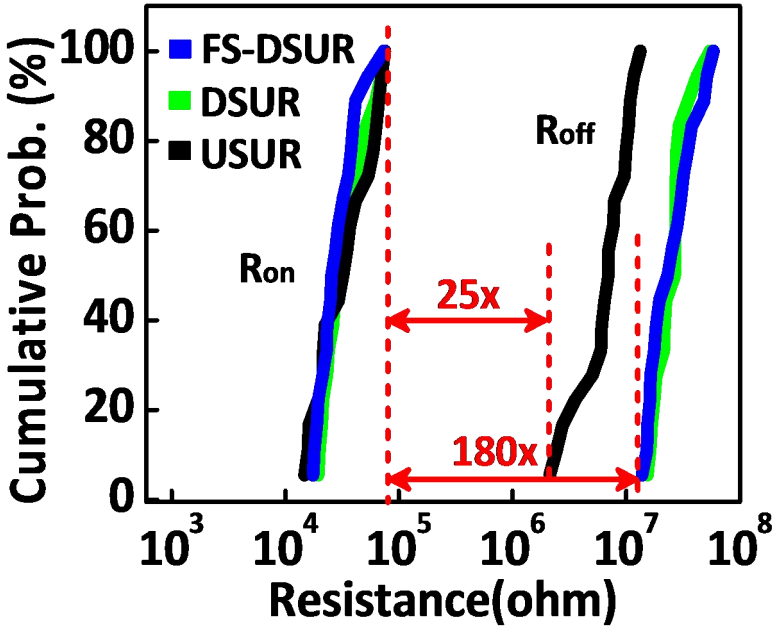
•Set/Reset pulse duration: 60ns/1us



✓ FS-DSUR drastically reduces retention tail bits failure rate for both R_{on} and R_{off} after 1000hrs.@125℃.

R_{off}/R_{on} window enlarges by FS-DSUR

•Set/Reset pulse duration: 60ns/1us



✓ FS-DSUR can get higher Roff, hence larger R_{off}/R_{on} window

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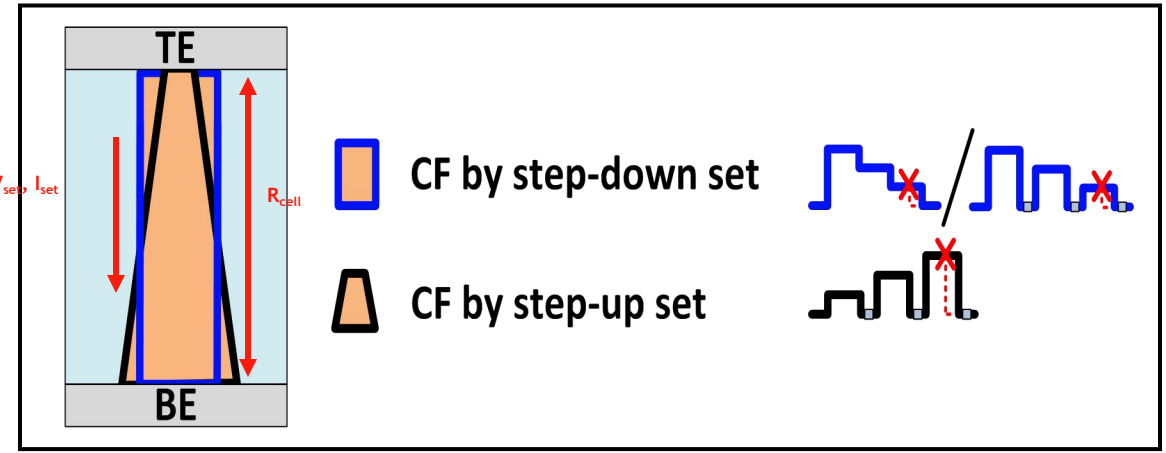
Step-down set refines CF size and shape

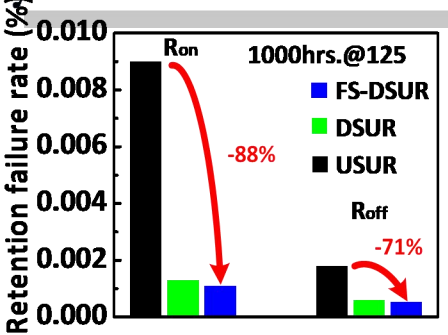


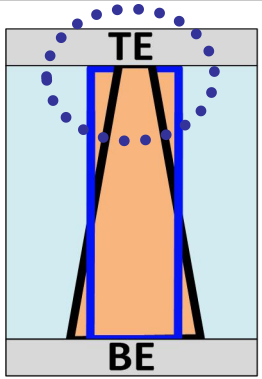
✓V_{set} step pulse applied, Vo and O ion generated, CF forms gradually, R_{cell} reduces step by step

✓R_{cell} reduces, higher next V_{set} step leads to larger I_{set}, hence thicker and stronger next CF parts, conical CF shape forms(step-up set)

R_{cell} reduces, reduce next V_{set} step to control uniform I_{set}, hence uniform next CF parts, cylindrical CF shape forms (step-down set)

Retention benefits of step-down set



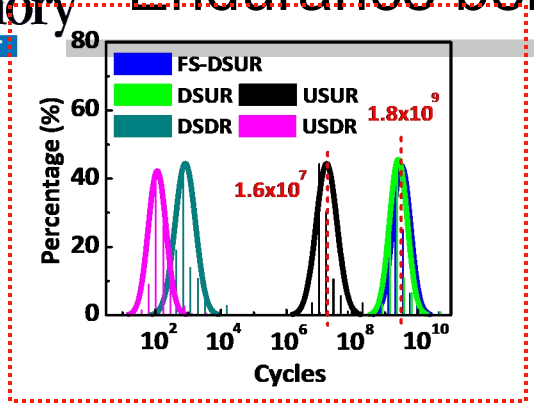


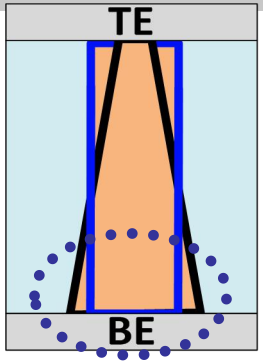
Optimized SET

Good for retention!

✓ Retention failure caused by thermal diffusion of the weakest CF part
✓ Higher first step voltage of step-down set forms larger CF size near TE, strengthen the weakest CF parts, hence good for retention

Endurance benefits of step-down set



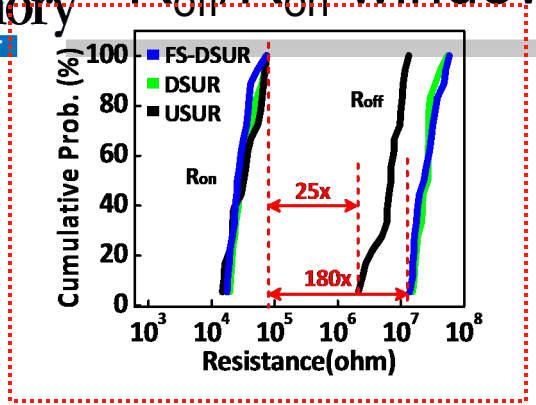


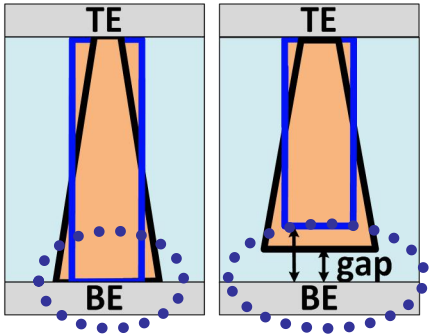
Optimized SET

Good for endurance!

✓ The depletion of movable O ions lead to endurance failure
✓ Higher set step voltage applies on relatively low CF resistance, hence thicker CF size near BE (caused by step-up set)
✓ Smaller CF size near BE consumes less O ion to rupture CF during reset by Vo and O ion recombination, hence good for endurance

R_{off}/R_{on} window enlarges by step-down set

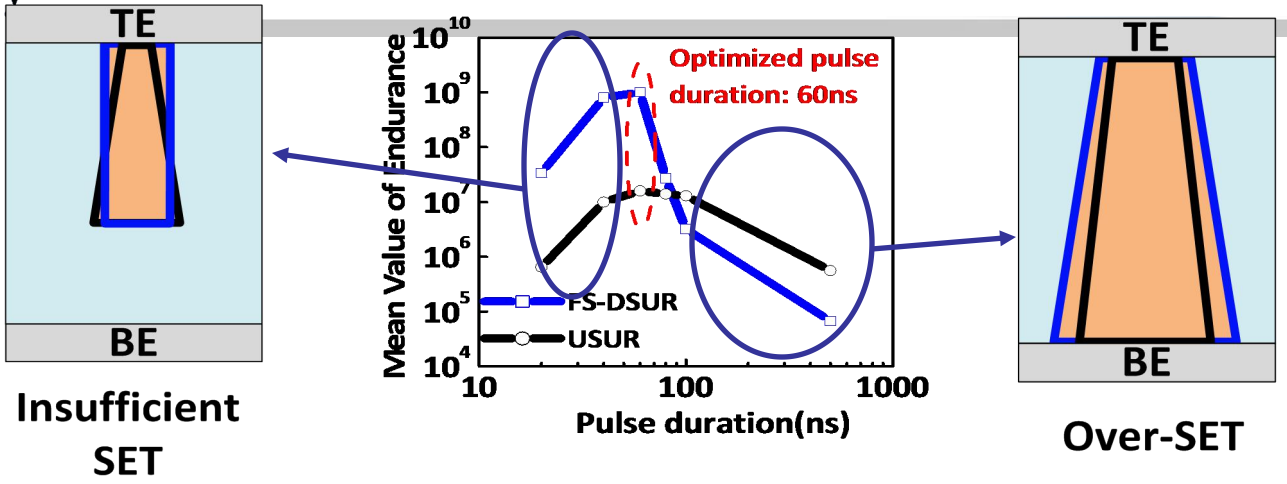




Higher Roff benefits!

✓ Smaller CF size near BE by step-down set leads to larger CF gap during Vo and O ion recombination in reset, hence higher R_{off} and tighten distribution achieves, R_{off}/R_{on} window enlarges

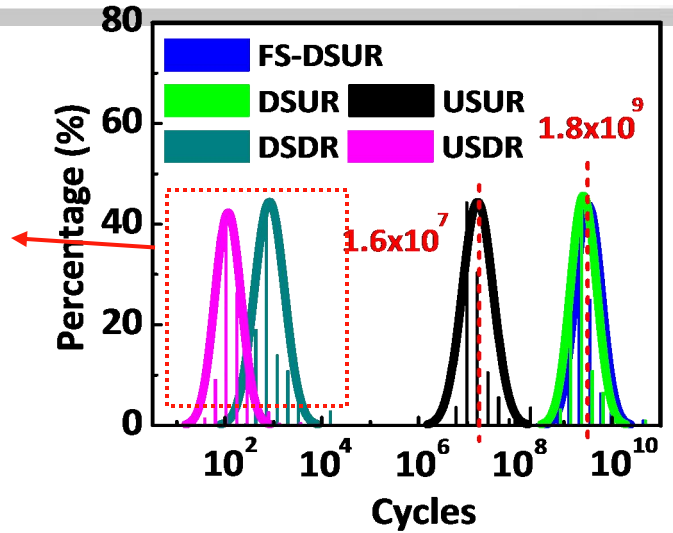
Insufficient- and over- set



✓Insufficient-set : CF has not formed yet under too short set pulse
✓Over-set : Serious conical CF shape caused by step-down set under too long set pulse since the first voltage step is higher than step-up set, endurance becomes more worse

Step-down reset damage endurance

step up/down set with
step-down reset



✓Initial large reset voltage step applied on minimum R_{on} state will cause the generation of large joule heat
✓More and more non-movable Vo is generated by large joule heat
✓Endurance performance becomes worse

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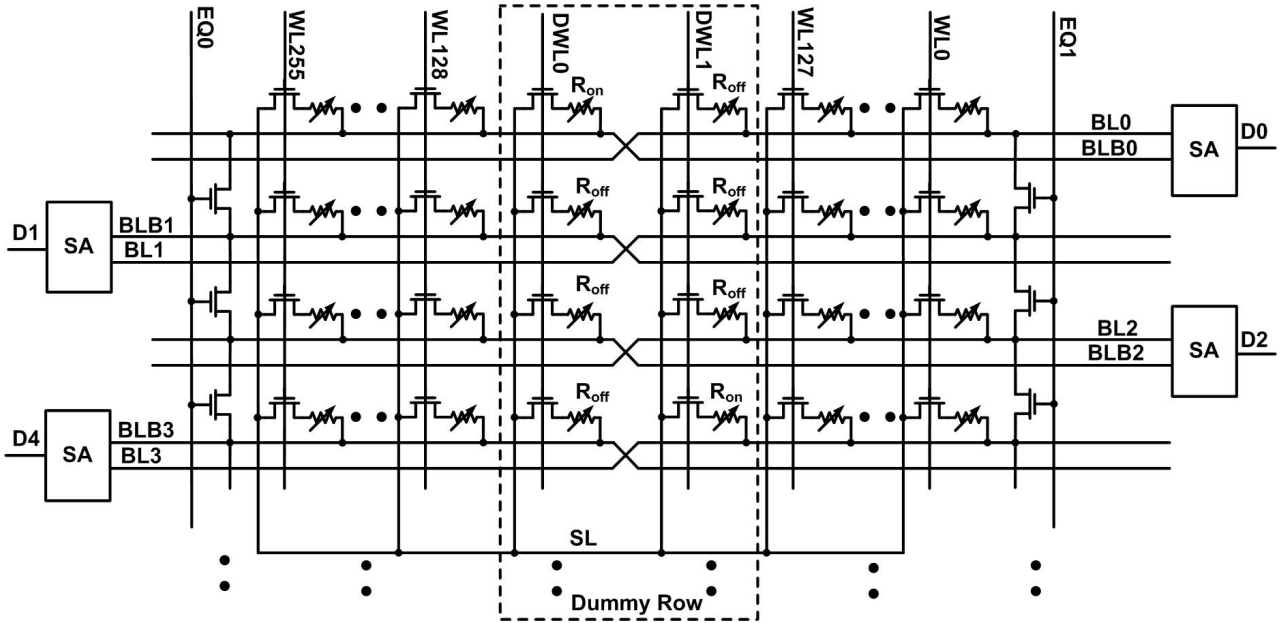
SARM (Self-Adaptive Read Mode) Reference

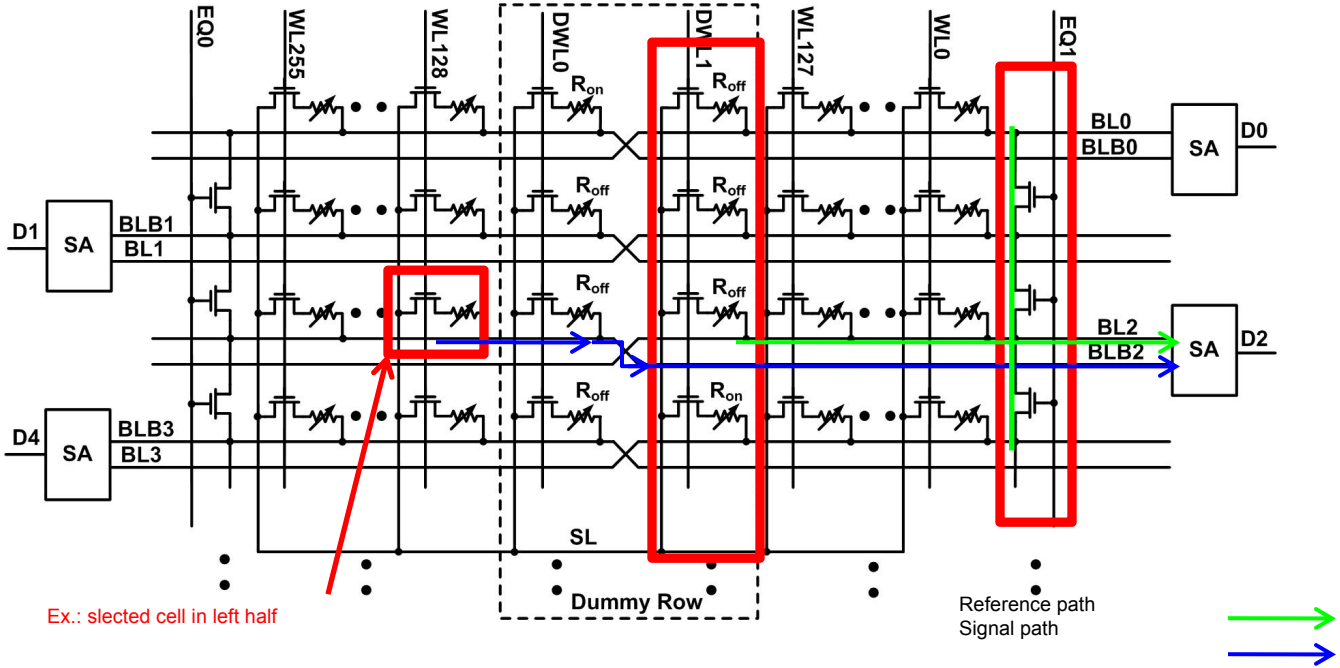


Array Architecture for SARM

Key points:

- Two dummy rows are embedded in array for SARM generation;
- On-pitch SA has a width of two adjacent columns.

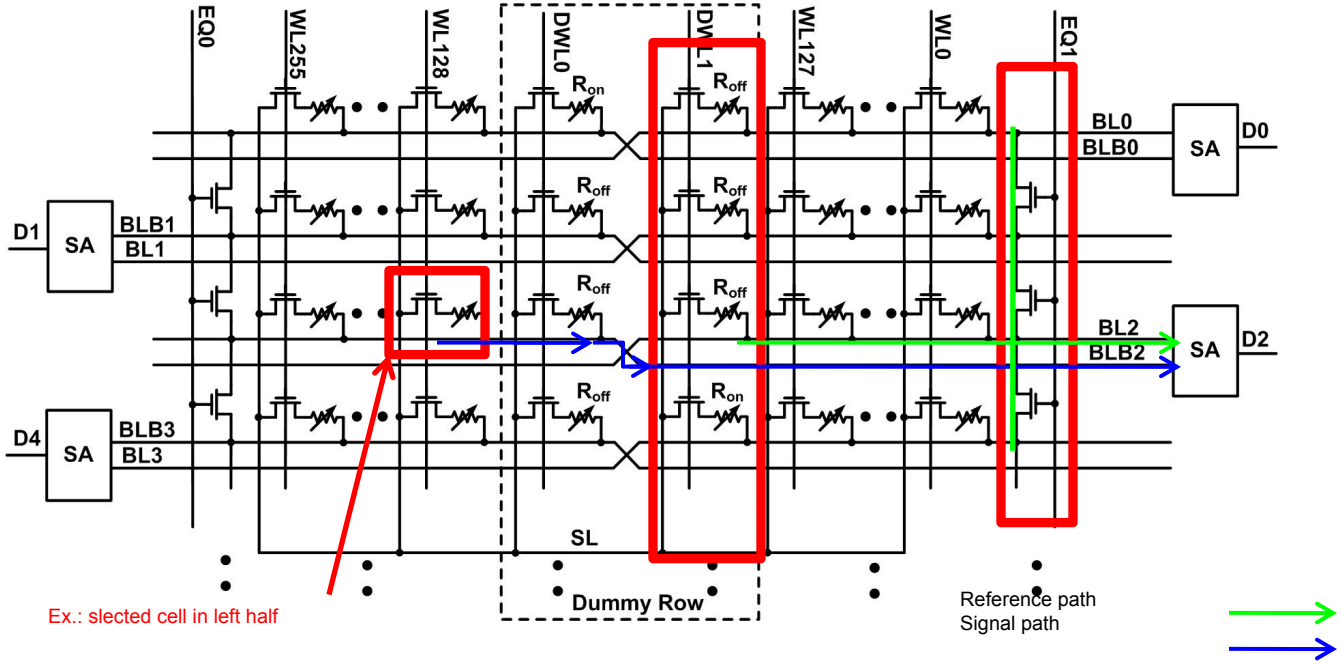
SARM (Self-Adaptive Read Mode) Reference (cont.)



SARM Reference Generation:

- Dummy row in different half is activated.
- Equalizaton transistors in the same half with dummy row are also activated for V_{BL} averaging.

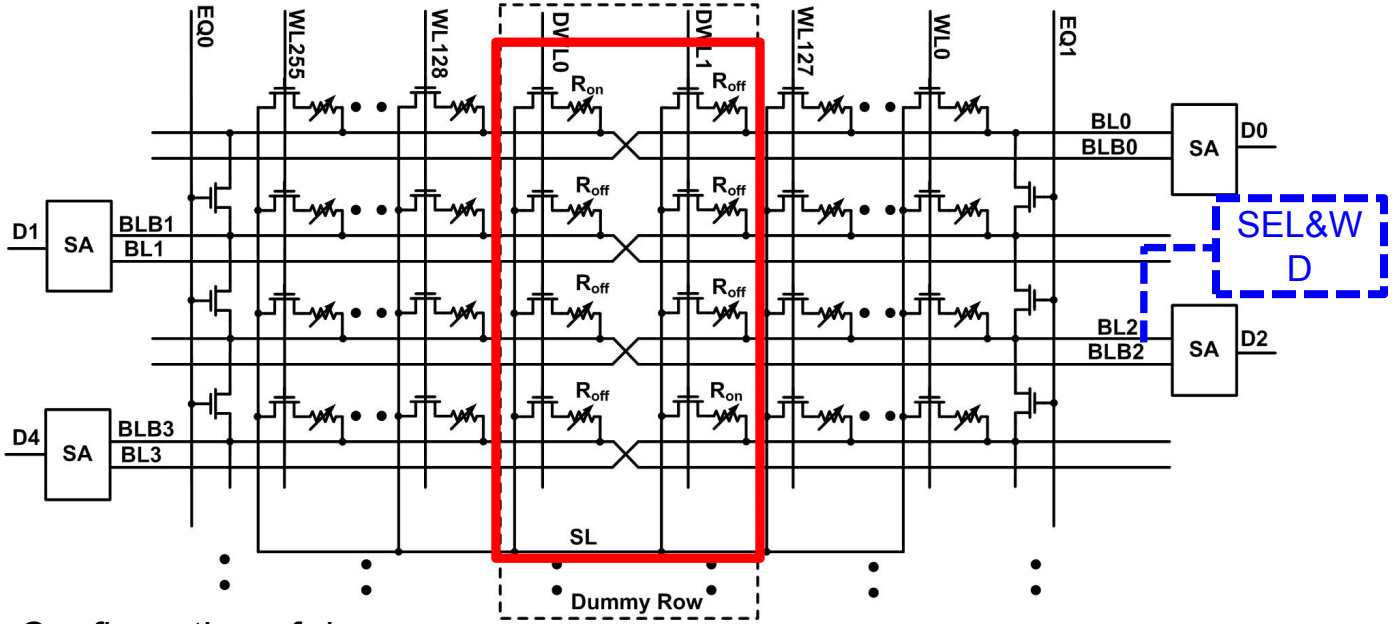
SARM (Self-Adaptive Read Mode) Reference (cont.)



Benefits of SARW reference by averaging dummy row:

- PVT variations in RRAM cells are tracked;
- The effect of rare tail bit is avoided.

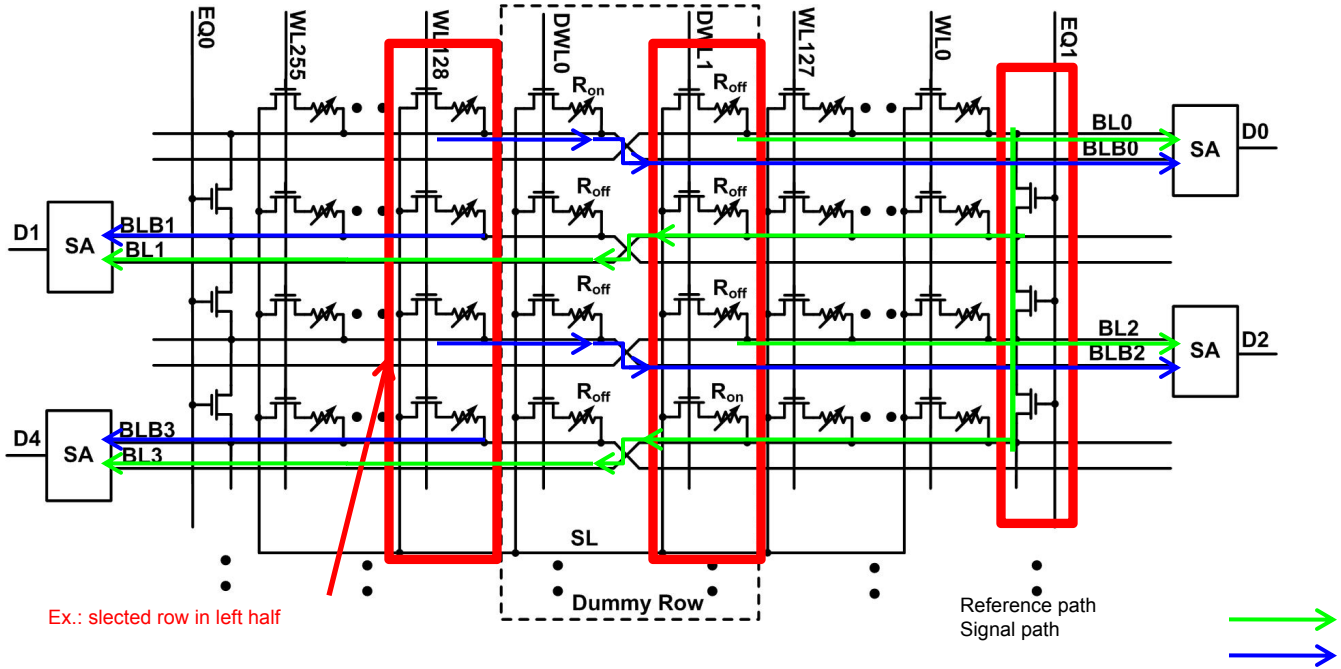
SARM (Self-Adaptive Read Mode) Reference (cont.)



Configuration of dummy row:

- Share the same WD and selector circuits with normal rows, thus low peripheral overburden.
- Configuration pattern is determined by practical R_{cell} distribution, thus for large sense margin.

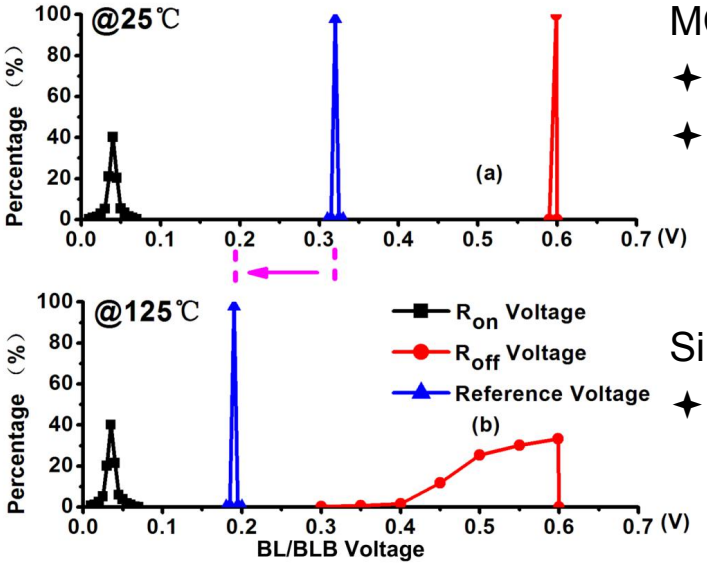
SARM (Self-Adaptive Read Mode) Reference (cont.)



High bandwidth read:

- Multiple SAs work at the same time.

SARM (Self-Adaptive Read Mode) Monte Carlo Simulation for Verification



MC simulation condition:

- Based on 1000 samples;
- Dummy row is configured as one R_{on} every 7 R_{off}'s according to practical R_{cell} distribution.

Simulation result:

- The reference voltage adaptively dynamically moves towards R_{on} direction to ensure enough sense margin at 125℃. Thus, read failure is avoided. R_{off}/R_{on} degradation issue is solved.

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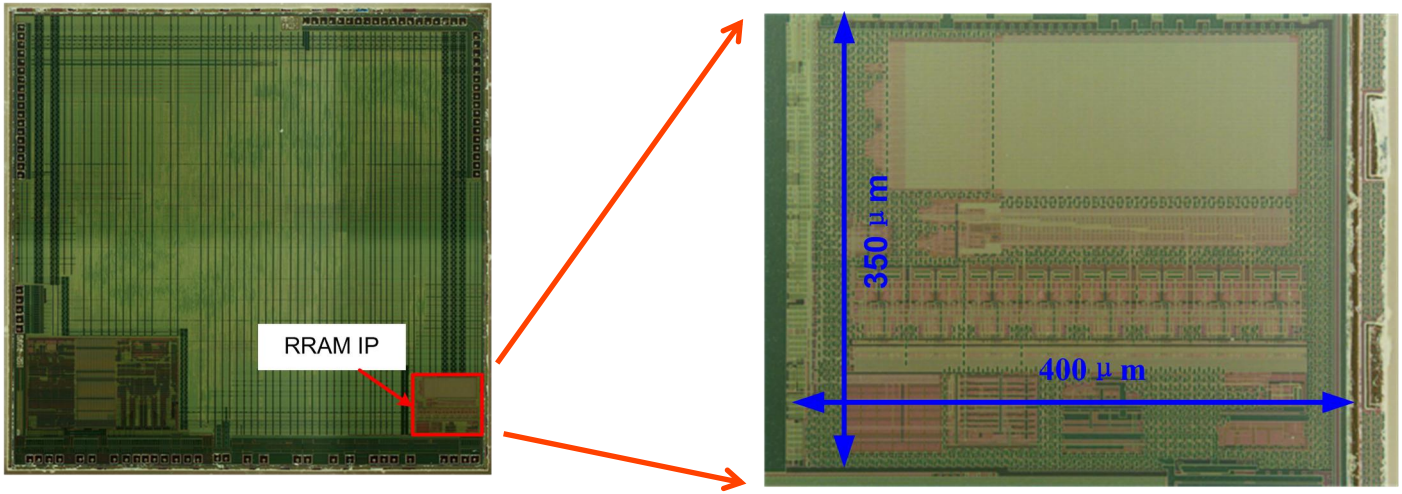
Pilot production of 16kb emRRAM IP by 0.11μm logic Cu BEOL process



RRAM IP here is used for security key and information such as true random number.

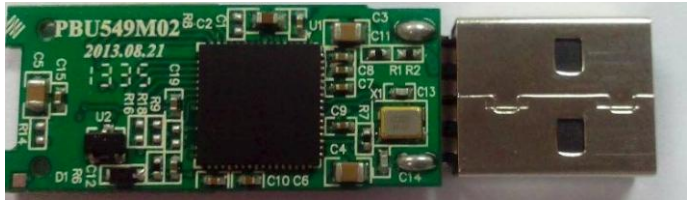
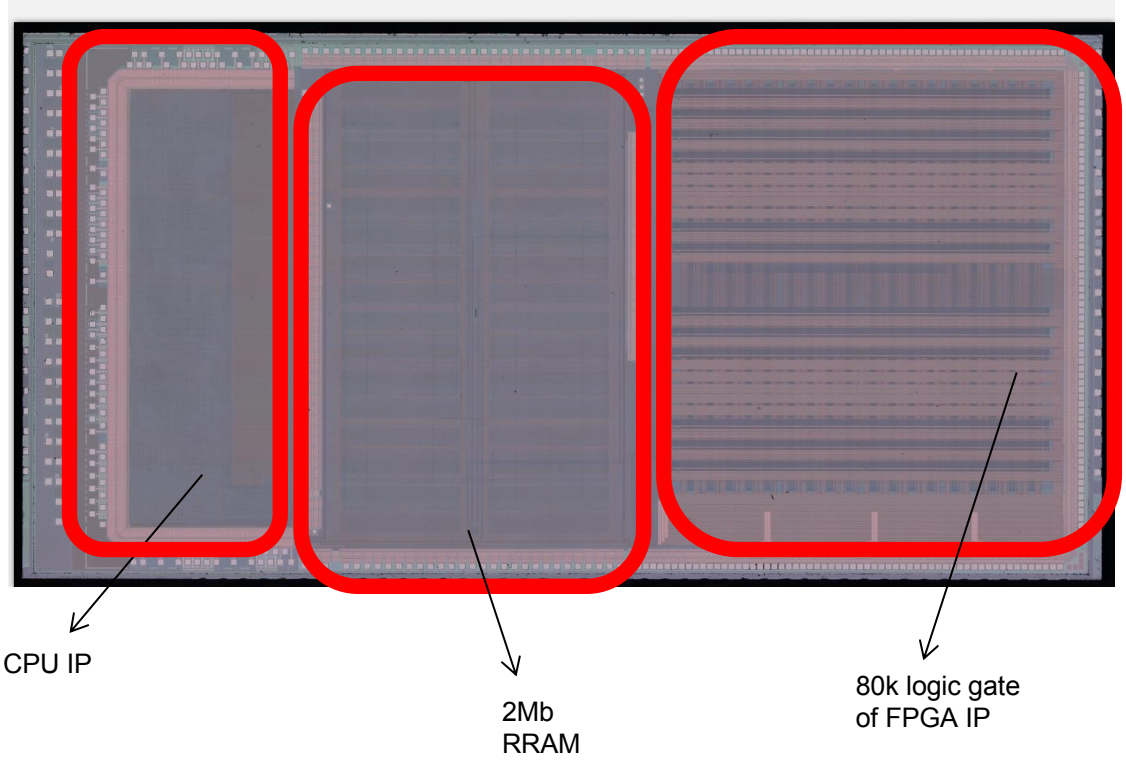


Photo of Customer's product, s261, which has been applied into financial security system.

SOC chip with CPU/FPGA/RRAM



- RRAM is used for configration information of FPGA and other security information like key etc.
- For a encryption application example, the key and encryption algorthim can be reconfigrable.
- The RRAM quality can ensure the critical requirment of no 1 bit error of FPGA configruation.

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Conclusions

- Reliable yield is the key for practical application of emRRAM IP.
- We develop logic-based RRAM technology, and self-adaptive circuits to co-optimize the yield of read/write/retention/endurance.
- Above mentioned co-optimization technology is verified. And embedded applications for information security in CPU product chip and FPGA test chip are demonstrated.

Acknowledgements

- This is team work for years of our research center of semiconductor memory and application of Fudan University. Thanks to all members who contribute, e.g., Ying Meng, Xiao Yong Xue, Jianguo Yang, Yali Song, Gang Chen, Yuxin Wu, Fanjie, Xiao, Yufeng Xie, etc..
- Thanks to our co-research partner on RRAM fabrication in product line, SMIC(Shanghai), especially appreciation to Dr. Jingang Wu, Ryan Huang, Qingtian Zou.
- Thanks to our product customer partner, Sage Micro. Corp., for their co-research of IP application in product.
- Thanks to groups of Prof. Xiaoyang Zeng and Zhiyi Yu, Prof. Lilang Wang and , Prof. Hao Min, etc., for their co-research in emRRAM IP applications.

Thanks!