Emerging Memories

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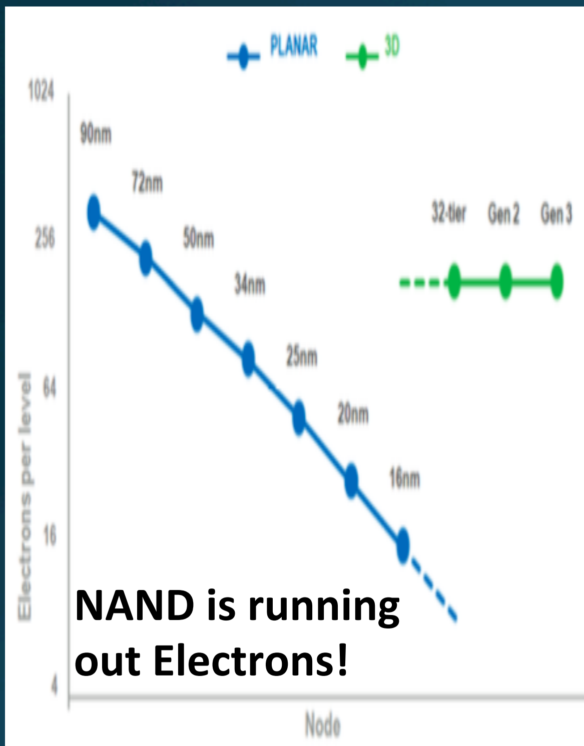
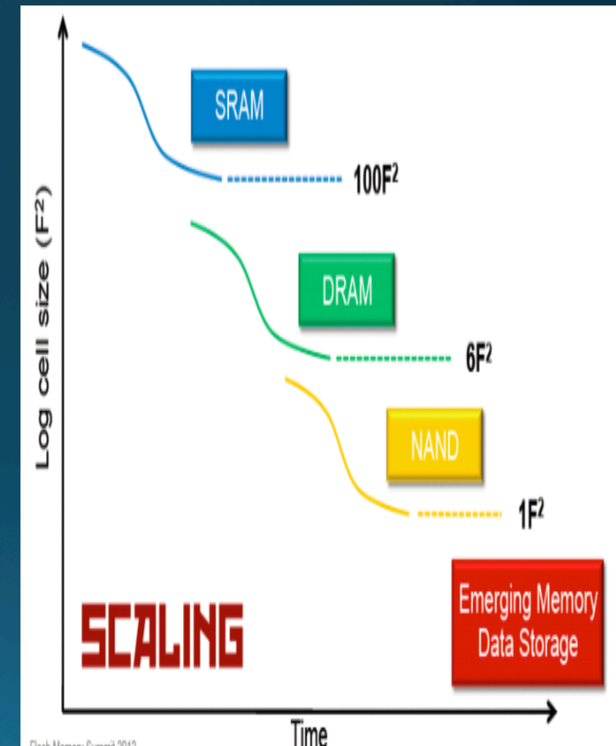
Main stream memories are charge based and are loosing momentum!





Emerging memories are needed; *400 Patents in 2015!*

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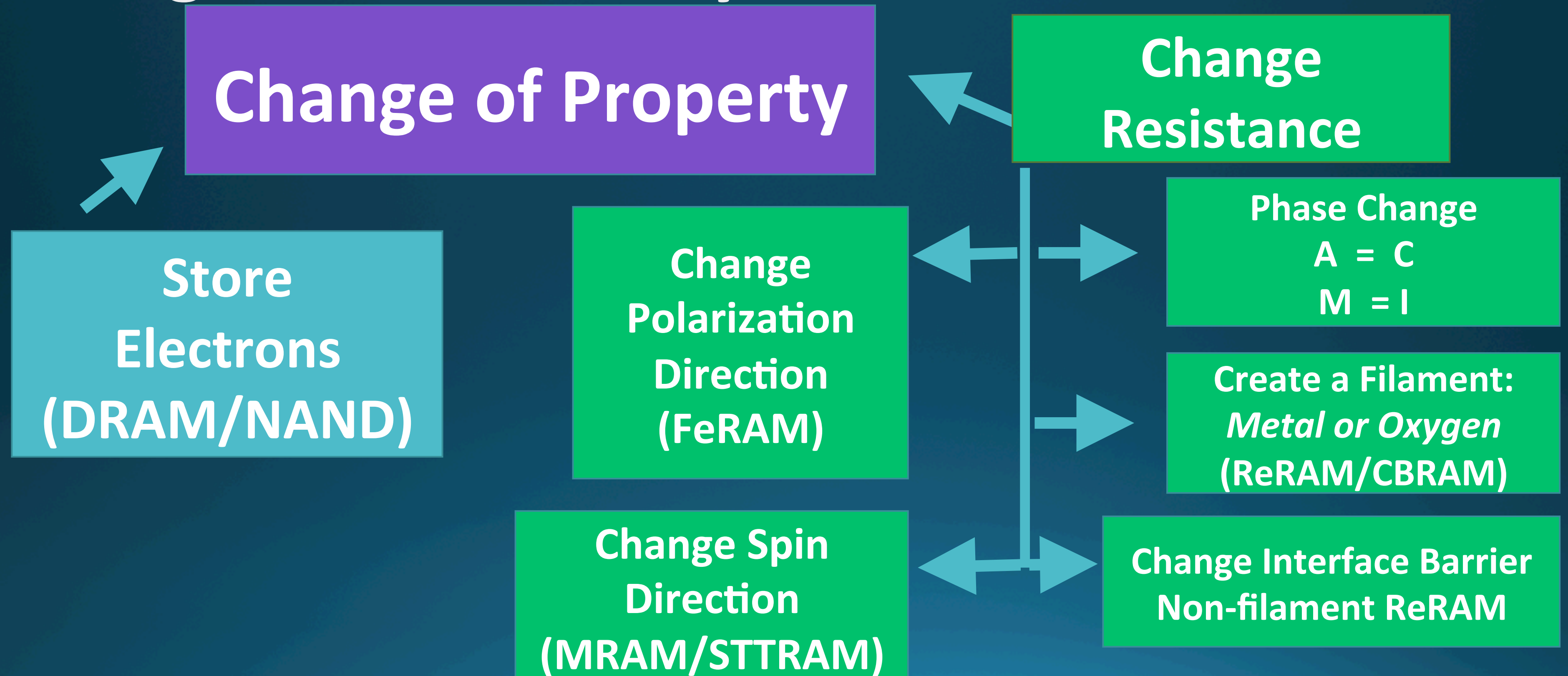
Memory device is possible, if a property can be changed electronically into different states
Change of Property
Change Resistance
Store Electrons (DRAM/NAND)
Change Polarization Direction (FeRAM)
Phase Change
A = C
M = I
Create a Filament:
Metal or Oxygen
(ReRAM/CBRAM)
Change Spin Direction (MRAM/STTRAM)
Change Interface Barrier
Non-filament ReRAM
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Memory Development Phases

Risk

Value

- Single memory cell
- Proof of concept
- Selector
- Scaling potential

- Memory array
- Selector integration
- Significant statistics
- Scaling limits
- Proximity effects
- CMOS integration

- Yield improvement
- Packaging
- Product testing
- Product qualification

Research

Development

Production

Time

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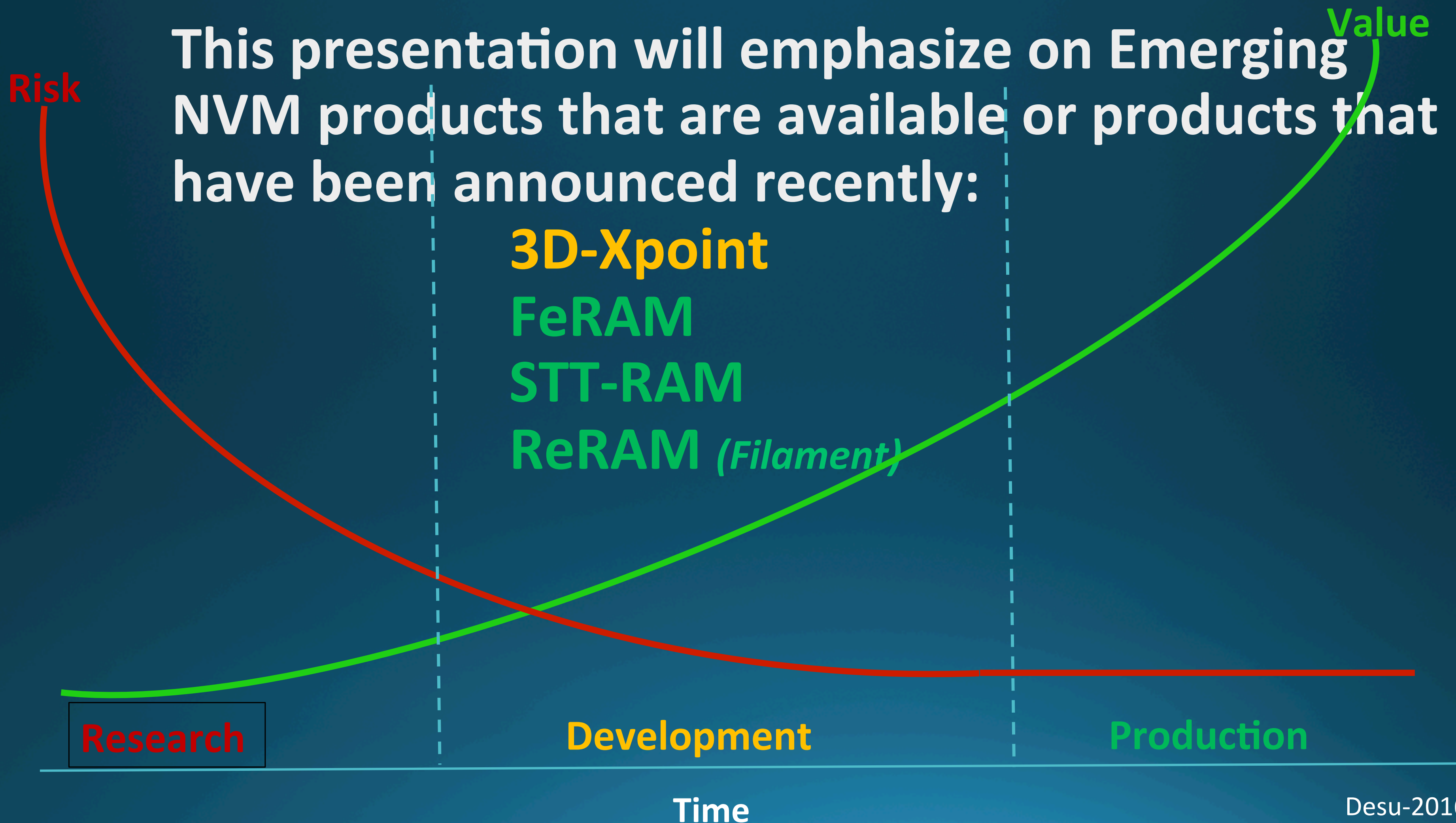

This presentation will emphasize on Emerging NVM products that are available or products that have been announced recently:
3D-Xpoint
FeRAM
STT-RAM
ReRAM (Filament)
Risk
Value
Research
Development
Production
Time
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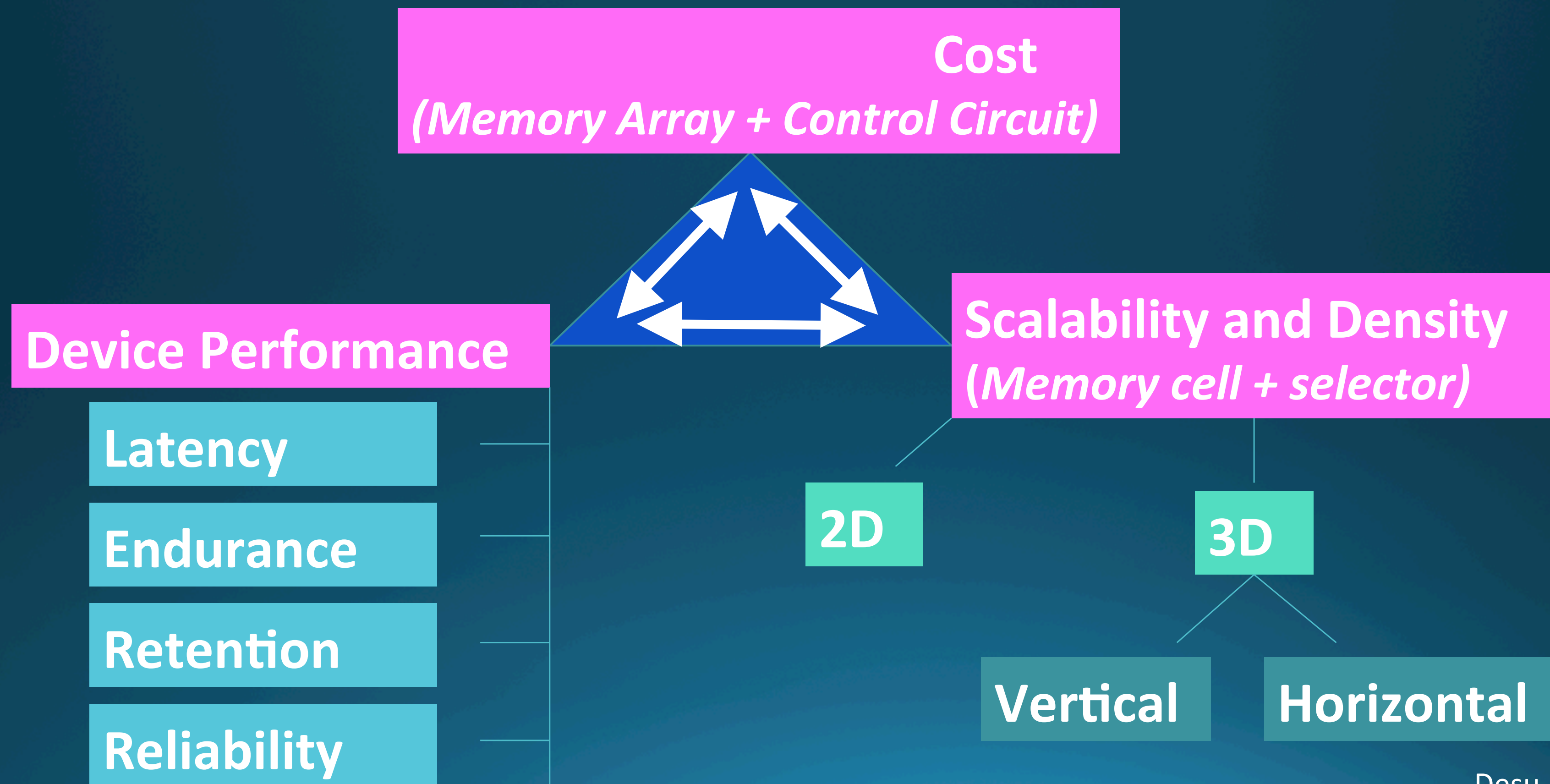
Most Important Metrics for Emerging Memories
Cost
(Memory Array + Control Circuit)
Device Performance
Latency
Endurance
Retention
Reliability
Scalability and Density
(Memory cell + selector)
2D
3D
Vertical
Horizontal
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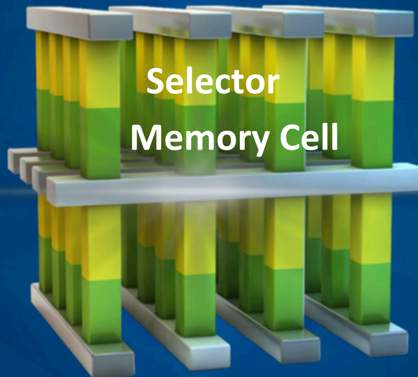
3D X-Point by Intel and Micron

WHAT IS 3D XPOINT™?

Crosspoint Structure
Selectors allow dense packing and individual access to bits

Scalable
Memory layers can be stacked in a 3D manner



Breakthrough Material Advances
Compatible switch and memory cell materials

High Performance
Cell and array architecture that can switch states 1000x faster than NAND

THE BREAKTHROUGH

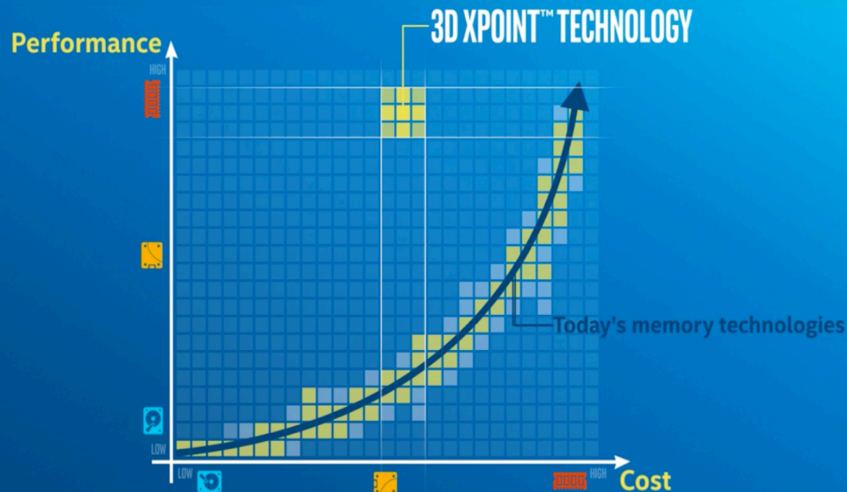
A NEW CLASS OF NON-VOLATILE MEMORY

1000X FASTER THAN NAND

1000X ENDURANCE OF NAND

10X DENSER THAN CONVENTIONAL MEMORY

*Results have been estimated or simulated using internal analysis or architecture simulation or modeling, and provided to you for informational purposes. Any differences in your system hardware, software or configuration may affect your actual performance



3D XPOINT™ ENABLES FUTURE APPLICATIONS

END USER POSSIBILITIES

- Massive in-memory data base
- Fast system recovery
- Low latency
- High endurance

- Gaming
- High fidelity pattern recognition
- Genomics

AMAZING NEW EXPERIENCES

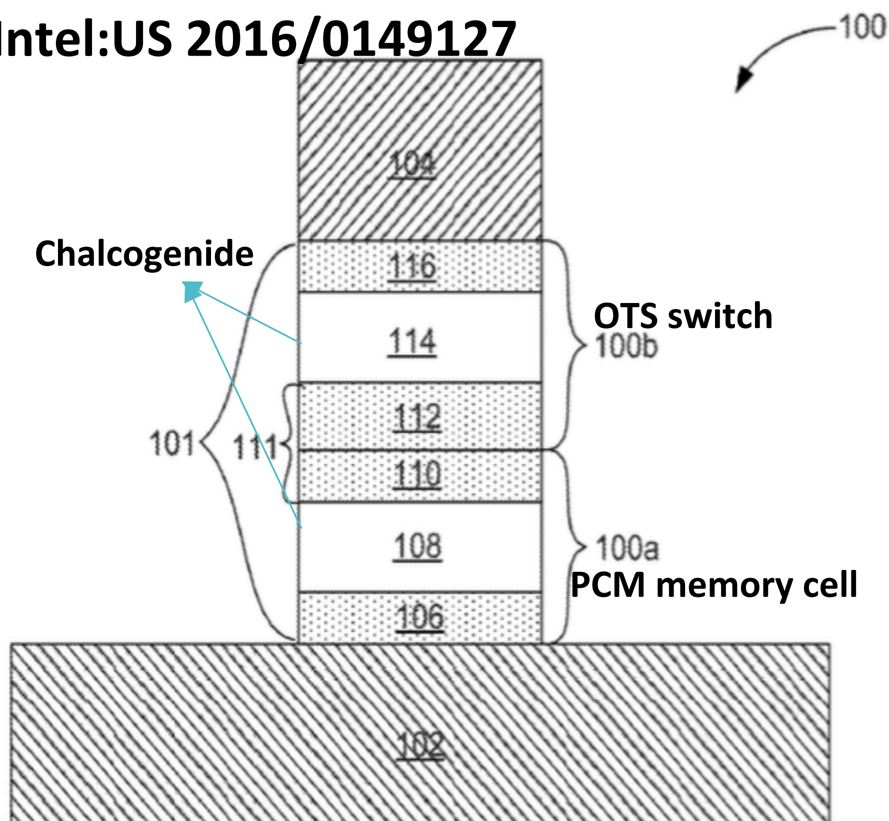
What did they reveal about 3D X-Point?

- Non-volatile memory is NOT based on a filament
- Non-Volatile memory is based on bulk-resistance change
- The memory material is a chalcogenide
- They also insist it is not a Phase Change Memory!
- Ovonic Threshold Switch (OTS) is the Selector
- It could take 12-18 months to get into mass production (Jan 2016)

- Uses ~100 new materials (raising supply chain issues)
- Lots of process steps to control the cross contamination
- 128 Gbit (in two planes) suggest ~19 nm feature size
- No retention numbers

Patents assigned to Intel and Micron indicate that 3D X-Point is 'a flavor of PCM'

Intel:US 2016/0149127



Other Similar Patents Assigned to Intel/Micron:

US 9,236,566 (2016)/Micron
US 9,299,747 (2016)/Intel
US 9,299,930 (2016)/Micron
US 9,343,676 (2016)/Micron
US 9,362,494 (2016)/Micron
US 9,064,560 (2015)/Iintel
US 8,953,387 (2013)/Micron
....

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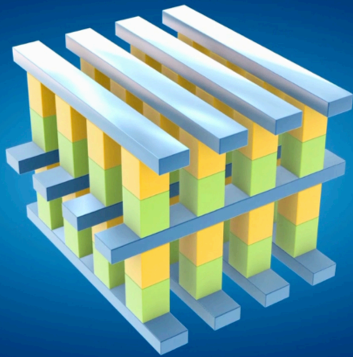
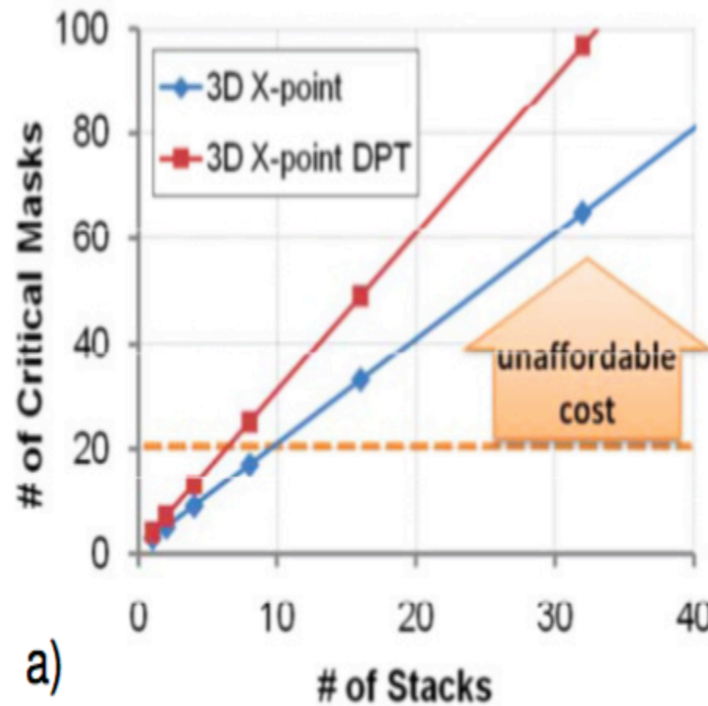
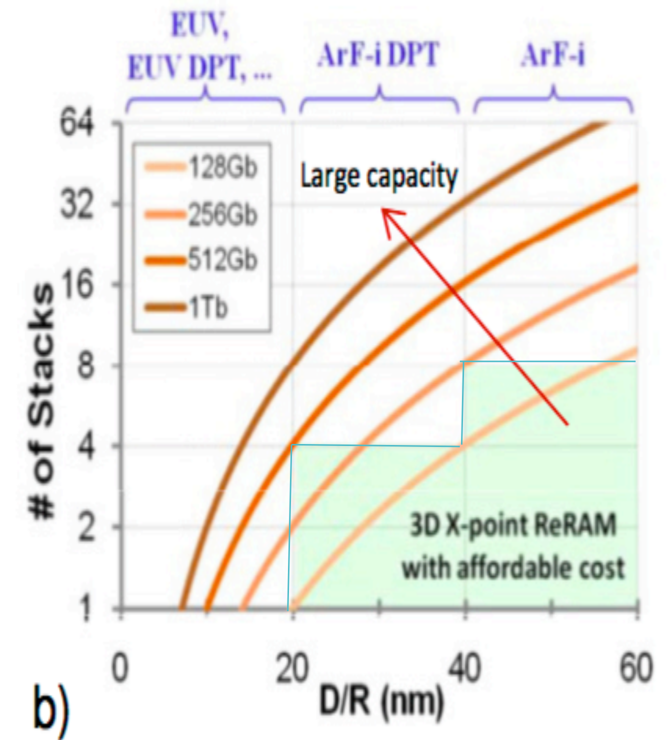
Stacked 3D cross-point architecture is not cost effective if the number layers increase



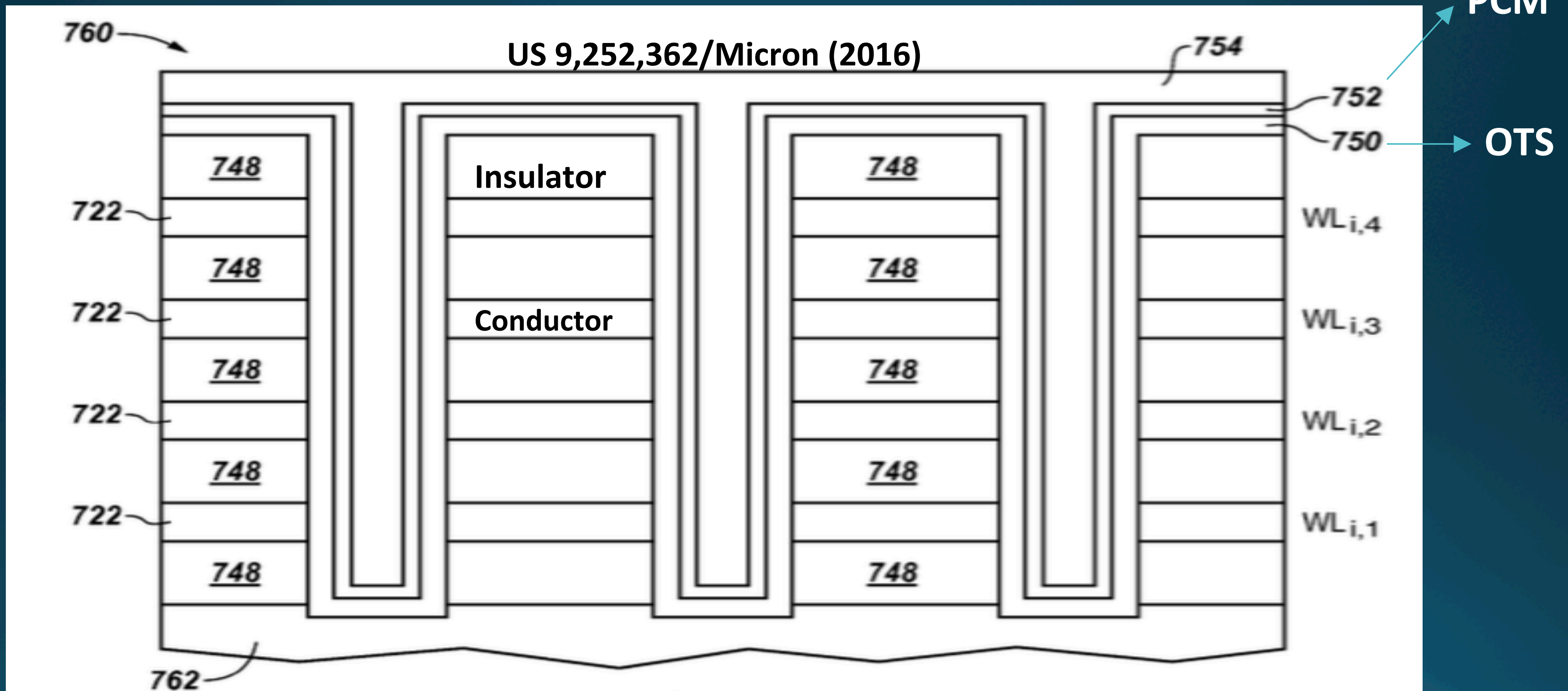
I. Baek, et al, IEDM 2011





Cost Limit:
4 stacks,
512Gb?

Solution for the density limitation of stacked 3D X-Point: Vertical?



PCM

OTS

Method for making 3D memory array using Phase Change and Ovonic Switching

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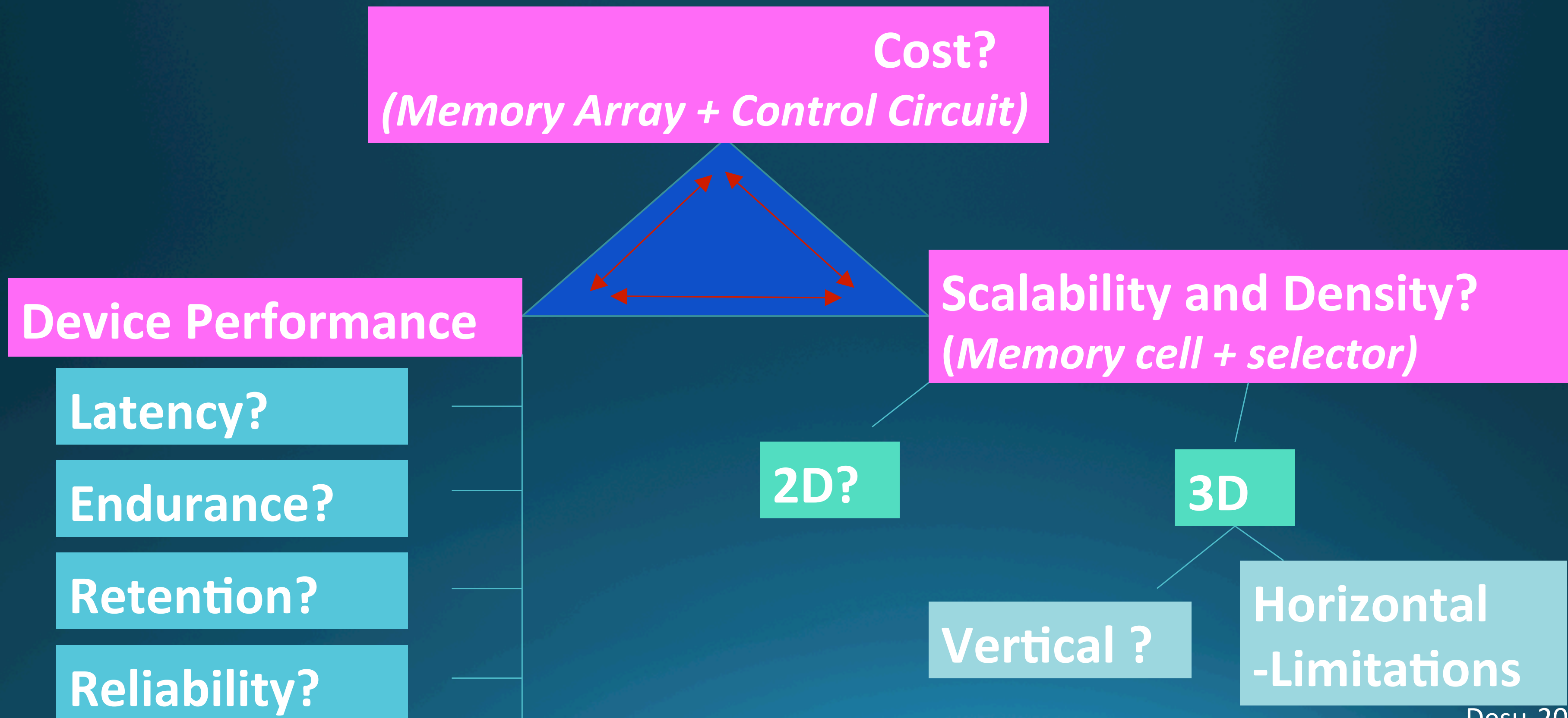
Metrics for 3D X-Point
My Crystal Ball is Foggy!!!
Cost?
(Memory Array + Control Circuit)
Device Performance
Latency?
Endurance?
Retention?
Reliability?
Scalability and Density?
(Memory cell + selector)
2D?
3D
Vertical ?
Horizontal
-Limitations
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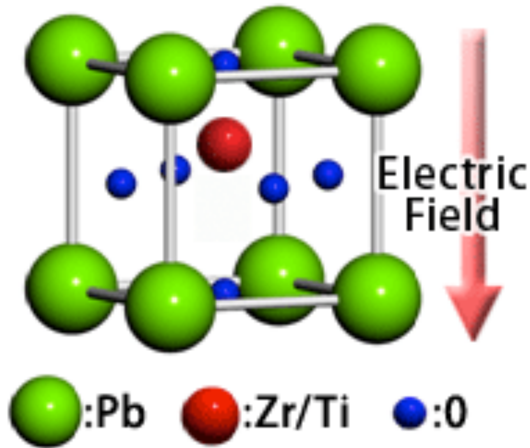
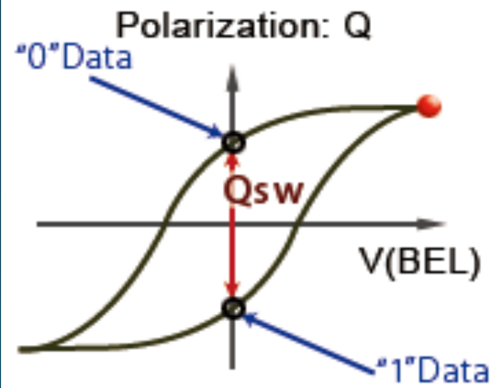
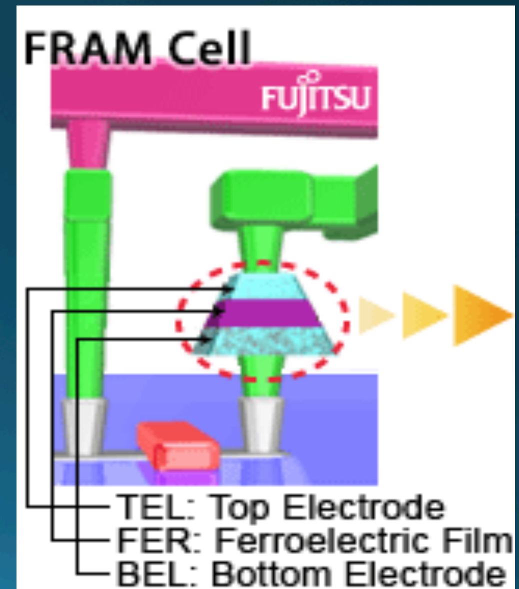
Ferroelectric Random Access Memory (FRAM)







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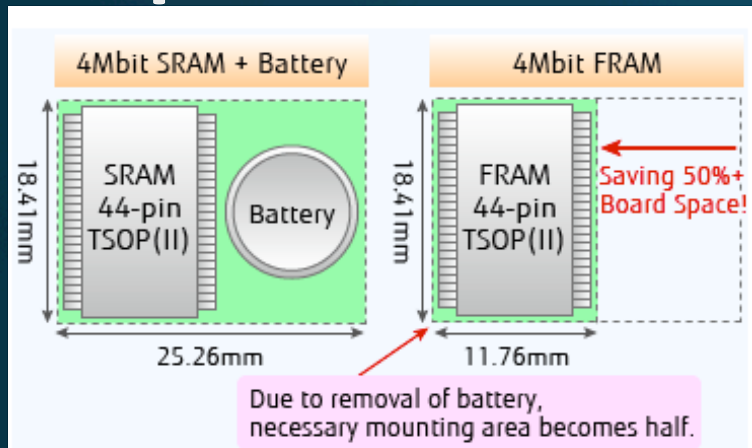
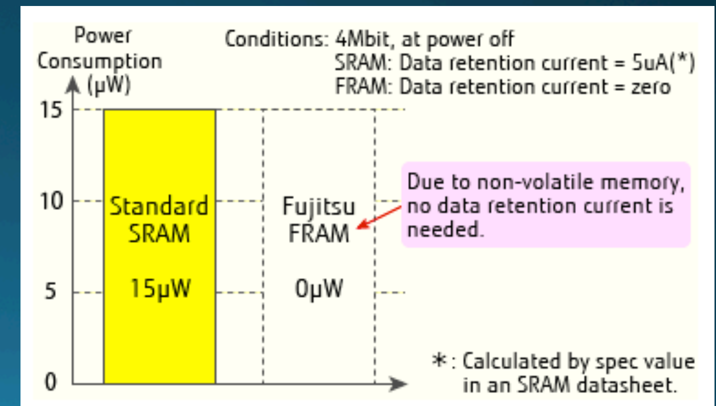
Fujitsu Develops 4 Mbit Quad SPI FRAM Capable of 54 MB/s Data Transfer (2/2016)



- 1.8V to 3.6 V
- -40⁰C to +85⁰C
- 10^{13} Cycles of Endurance
- 10 Years of Retention



- Access Time 75 ns—150 ns
- Operating = 20 mA
- Standby = 150 μA
- Sleep = 20 μA

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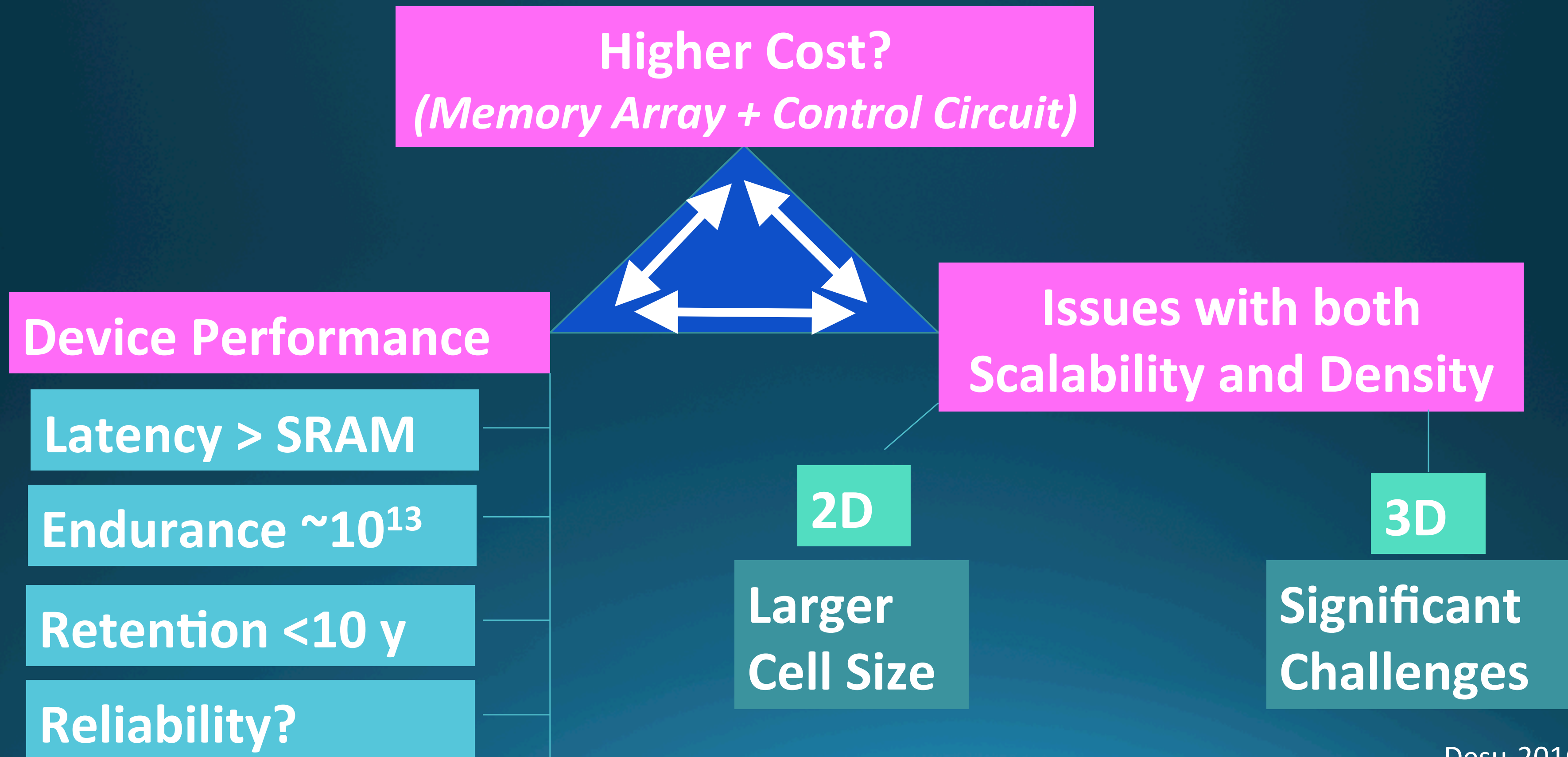
Metrics for FRAM
Higher Cost?
(Memory Array + Control Circuit)
Device Performance
Latency > SRAM
Endurance ~10^13
Retention <10 y
Reliability?
Issues with both Scalability and Density
2D
Larger Cell Size
3D
Significant Challenges
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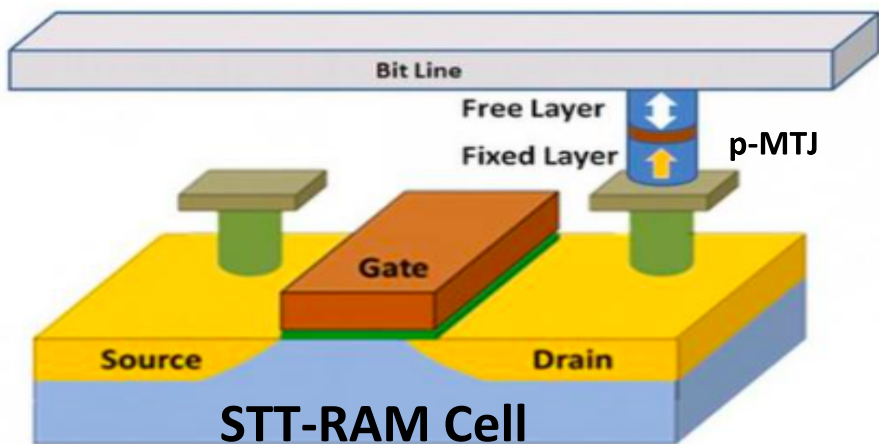
MRAM/STT-RAM

The difference in resistance between Parallel and Anti-Parallel spin arrangements of MTJ is the key for MRAM

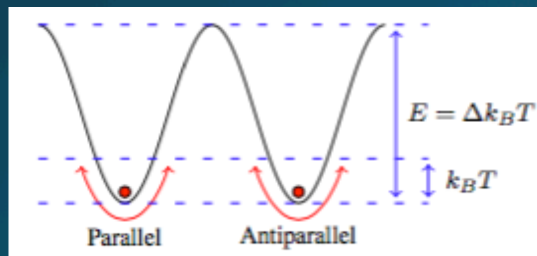


STT-RAM Cell

Non-Deterministic Write

- STT write process is inherently stochastic *(sigmoidal distribution with very long tail)*
- The stochasticity of switching time is temporal *(leading to variation in transition time for a single cell)*

Thermal Stability Factor (Δ) is the key metric of an MTJ



Perpendicular (p) MTJ

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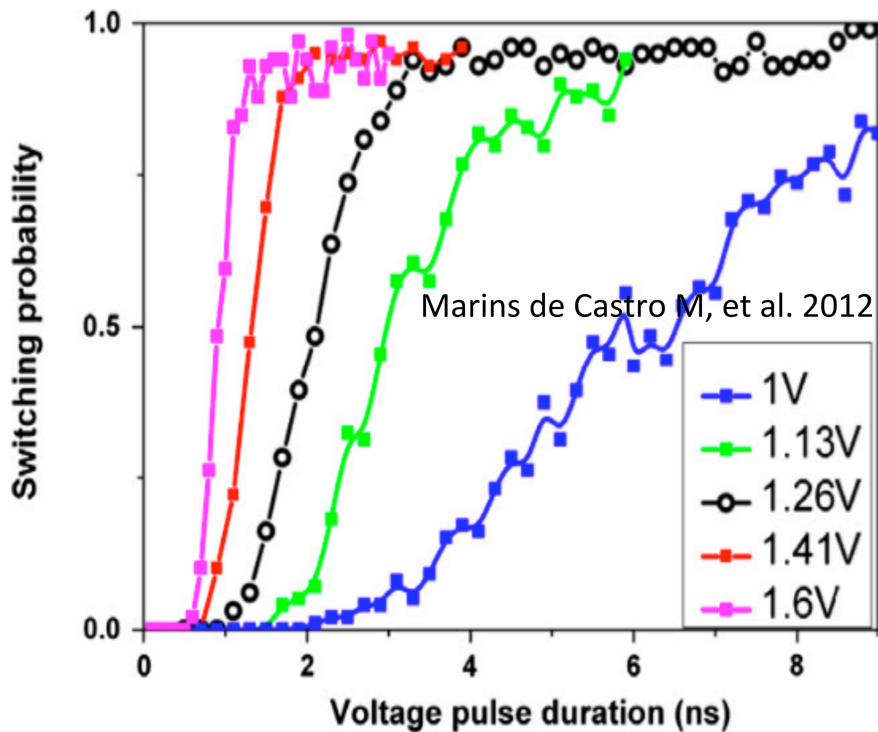
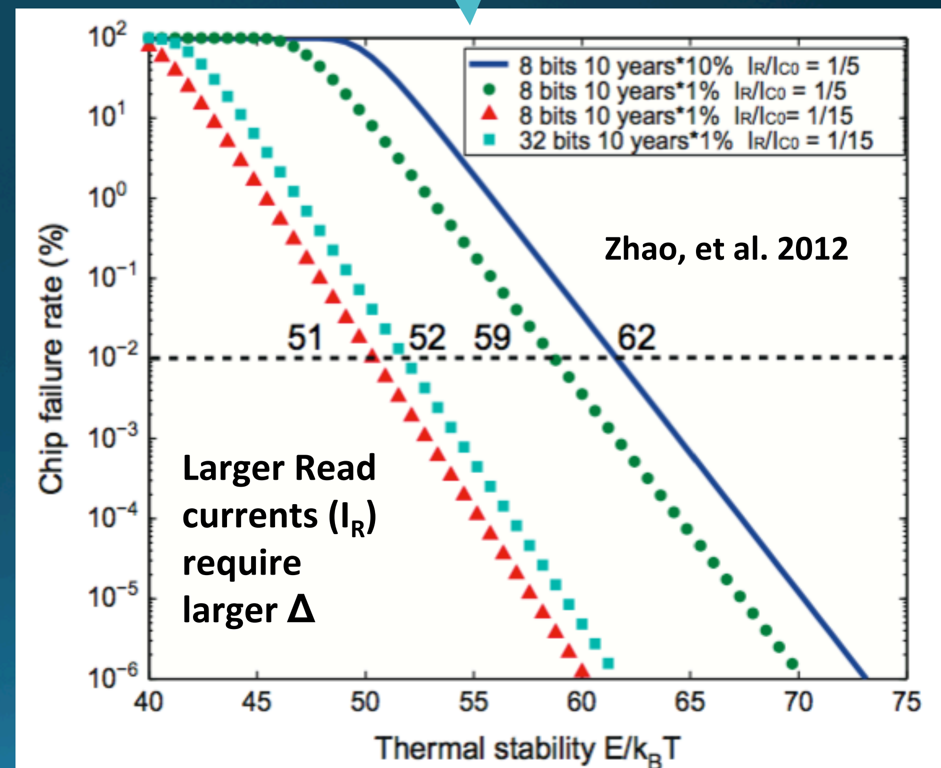


STT stochastic switching behavior

- Increasing the write current value I_{WR} or driver pulse duration are the most efficient methods to avoid the writing failures
- But lead to significant power, speed, surface overhead storage, and could drive the breakdown or damage of oxide barrier

High thermal stability factor (Δ) is required to reduce the erroneous sensing rate

$$F_{chip} = 1 - \exp\left[-N\frac{\tau}{\tau_0}\exp\left(-\Delta\left(1-\frac{I_R}{I_{CO}}\right)\right)\right]$$



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1 Gbit STT-RAMs may be available

- **Everspin is sampling 256 Mbit STT-RAM (p-MTJ) at 40 nm node and DDR interface and 100,000 X faster write time than NNAD**
- **Everspin 1 Gbit STT-RAM (28 nm) kit due by the end of the year!**
- **Avalanche Technology offers 32Mb SPSRAM™, which is a Quad SPI Non Volatile SRAM (pMTJ)**
- **Several companies offer embedded MRAM (40 nm and 28 nm)**

IBM publishes a paper claiming 11 nm STT-RAM with write error rates of 7 X 10^{-10} at 10 ns with a write current of 7.5 µA corresponding to low switching energy below 100 fJ (June 2016)

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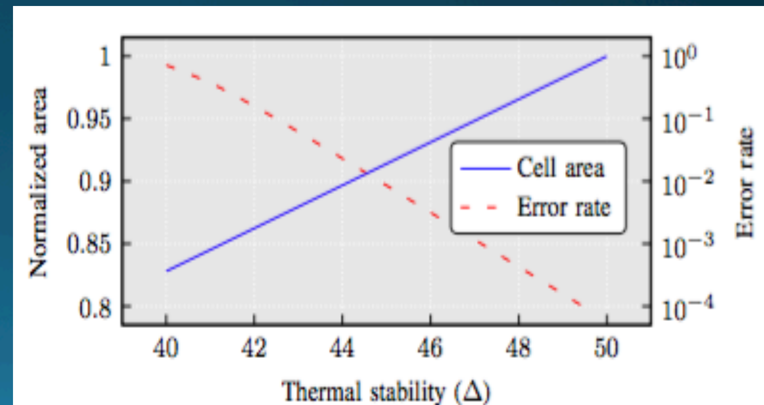
Can STT-RAM replace SRAM and DRAM?

	SRAM	DRAM	STT-RAM
Type	Volatile	Volatile	Non-Volatile?
Scalability	<20 nm?	<1x nm?	11 nm*
Cell Size (F^2)	120~200	4~6	15~50
Multi-level	No	No	Yes*
Read Speed	Very fast	Fast	Fast
Read Energy	Low	Medium	Medium
Write Speed	Very fast	Slow	Slow
Write Energy	Low	Medium	High
Leakage	High	Medium	Low
Endurance	10^{16}	10^{16}	$>10^{12}$
Refresh Power	NA	High	Medium?

*IBM (2016) R&D stage

- Relax retention time to scale STT-RAM and lower write energy
- STT-RAM errors are stochastic
- DRAM has deterministic errors
- DRAM-like refresh cannot be used in STT-RAM (bit could flip)
- In STT-RAM refresh operation must be accompanied by ECC



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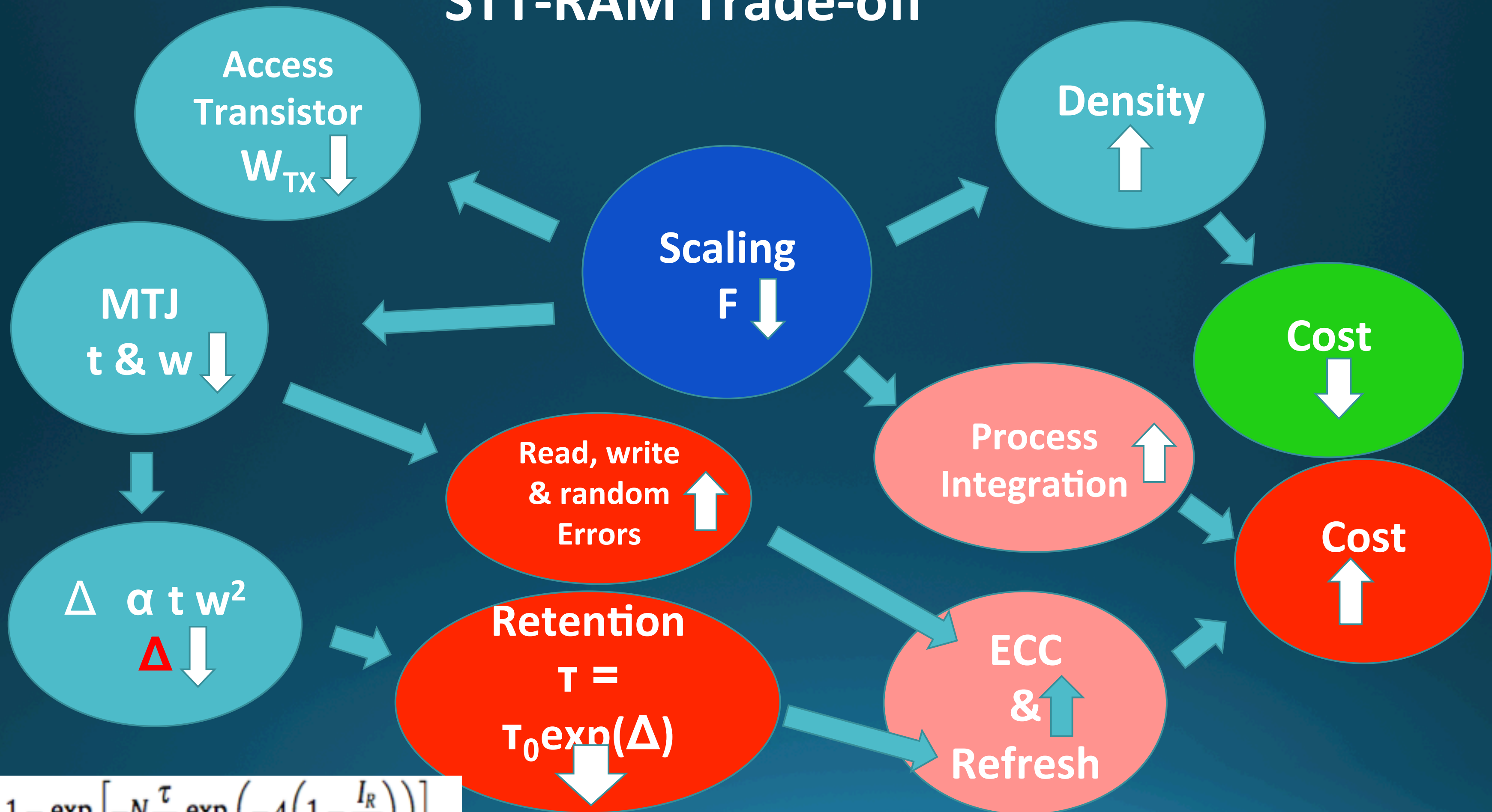
STT-RAM Trade-off
Access Transistor W_{TX}
Density
Scaling F
MTJ t & w
Cost
Process Integration
Read, write & random Errors
Cost
Δ α t w²
Δ
Retention τ = $\tau_0 \exp(\Delta)$
ECC & Refresh
$$F_{chip} = 1 - \exp\left[-N\frac{\tau}{\tau_0}\exp\left(-\Delta\left(1-\frac{I_R}{I_{CO}}\right)\right)\right]$$
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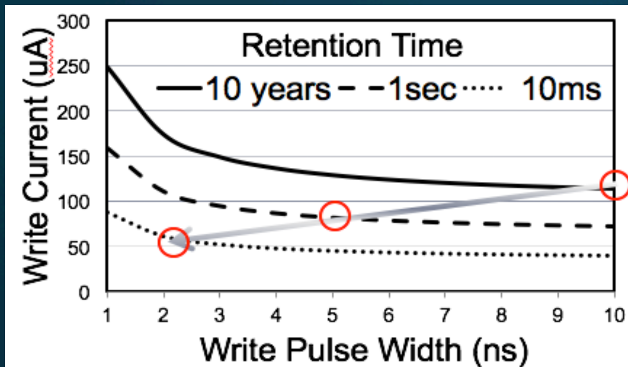
Most Important Metrics for STT-RAM



Cost???
(Memory Array? + Control Circuit??)

Scalability and Density
(Memory cell + selector)

Device Performance

- **Latency:** Write energy issues
- **Endurance:** Tradeoff with write energy
- **Retention:** High density may be volatile
- **Reliability:** Soft and Hard errors

2D	3D
40 nm-now 28 nm (1-2Y) 11 nm (Research)	Significant Challenges

Variability of oxide barrier thickness will lead to hard errors, as the resistance is exponential to the thickness

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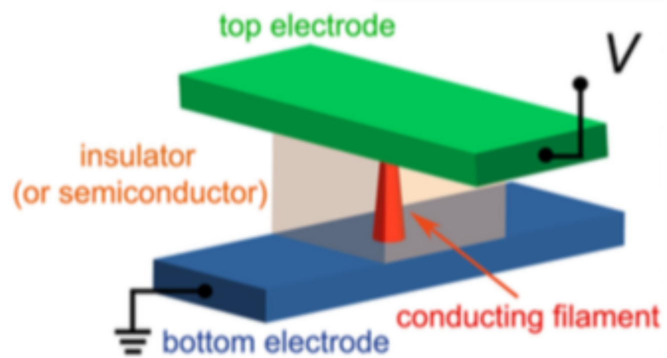
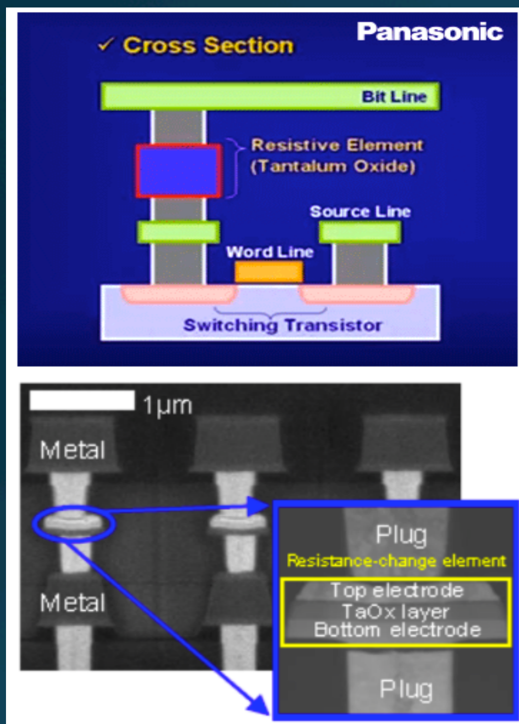


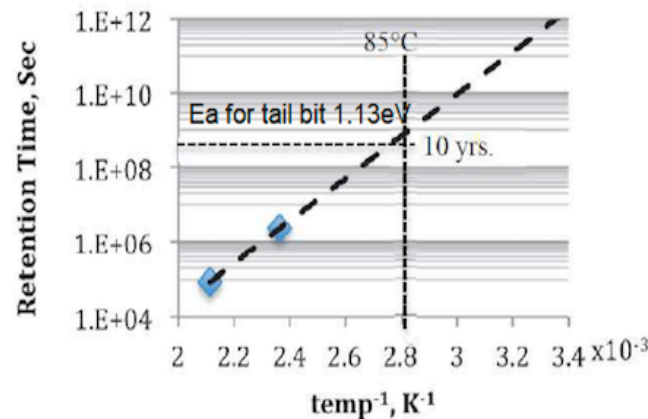
Filament ReRAM

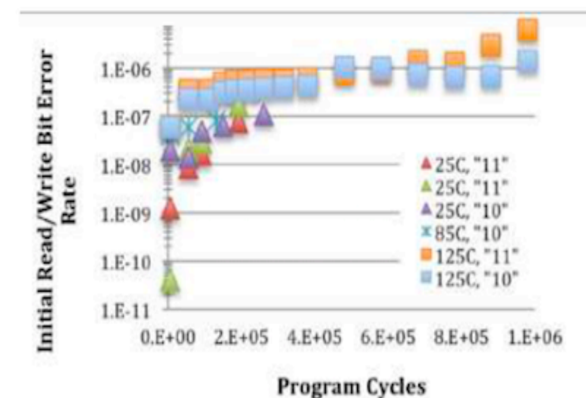
Oxy-ReRAM **CBRAM**

Panasonic MN101L, 64 kbytes Oxy-ReRAM (1T-1R) Embedded 8-bit MCUs



- 180 nm CMOS process with low leakage current
- 50% lower power consumption, and over 5 times faster rewriting than flash memory or EEPROM



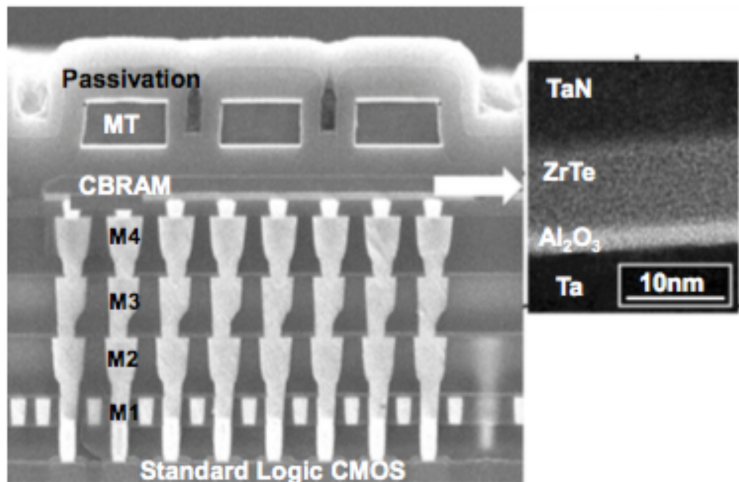


SET/RESET ~2.5V, 100ns
Verify ratio ~1.2
Vread~0.5V

J.Y.Scharlotta,IIRW 2014

*2Mbit ReRAM test memory array, claims 100K endurance cycling and 10 years of memory retention at 85°C at 28 nm node (Panasonic & IMEC, paper, 2015)

Adesto 512 Kbit EEPROM-compatible CBRAM



Parameter	Adesto Moneta	Standard EEPROM
Core Supply Voltage	0.97–1.03V	Not Applicable
I/O Supply Voltage	1.65–2.75V	Not Applicable
Single Supply Voltage	Not Applicable	1.7–5.5V
Read Power (500Kb/s)	10μW	1250μW
Lowest Power-Down Mode	.05μW	.25μW
Clock Frequency (Max)	1MHz	20MHz
Operating Temp Range	–40 to +85°C	–40 to +85°C
Write Supply Voltage	3.6–4.4V	1.7–5.5V
Write Power (10Kb/s)	7.5μW	375μW

- Single supply voltage: 1.65V - 3.6V
- 1.6 MHz maximum clock rate for normal read
- 20 MHz maximum clock rate for fast read
- Byte Write consuming 50 nJ
- 0.25 mA Read current; 1 mA Write current
- Byte Write within 25 μs
- Data Retention: 10 years
- Endurance: 10,000 Write Cycles
- Unlimited Read Cycles

Te---Metalloid Filament!!

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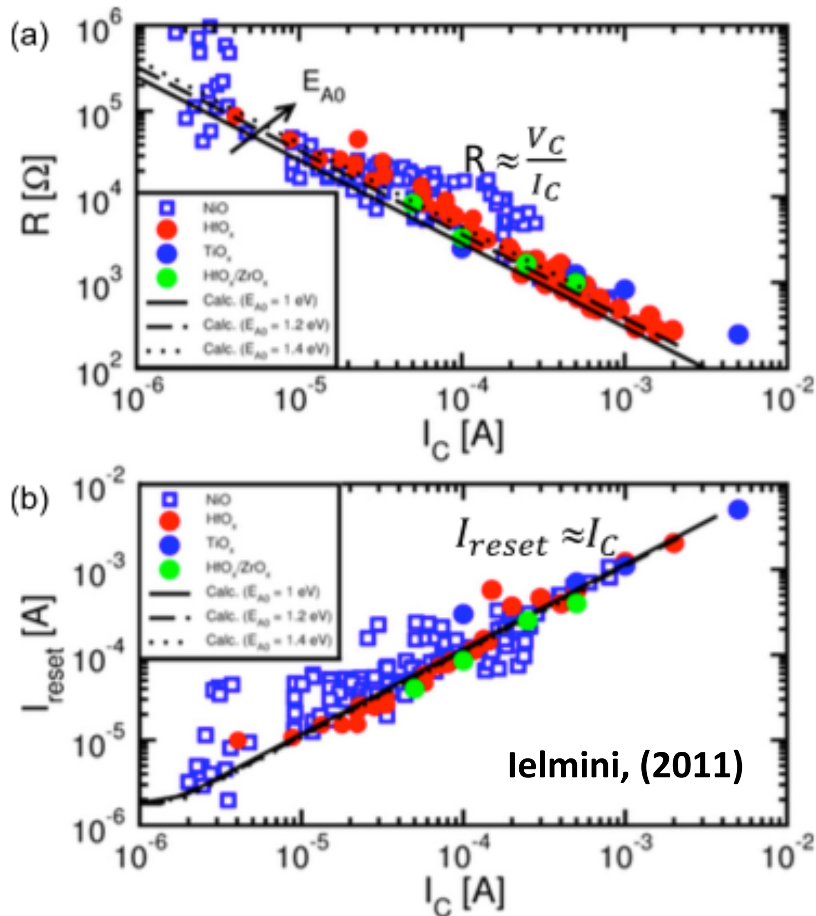
Universal Characteristics of Filament ReRAM



- **The measured and calculated LRS Resistance (a) and I_{reset} (b) as a function of compliance current (I_C).**
- **I_C controls the Conducting Filament size and resistance**
- **Negligible dependence on the switching mode (unipolar, bipolar) and stack composition or structure.**

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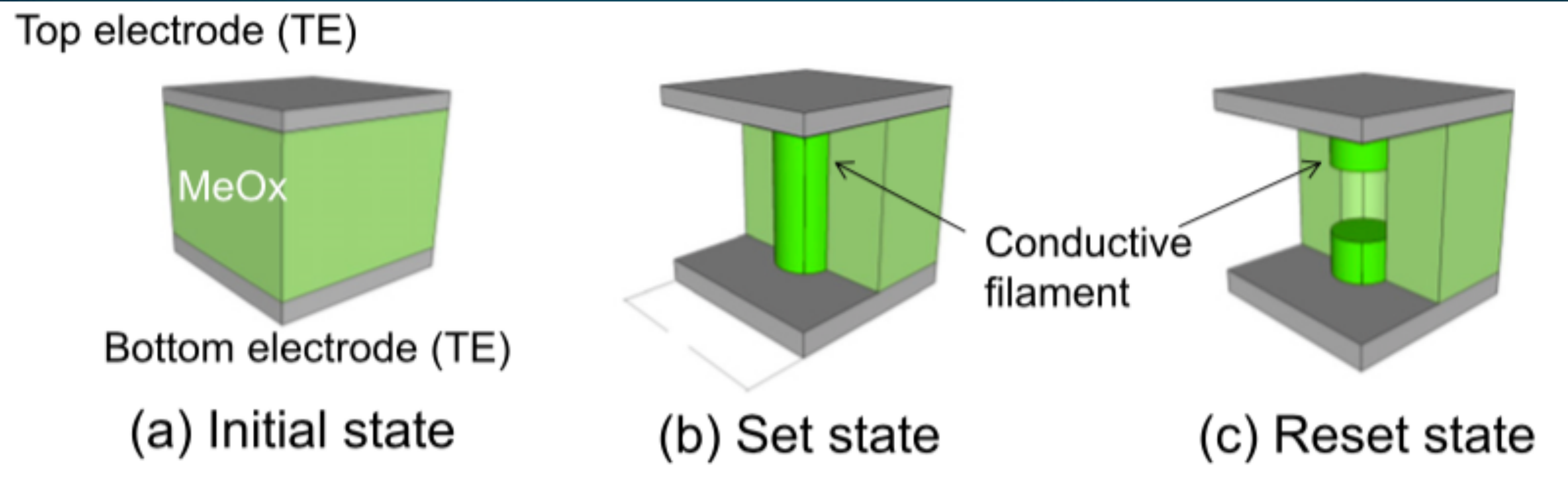
In addition to the process variations, Filament formation, rupture and regrowth are stochastic processes!!



- Local high fields can change due to change in nature of defects and their concentrations (> 1 MV/cm)
- Local power dissipation can alter the local temperatures (~ 1 TW/cm^3)
- Local electronic current densities can vary (> 10^6 A/cm^2)
- Significant local variations in ionic current densities

Verify & ECC

Extensive optimization needed to engineer the tail bits

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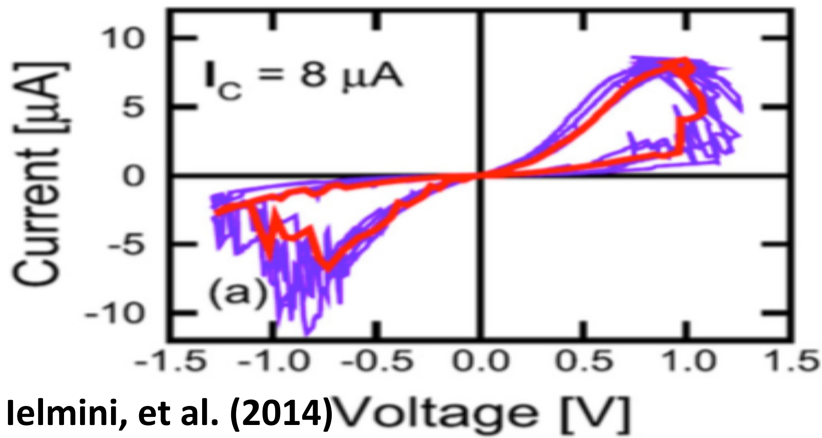
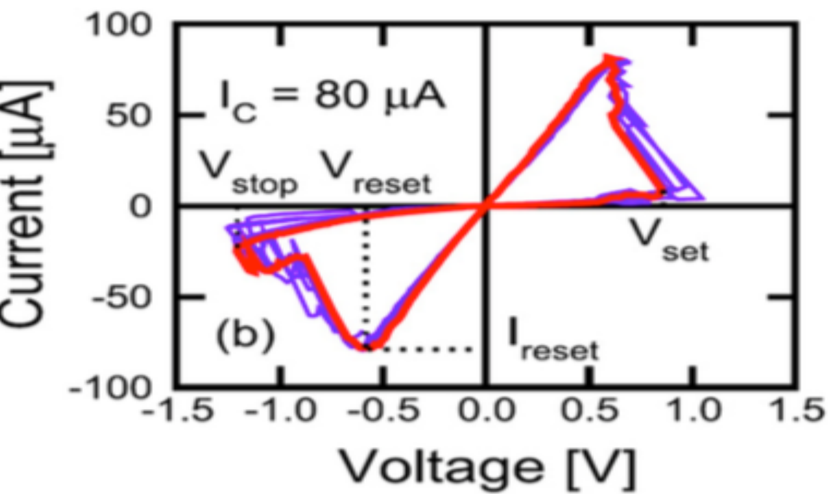
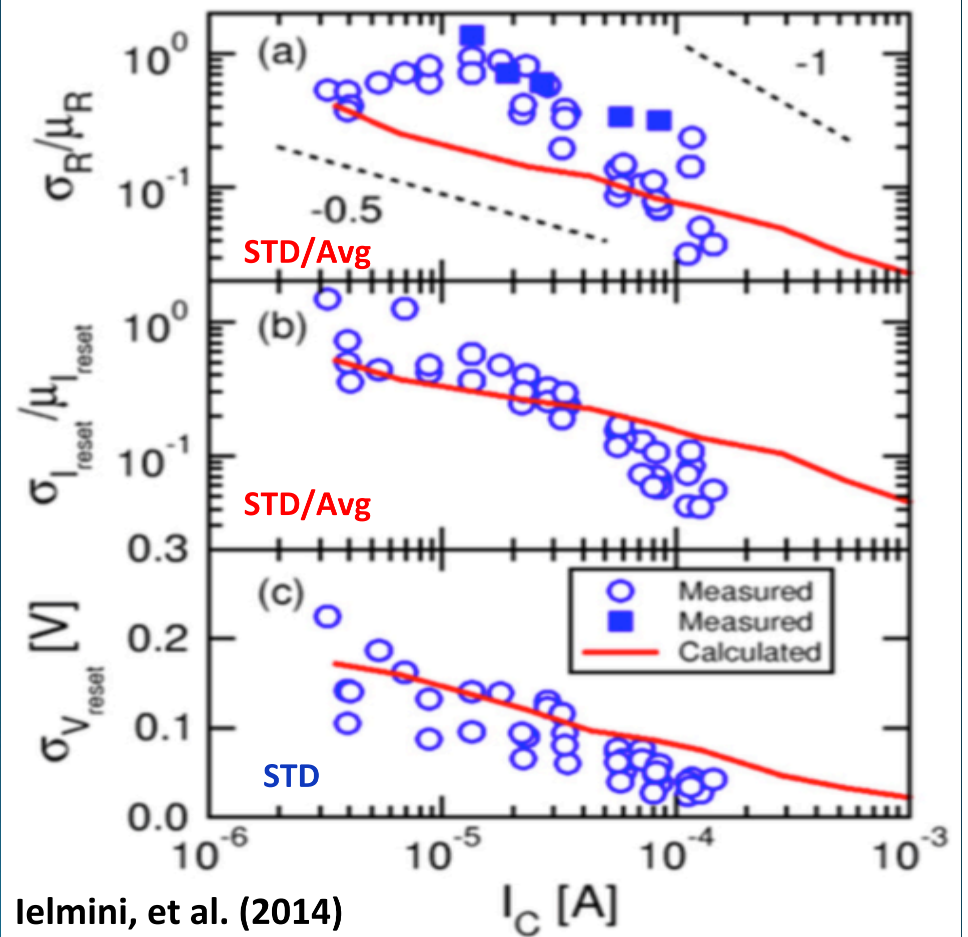


Ielmini, et al. (2014)





Ielmini, et al. (2014)

Variability of switching in HfO2 ReRAM Indicating the stochastic nature of CF

The cycling variability of switching parameters in HfO2 ReRAM devices

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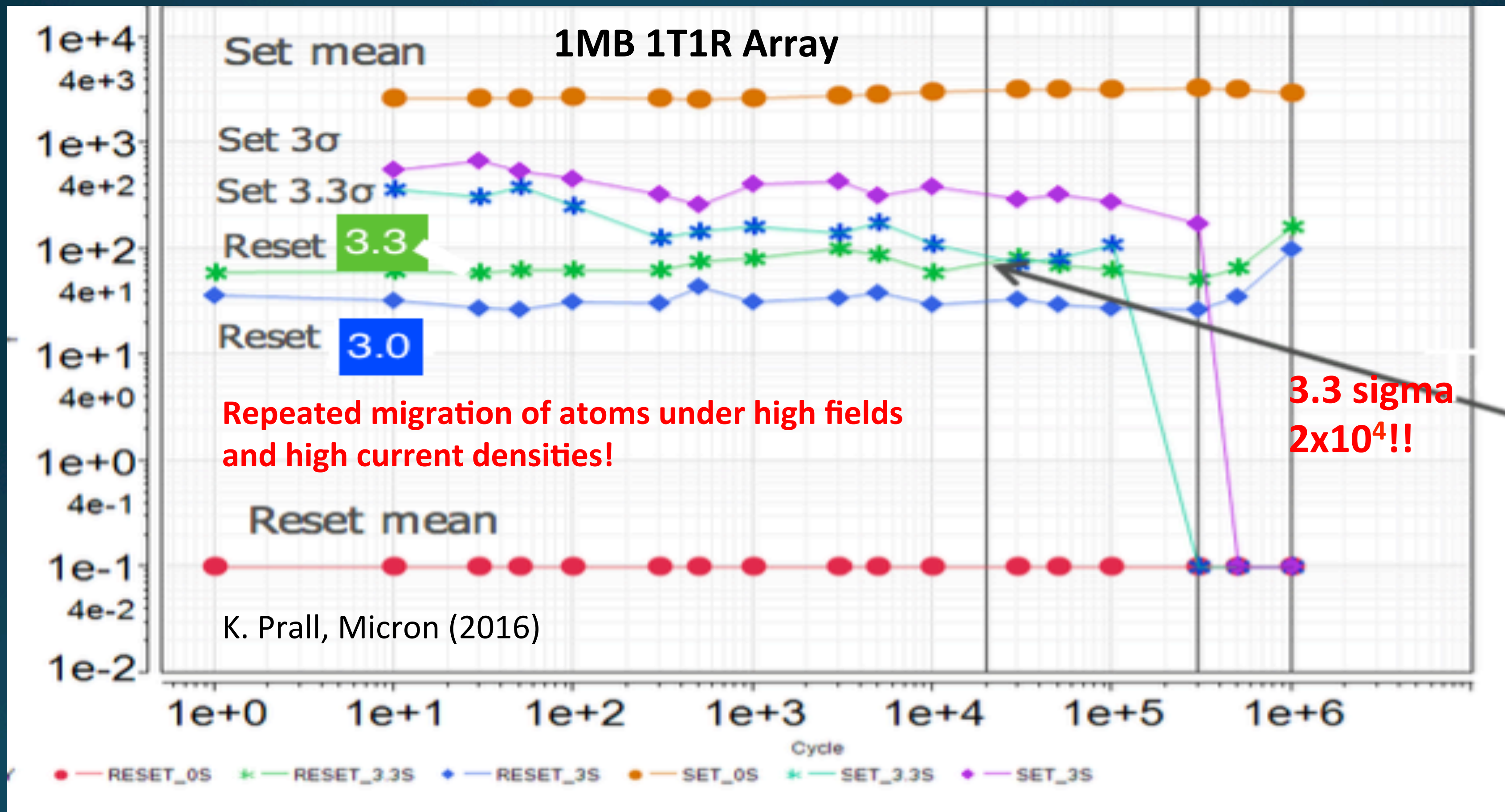
Defect tails determine the Endurance

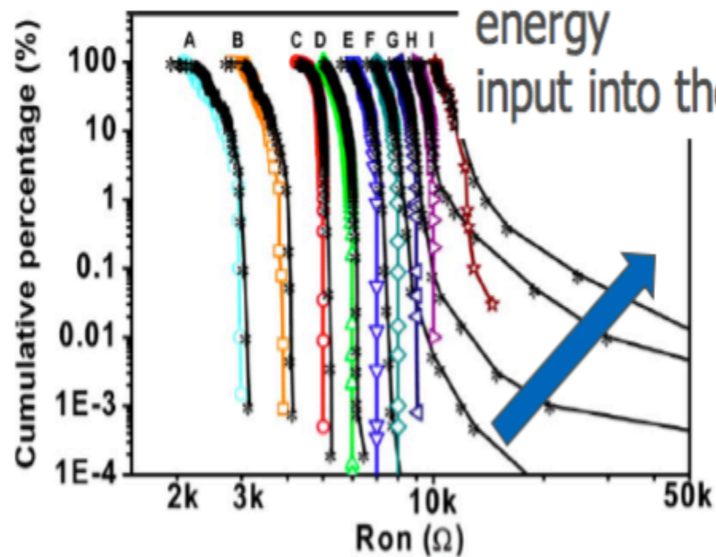


Retention is a strong function of SET energy!

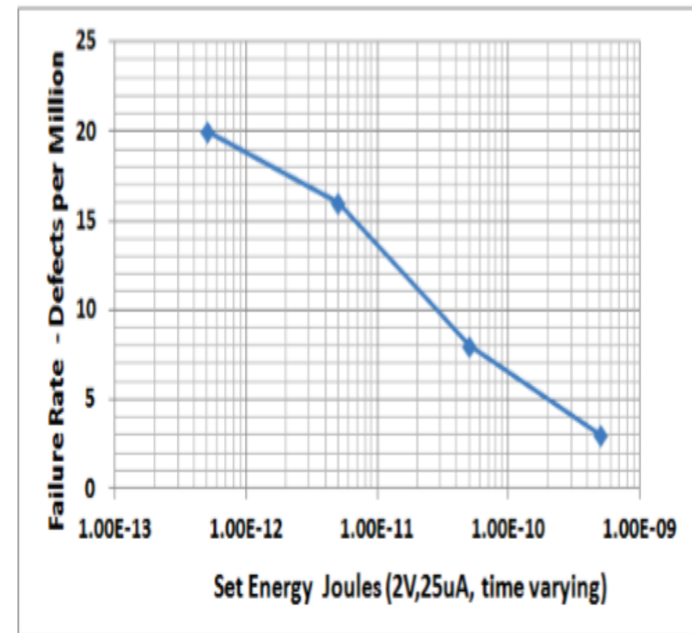
Cu RRAM Example

K. Prall, Micron (2016)

Retention defect tail grows with less energy input into the cell



RRAM Retention vs. R for 1000hr 150C Bake



Bit Failure Rate vs. Set Energy for a 150C 1000 Hour Bake

Higher the input SET energy the lower the SET resistance

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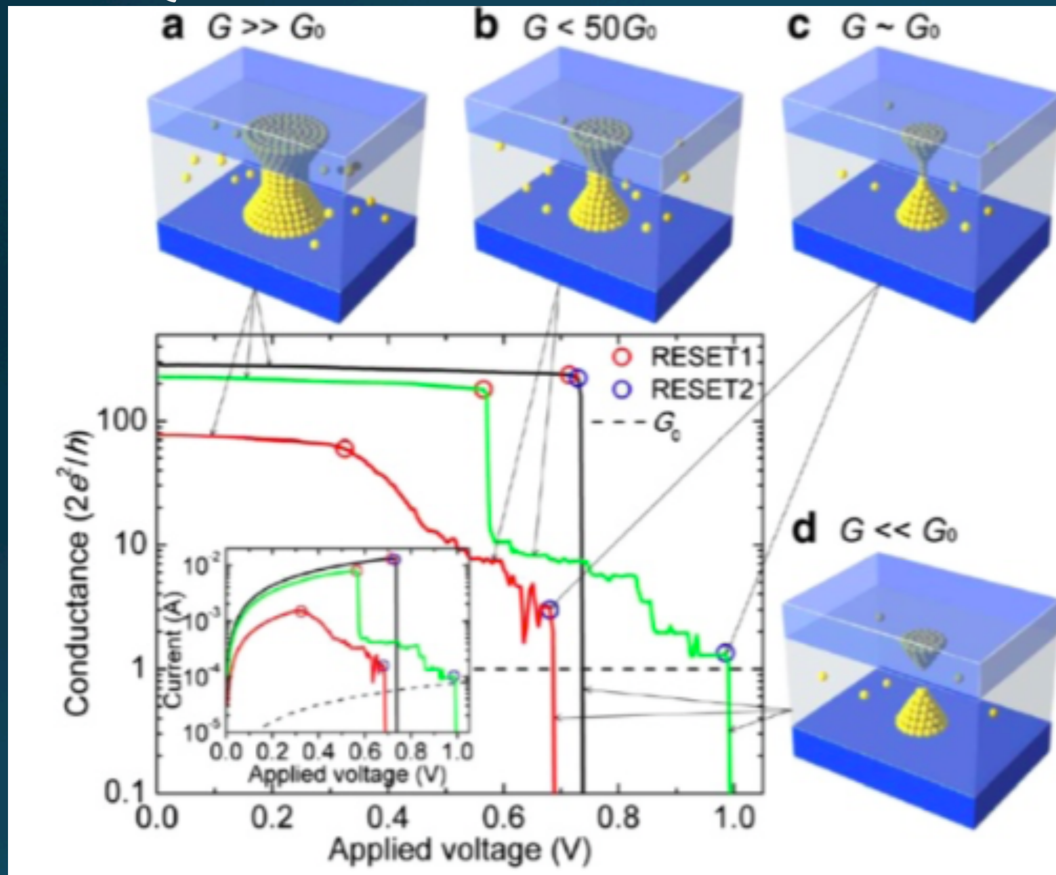
Quantization of Filament Resistance!



- When the electron mean free path is close to the diameter of the CF, ballistic transport is possible
- Conductance of CF is quantized
- $G_0 = 2\ e^2/h$ (R_0 = 12.9 k Ohms)
- 76 µA at 1V
- Independent of the nature of the filament and material composition!
- Would MLC possible??
- What about the statistical variability of CF with small dimensions?

Long, et al., (2013); Pt/HfO2/Pt RESET Process

Most Important Metrics for Filament ReRAMs

Cost??

(Memory Array + Control Circuit??)

*High Density

High bit error rates

Scalability and Density

*Memory cell can be scaled**

Selector scaling??

Device Performance

- **Latency:** Higher write energy?
- **Endurance:** Tail Bits?
- **Retention:** Tradeoff with SET Energy
- **Reliability:** Soft errors and Noise

2D
Low density

3D
- Vertical: Selector?
- Horizontal:Cost?

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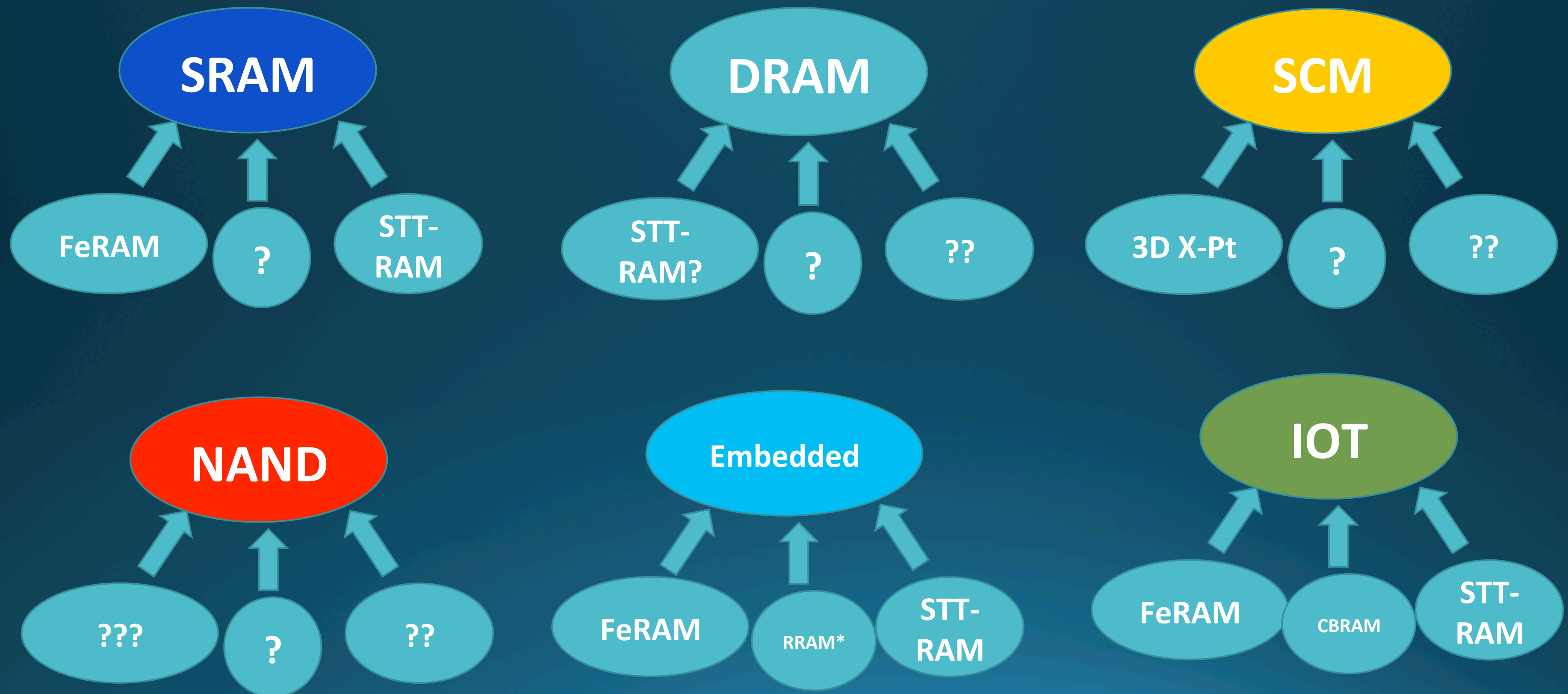
Emerging Memories: Are they Emerging?
SRAM
FeRAM
?
STT-RAM
DRAM
STT-RAM?
?
??
SCM
3D X-Pt
?
??
NAND
???
?
??
Embedded
FeRAM
RRAM*
STT-RAM
IOT
FeRAM
CBRAM
STT-RAM
* Filament RRAM
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Thanks

Questions and/or Comments