Management Schemes of Hybrid SSDs with SLC/MLC Flash Memory: A Survey

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Flash Memory SUMMIT Outlines

- Introduction and Background
  - Advantages of SSD over HDD
  - SSD Architecture
  - Flash Translation Layer (FTL)
    - Address Translation - Garbage Collection (GC) - Wear Leveling (WL)
  - Comparison Between SLC, MLC and TLC
- Hybrid SSD Schemes
  - Schemes using SLC as a buffer (SLC-Buf)
  - Schemes Using Both SLC and MLC as a Buffer (SLC/MLC-Buf)
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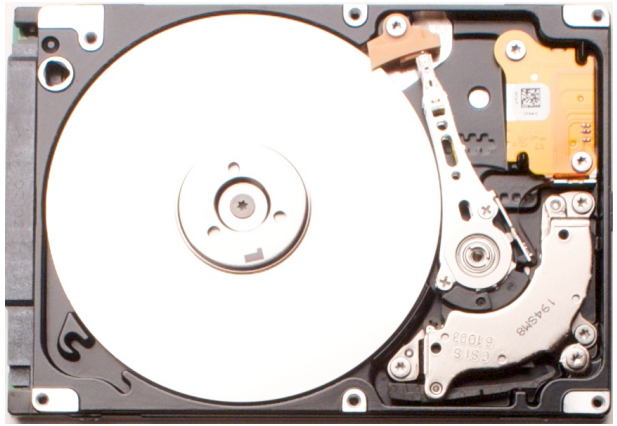
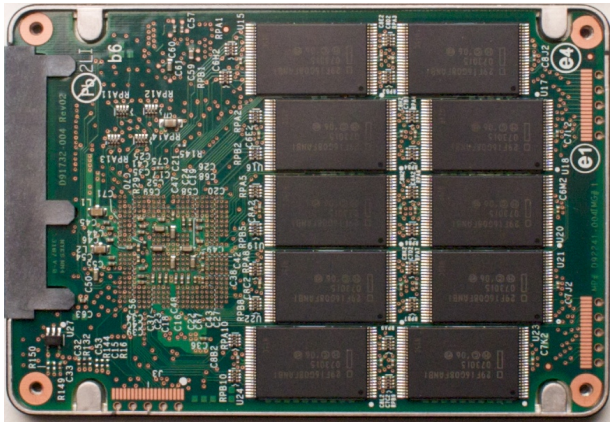
  - Schemes without a Buffer (No-Buf)
- Conclusion and Possible Future Directions

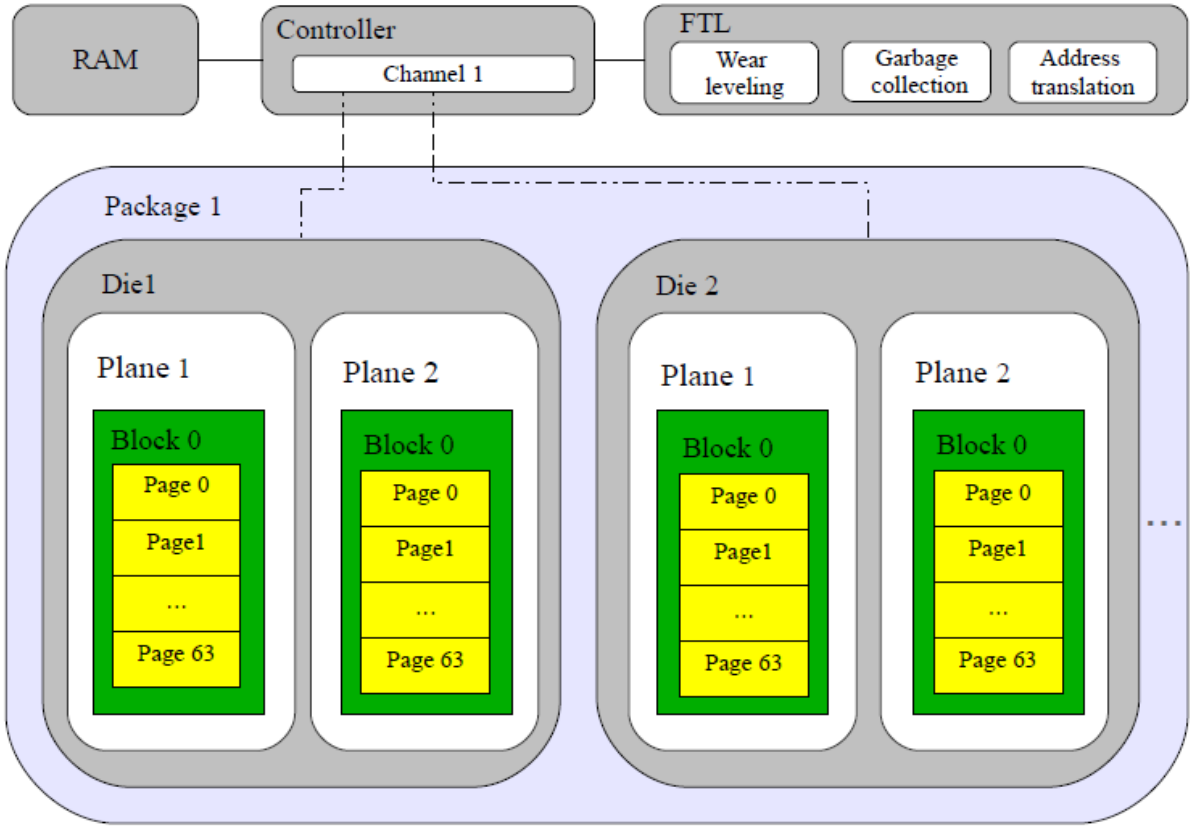
Advantages of SSD over HDD

- Low power consumption
- Higher flexibility to external shock
- High random access performance

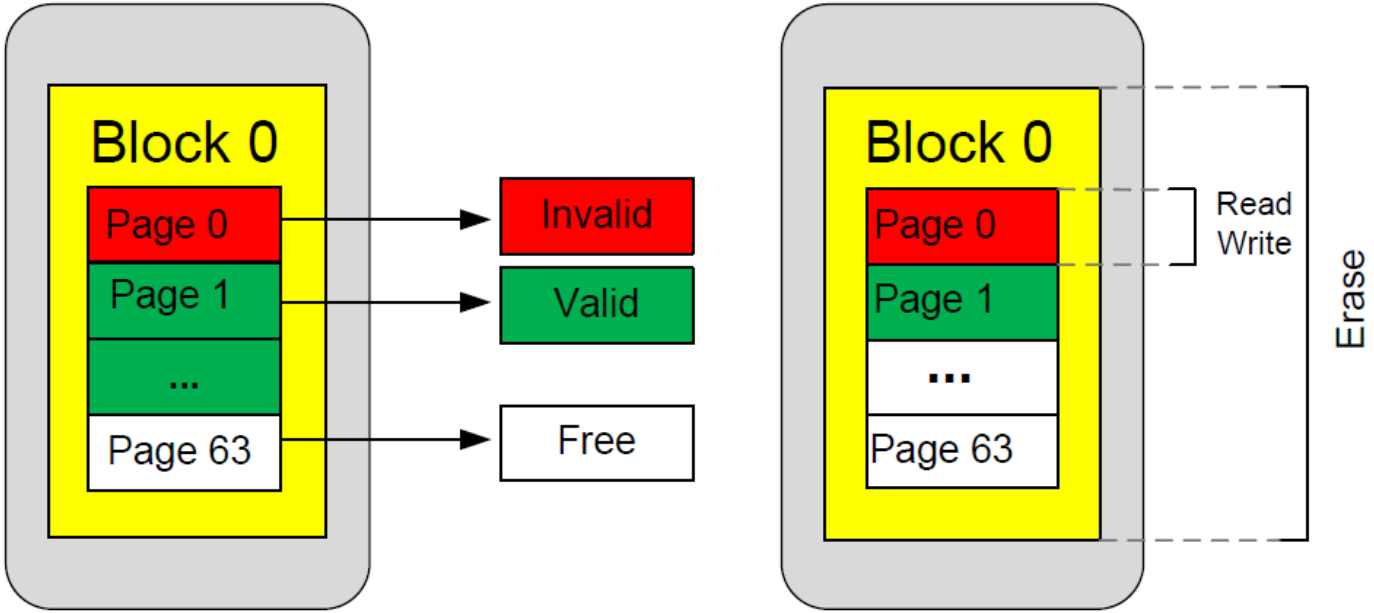




A typical SSD Architecture

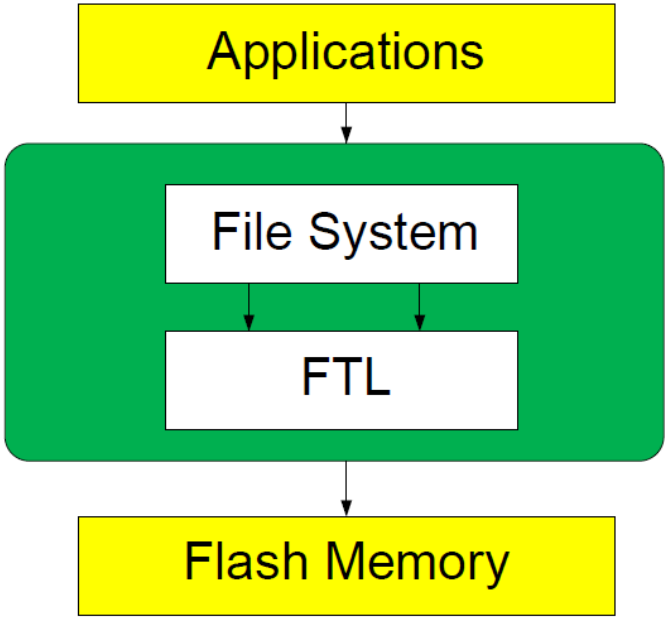


A typical SSD Architecture

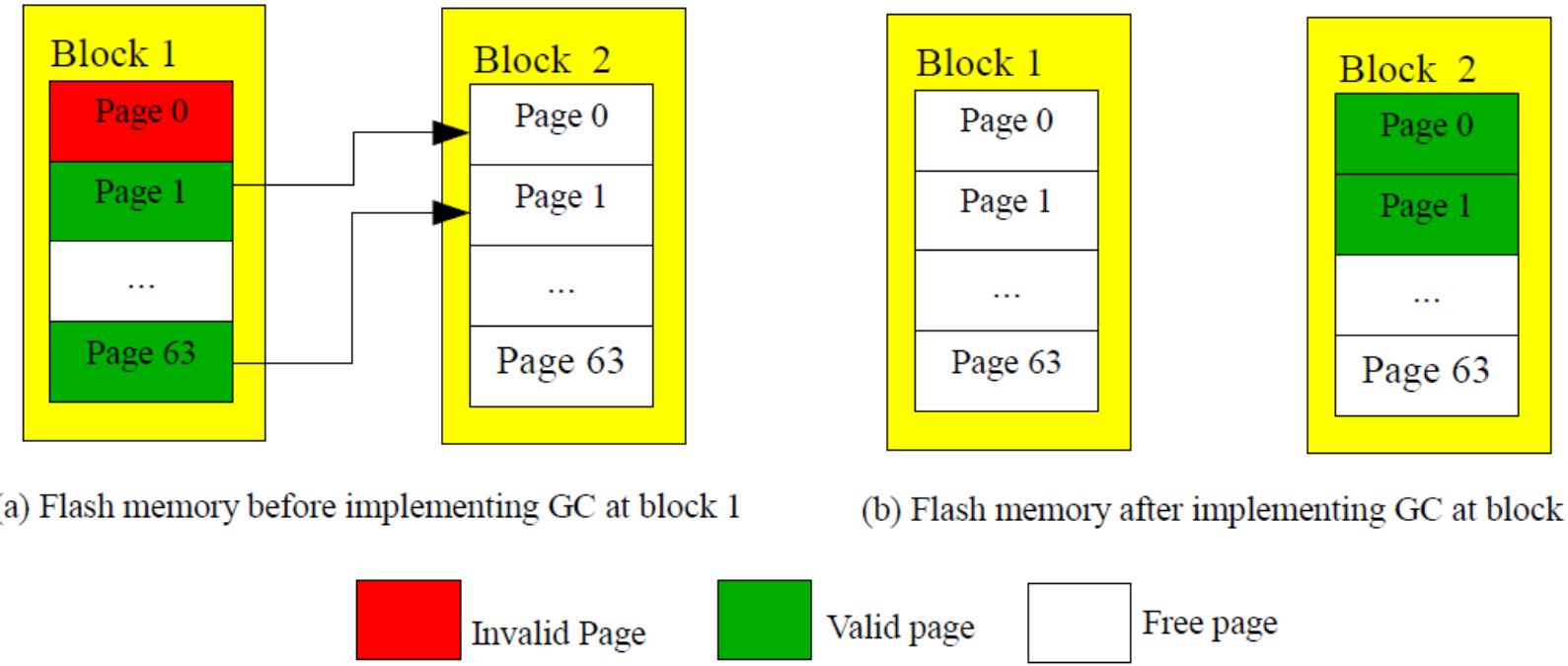


Flash Translation Layer (FTL)

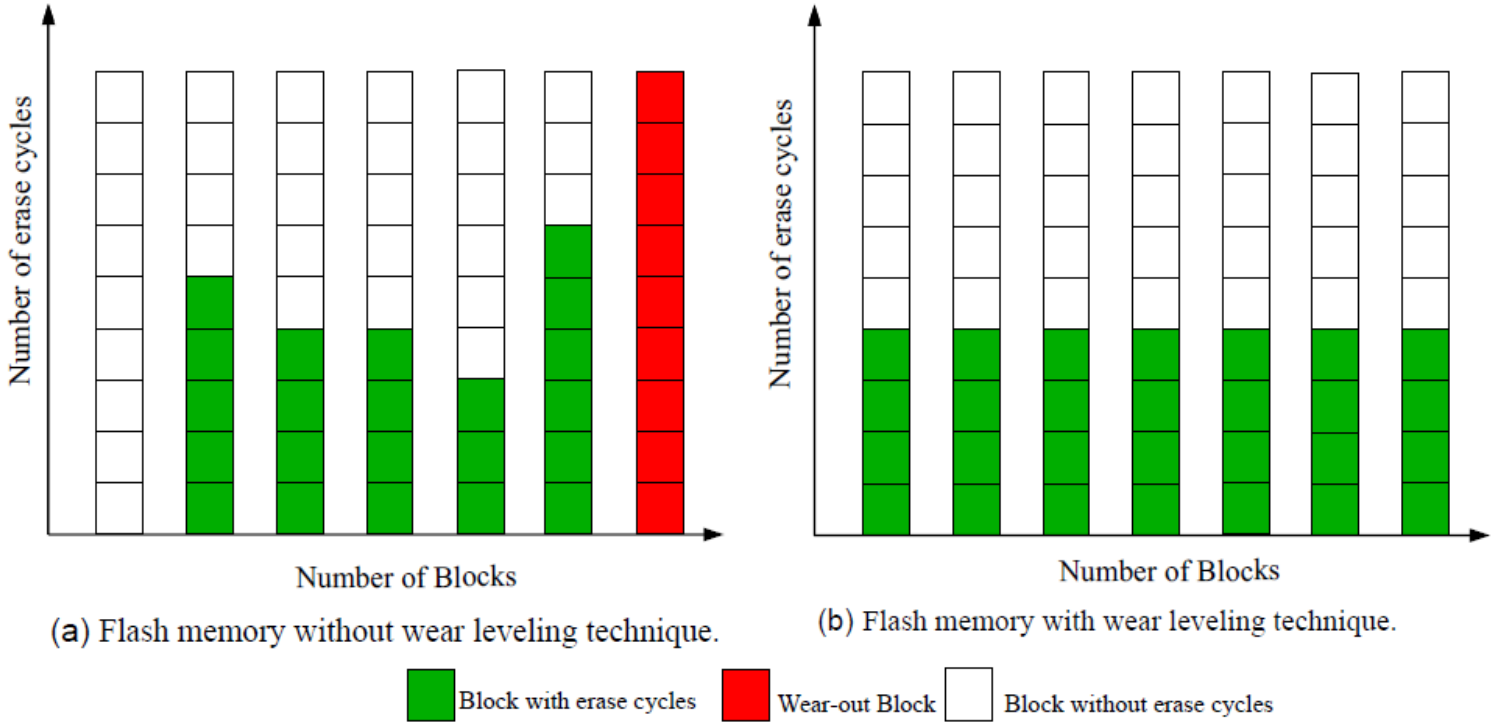
- FTL typically provide three software components:
  - Address Translation
  - Garbage Collection (GC)
  - Wear Leveling (WL)



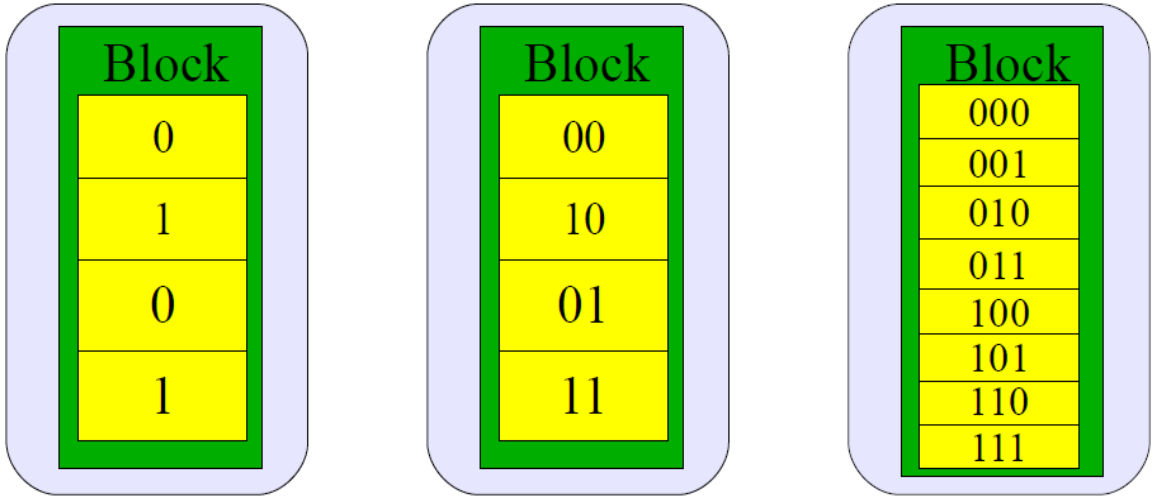
Garbage Collection



Wear Leveling



Comparison Between SLC, MLC and TLC



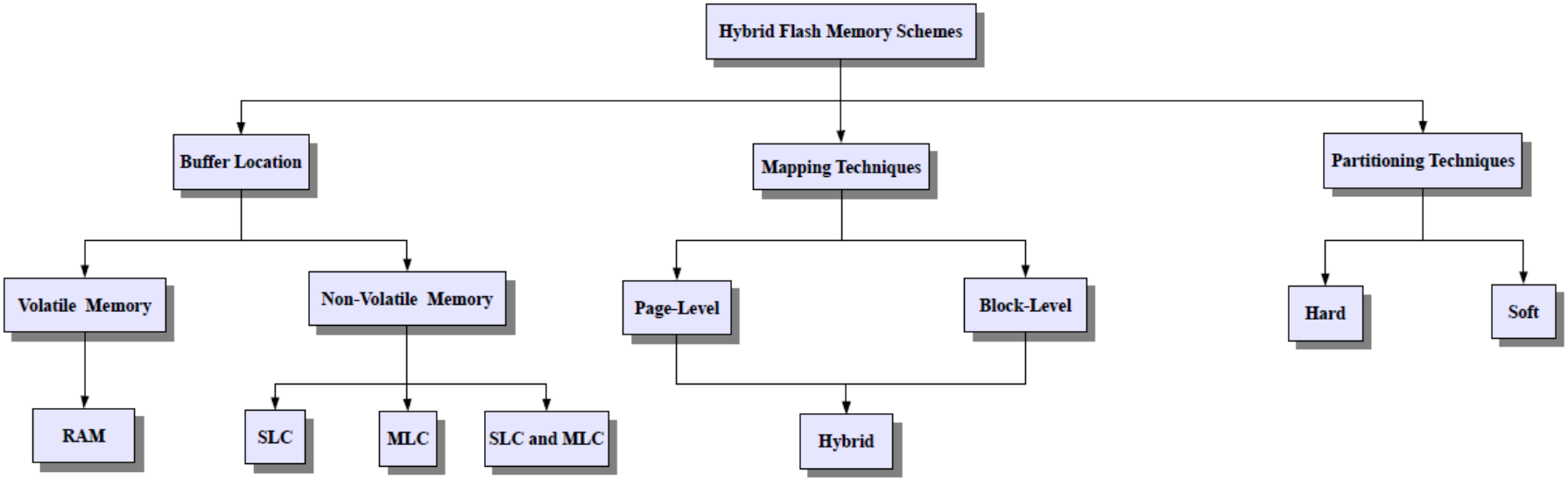
(a) SLC (b) MLC (c) TLC

Comparison Between SLC, MLC and TLC

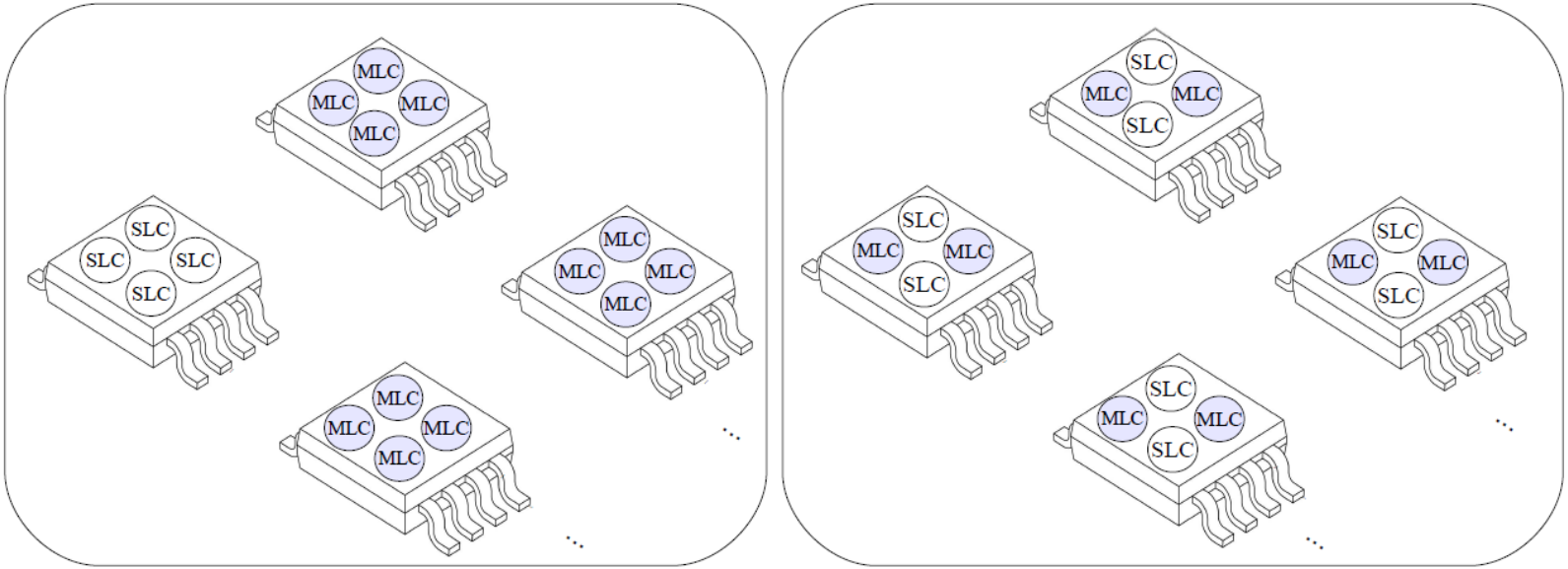
(Dong and Xie 2011)
(Hsieh et al. 2015)

Features	SLC	MLC	TLC
Density	Low	High	Very high
Cost per bit	High	Low	Very low
Page size	2K bytes	4K bytes	16K bytes
Block size	128K bytes	512K bytes	1.5M bytes
Page read	20 μs	50 μs	100 μs
Page write	350 μs	900 μs	2400 μs
Block erase	1500 μs	2000 μs	3000 μs
W/E Cycles	100,000	10,000	$<$ 1,000
Electrical Voltage	3.3V	3.3V	3.3V
Electrical Current	15 mA	15 mA	15 mA
Price (USD/GB)	4.92	1.7	0.63

Organizations of Hybrid SSD Schemes



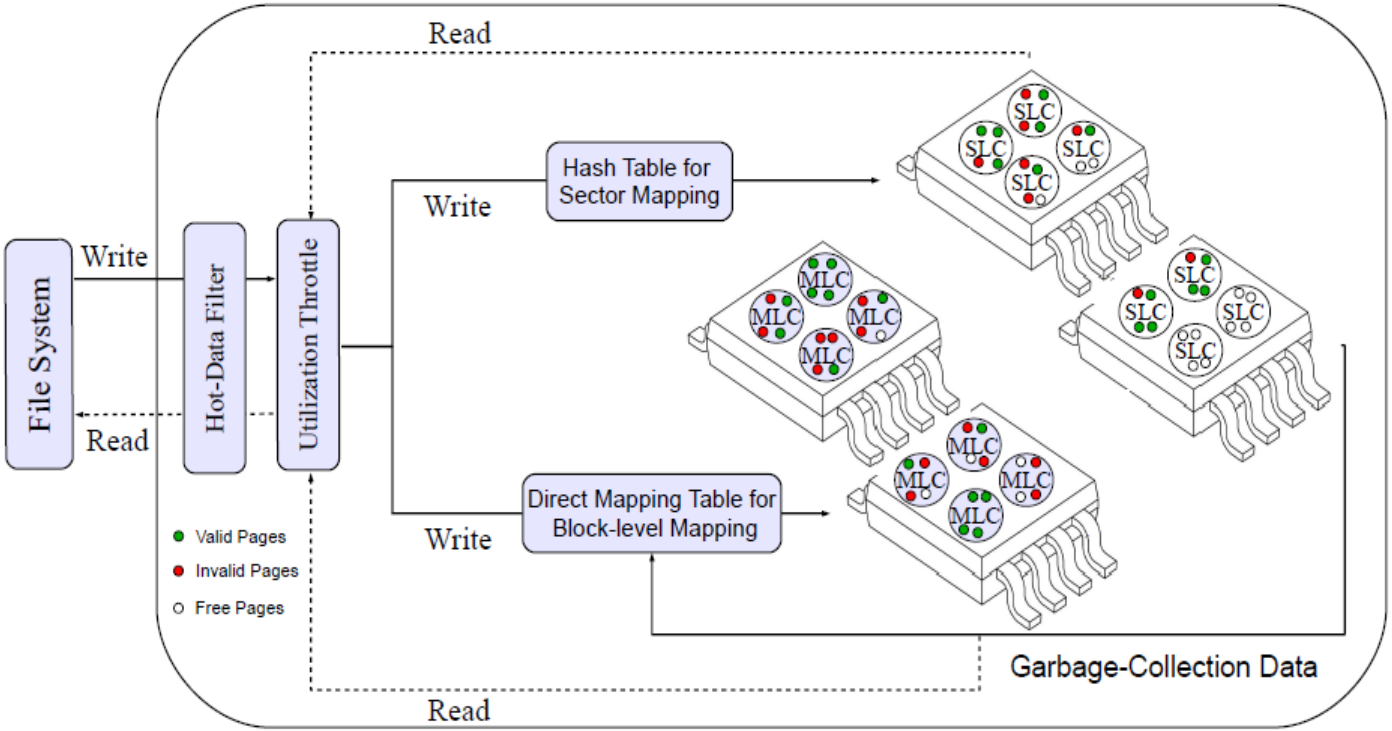
Hard vs. soft partitioning



Schemes using SLC as a buffer (SLC-Buf)

Schemes	Basic Idea	Buffer Location	Mapping Technique — SLC	Mapping Technique — MLC	Partitioning
Chang (Chang, 2008)	Passing the hot data to SLC and cold data in MLC. The small write request should be manipulated by SLC.	SLC	Page-Level	Block-Level	Hard
Hierarchical FAST-MS (Jung and Song, 2009)	Passing the write data to a non-volatile buffer, which located at SLC portion, to avoid performing write and erase operation at MLC.	SLC	Log-Based Hybrid	Log-Based Hybrid	Hard
Bypassing (Im and Shin, 2009)	Using the SLC as a log buffer and the MLC as a data block.	SLC	Page Level	Block Level	Hard
Combo FTL (Im and Shin, 2010)	Using small size of SLC for hot data and large size of MLC for cold data.	SLC	Page Level	Block-level	Hard
Hybrid Scheme (Nam et al., 2010)	Using small size of SLC for hot data and large size of MLC for cold data.	SLC	Page-level	Block-level	Hard

Architecture of hybrid storage combined SLC/MLC flash memory for Chang's scheme) Chang 2010(



Advantages and Disadvantages of (SLC-Buf)

- Advantages

Increasing the performance of SSD in terms of speed.

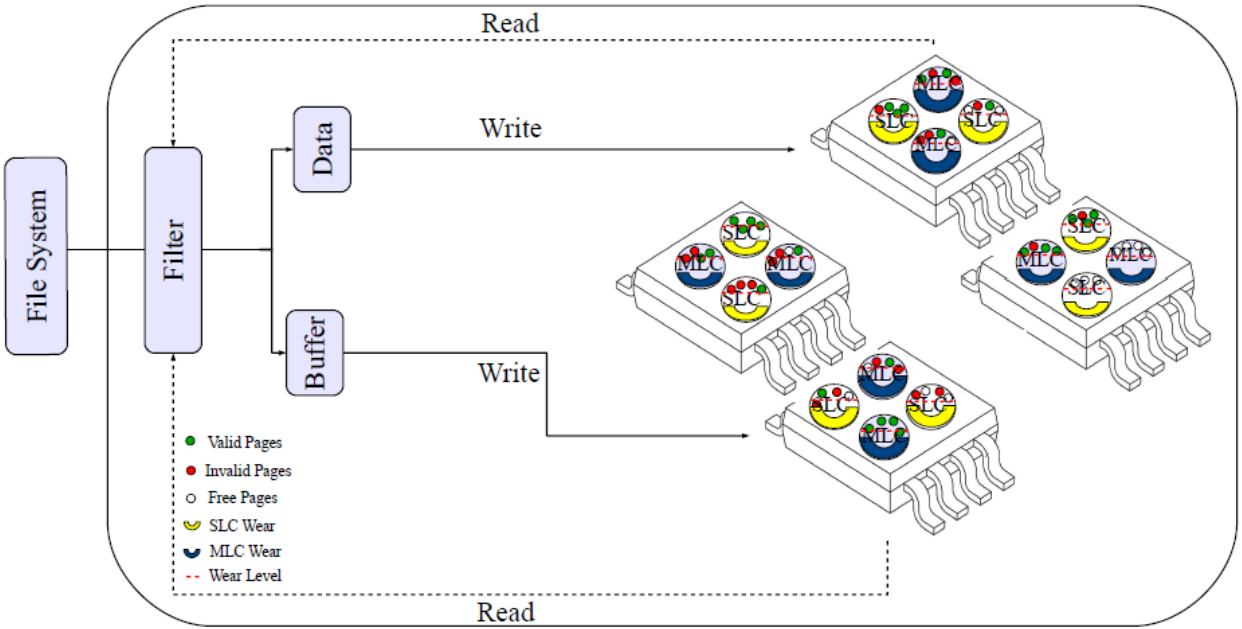
- Disadvantages

Using small size of SLC as a buffer to serve the hot data, thus the SLC portion will wear out quickly and that will affect the overall reliability of SSD.

Schemes Using Both SLC and MLC as a Buffer (SLC/MLC-Buf)

Schemes	Basic Idea	Buffer Location	Mapping Technique		Partitioning
			SLC	MLC	
Soft Partitioning (Jimenez et al., 2012)	Using soft partitioning technique to move the physical location of the buffer either to SLC or to MLC based on their wears.	SLC and MLC	Hybrid FTLs	Hybrid FTLs	Soft
Phoenix (Jimenez et al., 2013)	Reusing the MLC blocks that have been worn out as SLC blocks. Using the fact that MLC blocks become unreliable can still reliably be used to store a single bit per cell.	SLC and MLC	-	-	Soft
FlexFS (Lee and Kim, 2014)	Taking a benefit from flexible programming provided by MLC to provide ability for each cell to be programmed as SLC or MLC mode.	SLC and MLC	-	-	Soft
RR-FDCA (Hachiya et al., 2014)	Taking a benefit of TLC and adding it to hierarchy of hybrid SSD in order to decrease the cost.	MLC	-	-	Hard

Architecture of hybrid storage combined SLC/MLC flash memory for soft partitioning scheme (Jimenez et al. 2012(



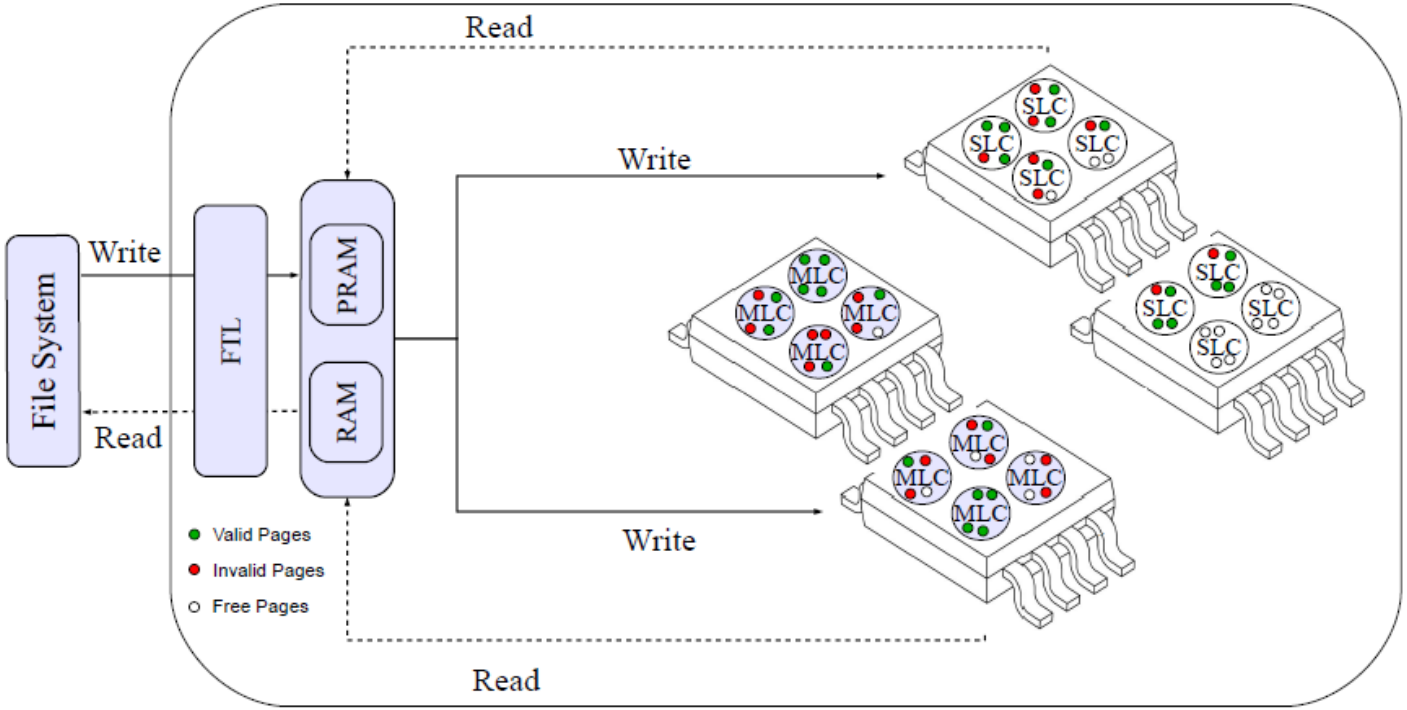
Advantages and Disadvantages of (SLC/MLC-Buf)

- Advantages
  - More reliable
  - More flexible
  - Cost efficient
- Disadvantages
  - More complex

Schemes Using External Memory as a Buffer (ExtM-Buf)

Schemes	Basic Idea	Buffer Location	Mapping Technique — SLC	Mapping Technique — MLC	Partitioning
Yim's scheme (Yim, 2005)	Using volatile RAMs and non-volatile RAMs as a write buffer, and using different types of flash memories in order to reduce the overall storage cost.	VRAM and NVRAM	-	-	Hard
HFTL (Park et al., 2011)	Managing both SLC and MLC connected to each others using parallel pattern. The short and long write request will passed to MLC and SLC respectively.	DRAM	Block Level	Page Level	Hard
PH-SSD (Lu et al., 2012)	Dividing the SSD to three categories: PRAM used as a primary updating area, SLC used as a secondary updating area, and MLC used as a main storage area.	PRAM	Page Level	Page Level	Hard
DABC-NV (Park et al., 2012)	Using two types of memory as buffer cache non-volatile RAM and volatile RAM.	VRAM and NVRAM	-	-	Hard

Architecture of hybrid storage combined SLC/MLC flash memory for Yim's scheme (Yim 2005)



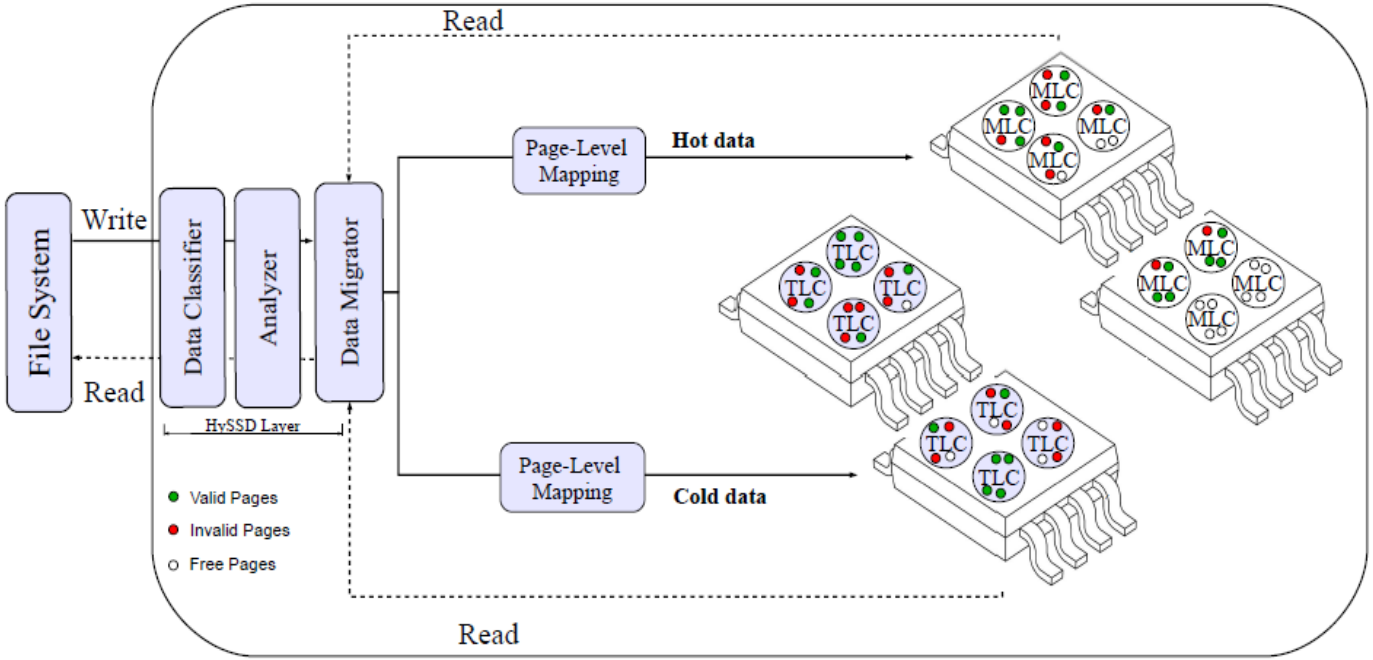
Advantages and Disadvantages of (ExtM-Buf)

- Advantages
  - High speed
- Disadvantages
  - High price
  - Losing data in case of power outage

Schemes without a Buffer (No-Buf)

Schemes	Basic Idea	Buffer Location	Mapping Technique — SLC	Mapping Technique — MLC	Partitioning
AFVM (Sung and Kim, 2012)	Exploiting the symmetry of SLC and MLC flash memory in their service time characteristics. The frequently writs operations with small size will be resided into SLC portion and the seldom writes operations with large size will be resided into MLC portion.	No Buffer	Device Mapper	Device Mapper	Soft
Hybrot (Murugan and Du, 2012)	Adapting the flow of hot data to the SLC and MLC regions in a systematic manner instead of using the SLC portion as a cache or log buffer for the MLC portion. .	No Buffer	Page Level	Block Level	Hard
AHDM (Batni and Safaei, 2014)	dividing the data to hot and warm data and identifying them using two LRU queues. It is based on dynamic WL (Yun et al., 2012).	No Buffer	-	-	Hard
HySSD (Oh, Lee, Choi, Lee and Noh, 2013a)	Passing the hot data to SLC and cold data to TLC.	No Buffer	Page Level	Page Level	Hard

Architecture of hybrid storage combined MLC/TLC flash memory for HySSD scheme) Oh et al., 2013 (



Advantages and Disadvantages of (No-Buf)

- Advantages
  - Cost efficient
  - More flexible
- Disadvantages
  - Low performance

Conclusion and Possible Future Directions

- There are several open research trends that have already started on the ground. These future directions are summarized as follow:

- Exploitation Trade-off Among SLC, MLC, and TLC.
- Use Adaptive Parameters for the Future Software Schemes of Hybrid SSD Devices.
- Use File-System-Level Information in Software Schemes of the Hybrid SSD.
- Standardize the Simulators for Evaluation Purposes.
- Build a Standard Benchmark for Comparison Purposes.

Thank you!