



An FPGA Based Enterprise SSD Reference Design

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"The IP enabled solutions provider"

Santa Clara, CA
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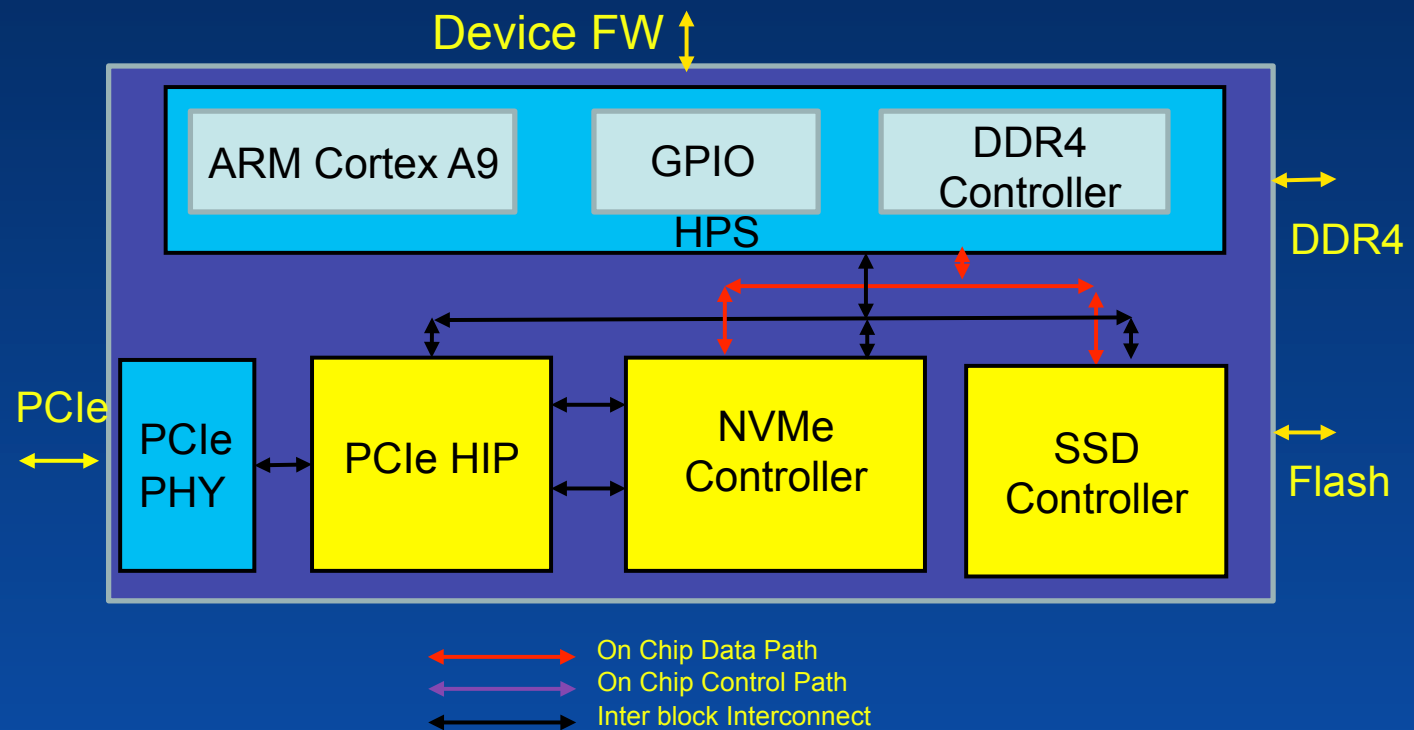
AGENDA

- **FPGA Based Enterprise SSDC**
- **Design Challenges**
- **Configurable IP Components**
- **Mobiveil SSDC Reference Design**
- **Summary**



Arria10 Based NVMe Enterprise SSDC Reference Design

NVMe Based Enterprise SSDC

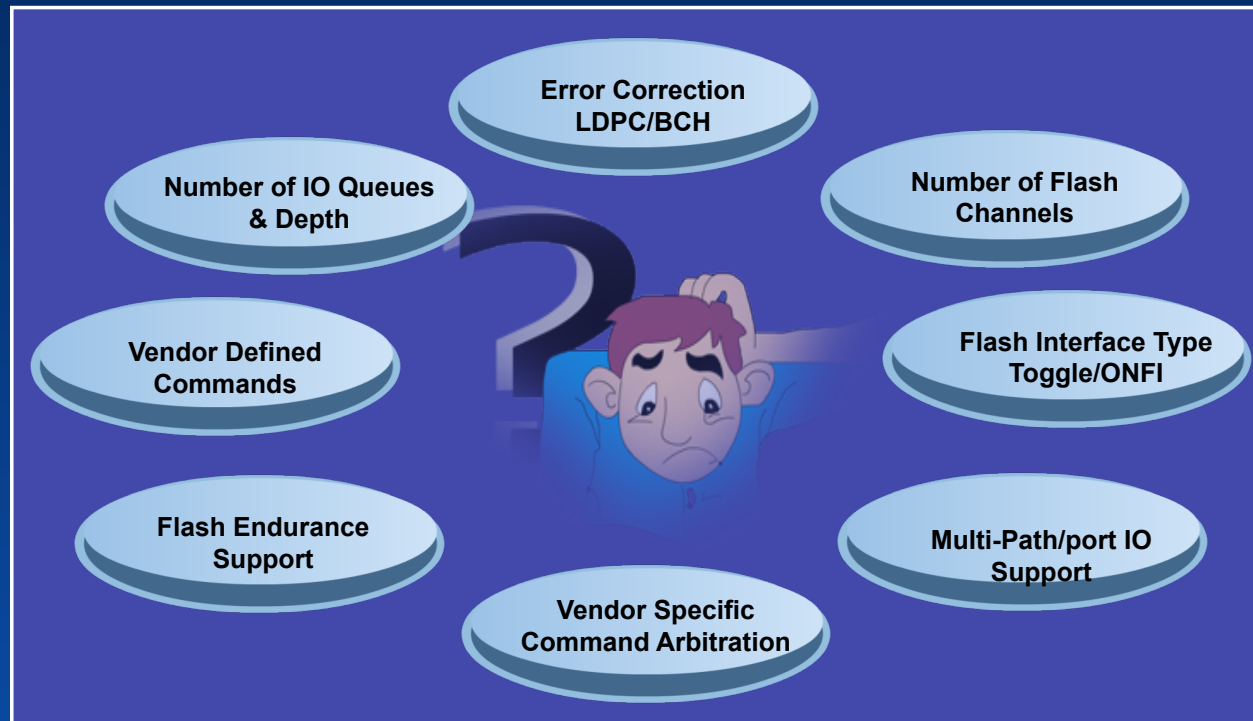




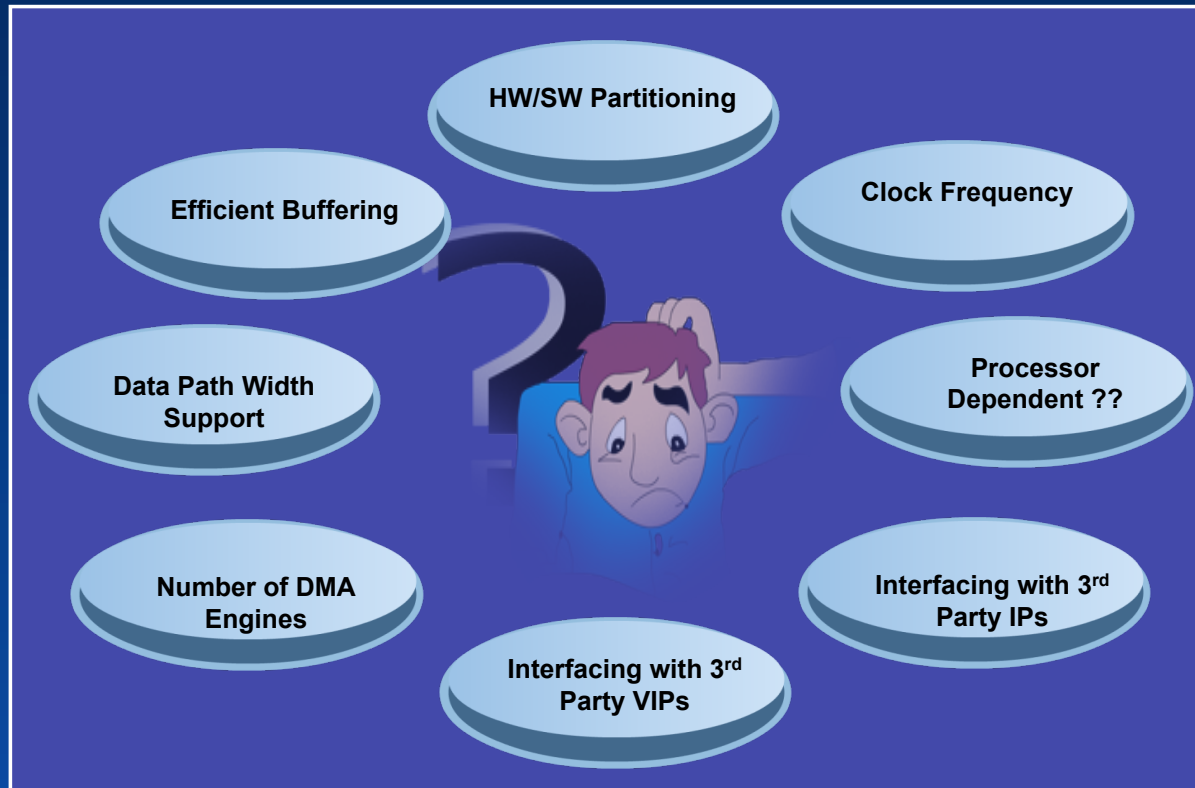
Design Challenges

- Reference Design should be flexible to support different hardware configurations
- Reference Design should be able to handle various target technologies
 - It should be able to handle performance targets across technologies
- Reference Design should allow customization for individual implementations
- Reference Design should provide hooks for Statistics gathering, Error recovery, Reclaim and other value added Enterprise SSD functions

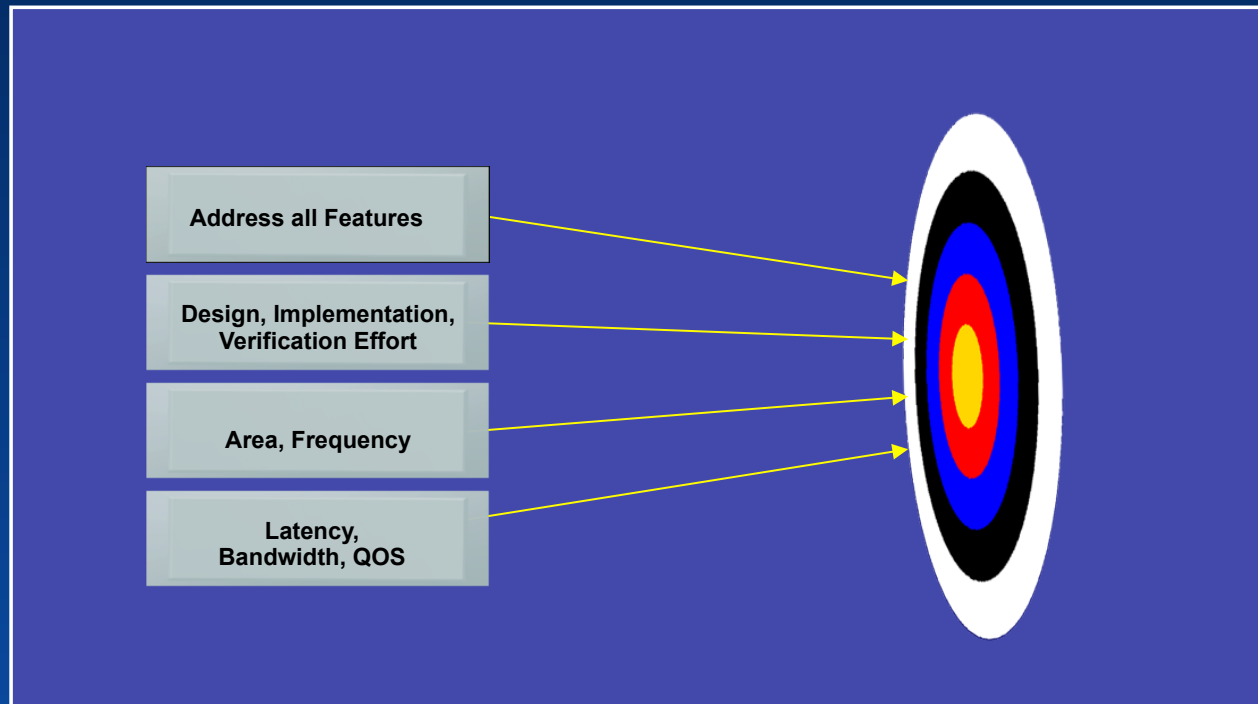
Feature Configurability



Implementation Challenges



Configurable NVMe Based SSDC





Configurable IP Components



UnH Certified NVM Express Controller IP (UNEX)

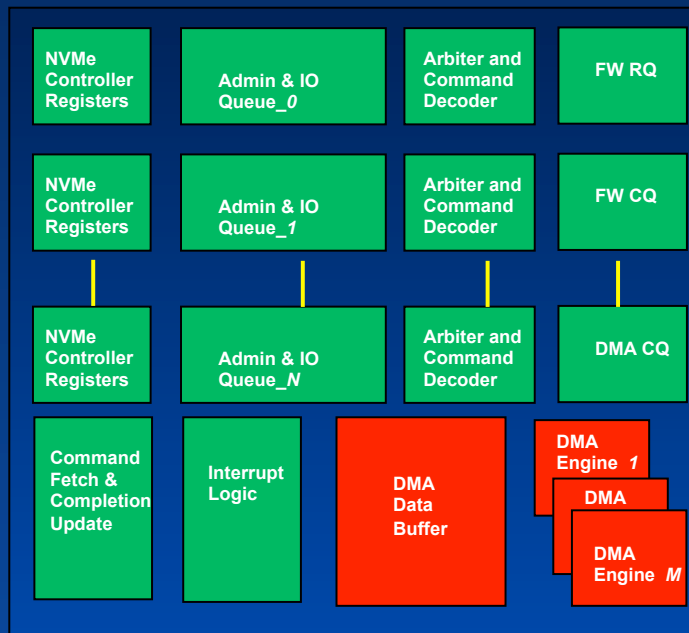


NVM Express (UNEX) Controller

- ✓ Highly Configurable
- ✓ Technology Independent



PCI Subsystem



Memory Subsystem

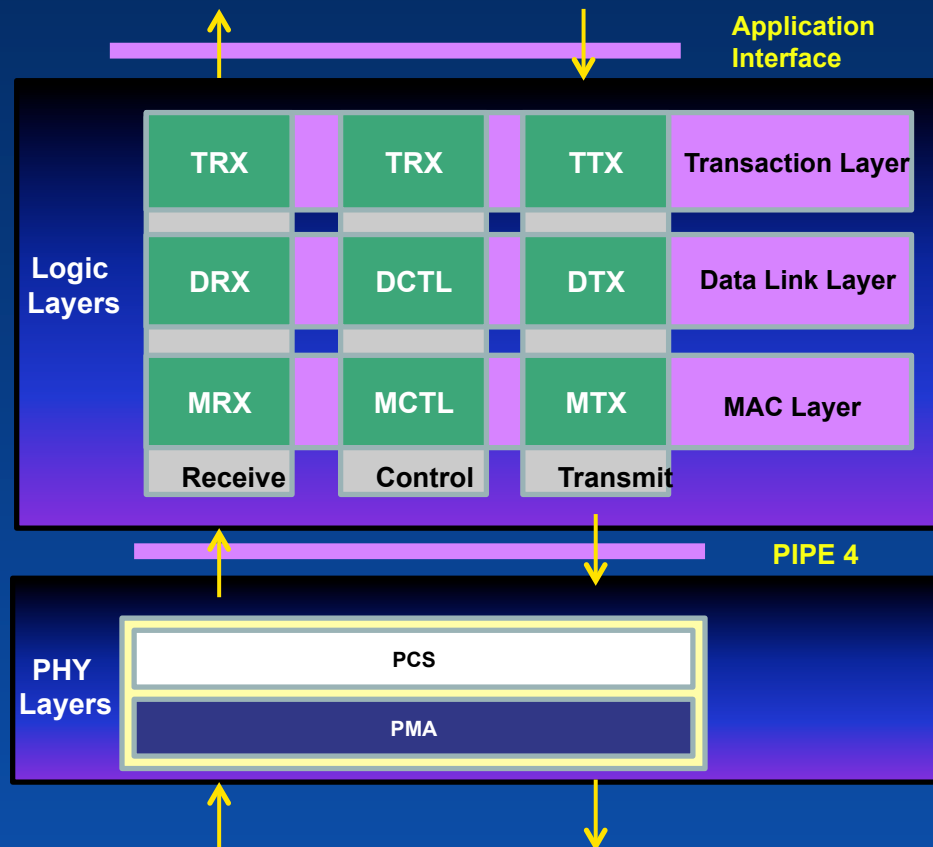
UNEX Controller



PCI Express Controller (GPEX)

PCI Express (GPEX)

- ✓ Highly Configurable
- ✓ Technology Independent
- ✓ System Validated



Gen4/3/2/1
Endpoint
Root Complex
Dual Mode
Switch Port
Switch
AMBA
X1 to x16



DDR4 Memory Controller

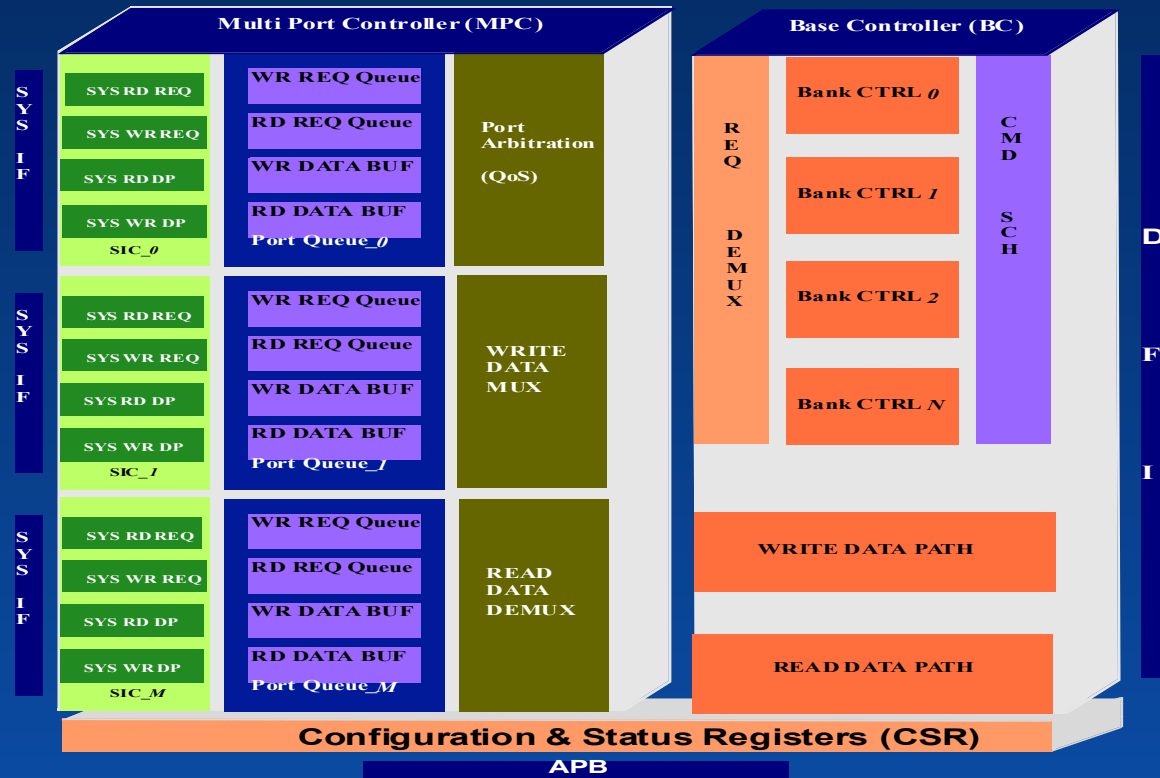


DDR3/4 Controller Requirements

- Compliant with AXI4
- Compliant with DFI 3.1 Interface
- Supports QoS through various arbitration schemes
- Configurable and programmable address mapping
- Supports up to 4 ranks
- Supports following BC Clock to PHY Clock ratio
 - 1:1 (Full-rate Mode)
 - 1:2 (Half-rate Mode)
 - 1:4 (Quarter rate Mode)
- Supports Burst Length 4, 8, 16
- Supports Active/Precharge Power down
- Supports software and hardware driven Self Refresh entry and exit
- Supports Auto-refresh and per-bank refresh
- Supports ECC Checking and Correction (optional)
- Supports automated memory initialization
- Supports ZQ Calibration

DDR4 Memory Controller

- ✓ Highly Configurable
- ✓ Technology Independent

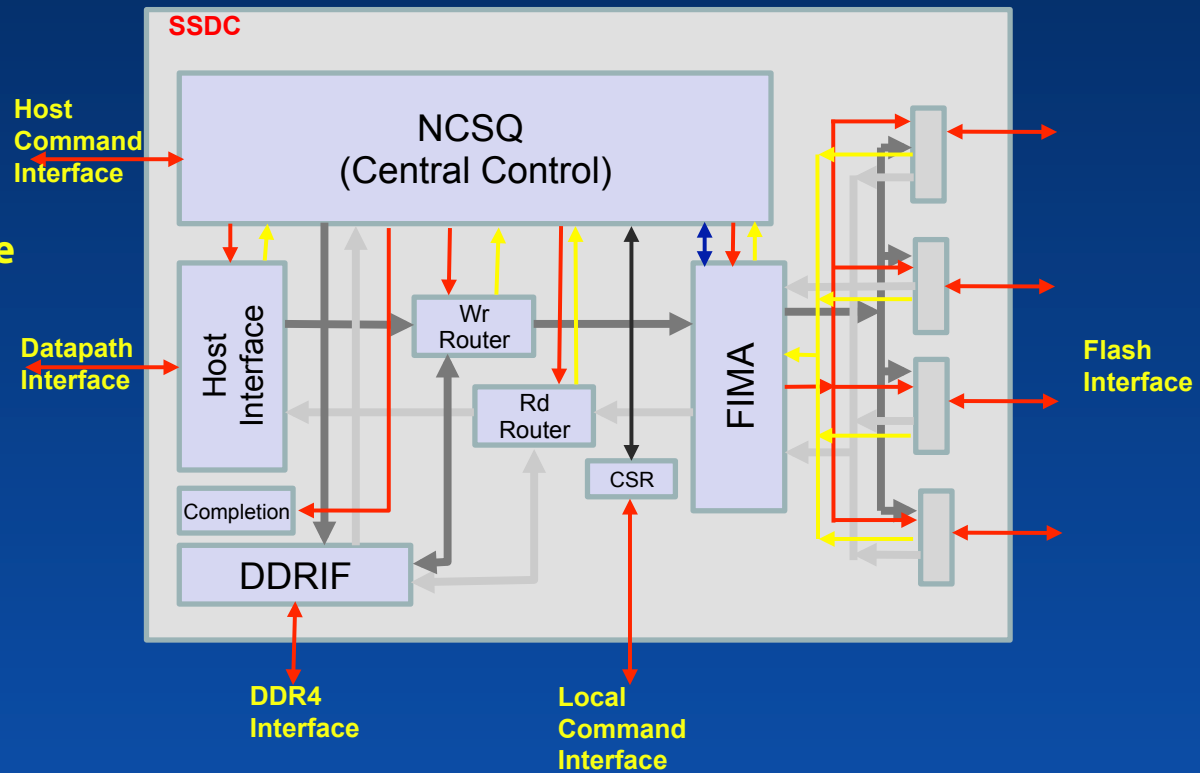




SSD Controller

SSD Controller

- ✓ Highly Configurable
- ✓ Technology Independent





SSD Controller Requirements

- ✓ **Highly Configurable**
- ✓ **Technology Independent**

- **NAND Core Sequencer**

- FTL in Hardware
- Manages all Flash Translation Tables
- Provides Interface to Device FW for Reclaim, Flash endurance Error Logging and other diagnostic feature implementation

- **Flash Interface and Media Access**

- Temporal Sequencing of Read/Write Commands to obtain maximum performance
- Striping and De-striping of data between multiple flash channels (Scatter/Gather).
- Manage the Usage Pools of data (like Hot/Cold Data)
- Implements ECC
- Implements Encryption/Decryption
- Implements Compression/Decompression

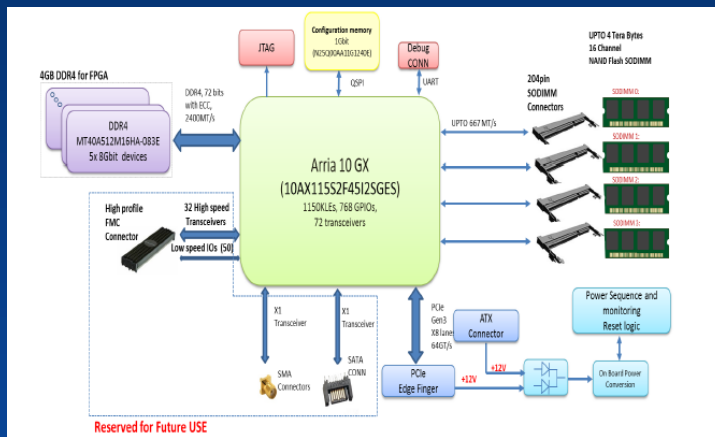


SSD Controller Requirements

- **Host Interface**
 - Interfaces with NVMe Host Command Path
 - Interfaces with NVMe Host Data Path
- **Flash Channel Controller**
 - Implements Flash Interface State Machine
 - Implements Flexible Architecture to support various Flash devices
 - Allows Control Interface to Manage Flash through Test mode (Endurance Support)



NVMe Based Enterprise SSD Reference Board



- High Performance SSD Reference Design with TLC NAND Technology
- Altera PCIe HIP based solution
- UNEX (Universal NVM Express controller) Compliant to NVMe 1.2 specifications
- Up to 16 channels of NAND flash array
- Offers up to 4TB Capacity
- Can be used for Various Flash Device



The Mobiveil Team

- **Leadership**
 - Management with 25+ years experience in Semiconductor/Silicon IP/Systems software
 - Previously founded GDA Technologies, Inc and grew to strong IP and Services group , 500+ engineers strong
 - 5 Patents in Flash Storage and Reliability

Key differentiators

Developed several highly configurable key high speed IP blocks in the last 15+ years (PCI Express, Hyper Transport, Serial RapidIO, SPI4.2, DDR4/3, NVMe and Enterprise Flash Controllers)

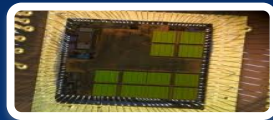
Locations

Headquarters in Milpitas, CA
India design centers: Chennai & Bangalore
Sales: Offices/Reps worldwide





Mobiveil IP Advantages



Market leading & most exhaustively proven cores in the market: *Industry leaders are using these cores*



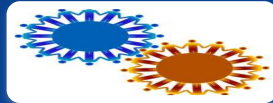
Consortium Participation : *RIO – Member, PCISIG – Member, HMC - Member*



Superior Technical Solution: *Most Feature rich IP, Complete Customization and delivery Solution*



Support: *Clear IP Focus & Worldwide Support*



3rd Party Partnerships for complete Solution: *(Verification and PHY IPs)*



Standard Body Certified Cores: *All Mobiveil IPs are validated and certified: PCI Plug fest, UNH, RTA*

Thank you.

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